| REVISIONS | | | |
|---|---|---|---|
| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
| A | Add RHA criteria and limits. Editorial changes throughout. - jak | 99-05-06 | Monica L. Poelking |
| B | Update the boilerplate paragraphs to current requirements as specified in MIL-PRF-38535. - jak | 09-03-20 | Thomas M Hess |

| | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV | | | | | | | | | | | | | | | | | | | | |
| SHEET | | | | | | | | | | | | | | | | | | | | |
| REV | B | B | B | | | | | | | | | | | | | | | | | |
| SHEET | 15 | 16 | 17 | | | | | | | | | | | | | | | | | |

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| REV STATUS | REV | B | B | B | B | B | B | B | B | B | B | B | B | B | B | B |
| OF SHEETS | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | |

PMIC N/A

PREPARED BY
Marcia B. Kelleher

**DEFENSE SUPPLY CENTER COLUMBUS**
**COLUMBUS, OHIO 43218-3990**
**http://www.dscc.dla.mil**

**STANDARD MICROCIRCUIT DRAWING**

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Monica L. Poelking

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
92-03-18

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, QUAD 2-PORT REGISTER, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

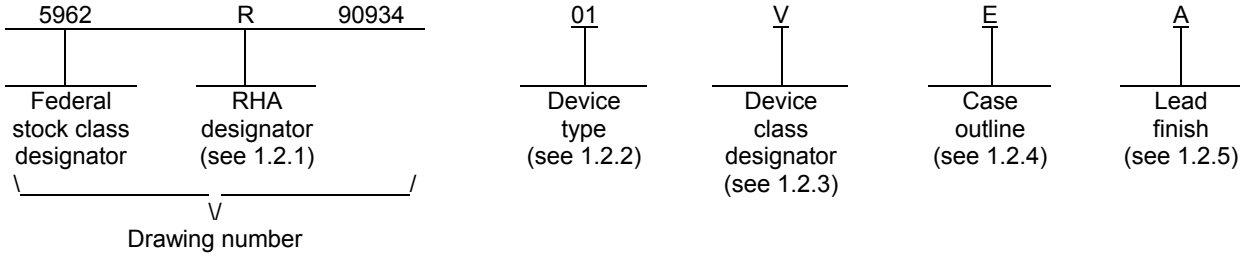
| REVISION LEVEL | SIZE | CAGE CODE | |
|---|---|---|---|
| B | **A** | **67268** | **5962-90934** |

SHEET 1 OF 17

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54ACT399 | Quad 2-port register, TTL compatible inputs |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 pr CDIP2 T-16 | 16 | Dual-in-line |
| F | GDFP2-F16 pr CDFP3 F-16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square leadless chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | -0.5 V dc to +7.0 V dc |
| DC input voltage range ($V_{IN}$) | -0.5 V dc to $V_{CC}$ +0.5 V dc |
| DC output voltage range ($V_{OUT}$) | -0.5 V dc to $V_{CC}$ +0.5 V dc |
| DC input diode current ($I_{IK}$) | ±20 mA |
| DC output diode current ($I_{OK}$) | ±20 mA |
| DC output source or sink current (per pin) ($I_{OUT}$) | ±50 mA |
| DC $V_{CC}$ or GND current | ±200 mA |
| Maximum power dissipation ($P_D$) | 500 mW |
| Storage temperature range ($T_{STG}$) | -65°C to +150°C |
| Lead temperature (soldering, 10 seconds) | +300°C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | +175°C 4/ |

1.4 Recommended operating conditions. 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Input voltage range ($V_{IN}$) | +0.0 V dc to $V_{CC}$ |
| Output voltage range ($V_{OUT}$) | +0.0 V dc to $V_{CC}$ |
| Case operating temperature range ($T_C$) | -55°C to +125°C |
| Input rise or fall rate *( $V_{CC}$ = +4.5 V to 5.5 V) | 0 to 8 ns/V |

1.5 Radiation features.

| | |
|---|---|
| Maximum total dose available (dose rate = 50 – 300 rads (Si)/s) (MIL-STD-883, method 1019, condition A, followed by extended room temperature anneal; effective dose rate ≤ 165 mrads(Si)/s | 100 krads (Si) |

1/ Stresses above the absolute maximum rating may cause permanent damage to the device, Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55°C to +125°C.

4/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening conditions in accordance with method 5004 of MIL-STD-883.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD-20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of this document is available online at www.eia.org/ or from the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 40 (see MIL-PRF-38535, appendix A).

TABLE I. Electrical performance characteristics.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Positive input clamp voltage 3022 | $V_{IC+}$ | For input under test, $I_{IN} = +1.0$ mA | All V | 0.0 V | 1 | 0.4 | 1.5 | V |
| Negative input clamp voltage 3022 | $V_{IC-}$ | For input under test, $I_{IN} = -1.0$ mA | All V | Open | 1 | -0.4 | -1.5 | V |
| High level input voltage | $V_{IH}$ 5/ | | All All | 4.5 V | 1, 2, 3 | 2.0 | | V |
| | | | All All | 5.5 V | 1, 2, 3 | 2.0 | | |
| Low level input voltage | $V_{IL}$ 5/ | | All All | 4.5 V | 1, 2, 3 | | 0.8 | V |
| | | | All All | 5.5 V | 1, 2, 3 | | 0.8 | |
| High level output voltage 3006 | $V_{OH}$ 6/ | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OH} = -50$ µA | All All | 4.5 V | 1, 2, 3 | 4.4 | | V |
| | | | All All | 5.5 V | 1, 2, 3 | 5.4 | | |
| | | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OH} = -24$ mA | All All | 4.5 V | 1, 2, 3 | 3.7 | | |
| | | | All All | 5.5 V | 1, 2, 3 | 4.7 | | |
| | | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OH} = -50$ mA | All All | 5.5 V | 1, 2, 3 | 3.85 | | |
| Low level output voltage 3007 | $V_{OL}$ 6/ | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OL} = +50$ µA | All All | 4.5 V | 1, 2, 3 | | 0.10 | V |
| | | | All All | 5.5 V | 1, 2, 3 | | 0.10 | |
| | | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OL} = +24$ mA | All All | 4.5 V | 1, 2, 3 | | 0.50 | |
| | | | All All | 5.5 V | 1, 2, 3 | | 0.50 | |
| | | $V_{IH} = 2.0$ V or $V_{IL} = 0.8$ V $I_{OL} = +50$ mA | All All | 5.5 V | 1, 2, 3 | | 1.65 | |
| Input leakage current high 3010 | $I_{IH}$ | $V_{IN} = 5.5$ V | All All | 5.5 V | 1, 2, 3 | | 1.0 | µA |
| Input leakage current low 3009 | $I_{IL}$ | $V_{IN} = 0.0$ V | All All | 5.5 V | 1, 2, 3 | | -1.0 | µA |

See footnote at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | Min | Max | |
| Quiescent supply current delta, TTL input levels 3005 | $\Delta I_{CC}$ 7/ | For input under test, $V_{IN} = V_{CC} - 2.1\ V$ For all other inputs, $V_{IN} = V_{CC}$ or GND | | All<br>All | 5.5 V | 1, 2, 3 | | 1.6 | mA |
| | | | M, D | All<br>All | 5.5 V | 1 | | 1.6 | |
| | | | P, L, R | All<br>All | 5.5 V | 1 | | 3.5 | mA |
| Quiescent supply current outputs high 3005 | $I_{CCH}$ | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0.0\ A$ | | All<br>All | 5.5 V | 1, 2, 3 | | 80.0 | µA |
| | | | M, D | All<br>All | 5.5 V | 1 | | 300.0 | |
| | | | D | | | | | 1.0 | mA |
| | | | P, L, R | | | | | 3.5 | |
| Quiescent supply current outputs low 3005 | $I_{CCL}$ | $V_{IN} = V_{CC}$ or GND $I_{OUT} = 0.0\ A$ | | All<br>All | 5.5 V | 1, 2, 3 | | 80.0 | µA |
| | | | M, D | All<br>All | 5.5 V | 1 | | 300.0 | |
| | | | D | | | | | 1.0 | mA |
| | | | P, L, R | | | | | 3.5 | |
| Input capacitance 3012 | $C_{IN}$ | See 4.4.1c $T_C = +25°C$ | | All<br>All | GND | 4 | | 10.0 | pF |
| Power dissipation capacitance | $C_{PD}$ 8/ | See 4.4.1c $T_C = +25°C$ $f = 1\ MHz$ | | All<br>All | 5.0 V | 4 | | 40.0 | pF |
| Functional tests 3014 | 9/ | See 4.4.1b $V_{IN} = V_{IL}$ or $V_{IH}$ Verify output $V_{OUT}$ | | All<br>All | 4.5 V | 7, 8 | L | H | |
| | | | | | 5.5 V | 7, 8 | L | H | |
| Propagation delay time, CP to Qn 3003 | $t_{PHL}$, $t_{PLH}$ 10/ | $C_L = 50\ pF$ minimum $R_L = 500\Omega$ See figure 4 | | All<br>All | 4.5 V | 9 | 1.0 | 9.0 | ns |
| | | | | All<br>All | 4.5 V | 10, 11 | 1.0 | 10.0 | ns |

See footnotes at end of table.

TABLE I. Electrical performance characteristics – Continued.

| Test and MIL-STD-883 test method 1/ | Symbol | Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified | Device type and device class | $V_{CC}$ | Group A subgroups | Limits 4/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Clock pulse width, high or low | $t_{w1}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9, 10, 11 | 5.0 | | ns |
| Input setup time, lmn to CP High or low | $t_{s1}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9 | 3.0 | | ns |
| | | | All<br>All | 4.5 V | 10, 11 | 3.5 | | ns |
| Input hold time, lmn to CP, high or low | $t_{h1}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9, 10, 11 | 3.0 | | ns |
| Input setup time, S to CP High or low | $t_{s2}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9 | 5.0 | | ns |
| | | | All<br>All | 4.5 V | 10, 11 | 6.0 | | ns |
| Input hold time, S to CP High or low | $t_{h2}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9 | 2.0 | | ns |
| | | | All<br>All | 4.5 V | 10, 11 | 2.5 | | ns |
| Maximum clock frequency | $f_{MAX}$ 11/ | $C_L$ = 50 pF<br>$R_L$ = 500Ω<br>See figure 4 | All<br>All | 4.5 V | 9 | 95 | | MHz |
| | | | All<br>All | 4.5 V | 10, 11 | 90 | | MHz |

1/ For tests not listed in the referenced MIL-STD-883 (e.g. $\Delta I_{CC}$), utilize the general test procedure under the conditions listed herein.

2/ Each input/output, as applicable shall be tested at the specified temperature for the specified limits. Output terminals not designated shall be high level logic, low level logic, or open, except as follows:

a. $V_{IC}$ (pos) tests, the GND terminal can be open. $T_C$ = +25°C.
b. $V_{IC}$ (neg) tests, the $V_{CC}$ terminal shall be open. $T_C$ = +25°C.
c. All $I_{CC}$ tests, the output terminal shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter.

Additional detailed information on qualified devices (i.e. pin for pin conditions and testing sequence) is available from the qualifying activity (DSCC-VQC) upon request.

3/ RHA parts supplied to this drawing are tested through all levels M, D, P, L, and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in table I. When performing post irradiation electrical measurements for any RHA level, $T_A$ = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein. All devices shall meet or exceed the limits specified in table I, as applicable, at $4.5\ V \le V_{CC} \le 5.5\ V$.

TABLE I. Electrical performance characteristics – Continued.

5/ The $V_{IH}$ and $V_{IL}$ tests are not required if applied as forcing functions for the $V_{OH}$ and $V_{OL}$ tests.

6/ The $V_{OH}$ and $V_{OL}$ tests shall be tested at $V_{CC}$ = 4.5 V. The $V_{OH}$ and $V_{OL}$ tests are guaranteed, if not tested, for $V_{CC}$ = 5.5 V. Limits shown apply to operation at $V_{CC}$ = 5.0 V ±0.5 V. Transmission driving tests are performed at $V_{CC}$ = 5.5 V with a 2 ms duration maximum. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for $V_{IH}$ = 2.0 V or $V_{IL}$ = 0.8 V

7/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at $V_{IN} = V_{CC}$ - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times 1.6 mA; and the preferred method and limits are guaranteed.

8/ Power dissipation capacitance ($C_{PD}$) determines the power consumption ($P_D$) and the current consumption ($I_S$).
Where:
$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (nxdx\Delta I_{CC}xV_{CC})$
$I_S = (C_{PD} + C_L)V_{CC}f + I_{CC} + (nxdx\Delta I_{CC})$
f is the frequency of the input signal; n is the number of device inputs at TTL levels; and d is the duty cycle of the signal, and $C_L$ is the external output load capacitance.

9/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, $V_{IL}$ = 0.4 V and $V_{IH}$ = 2.4 V. For outputs, L ≤ 0.8 V, H ≥ 2.0 V.

10/ AC limits at $V_{CC}$ = 5.5 V are equal to limits at $V_{CC}$ = 4.5 V and guaranteed by testing at $V_{CC}$ = 4.5 V. Minimum AC limits for $V_{CC}$ = 5.5 V are 1.0 ns and guaranteed by guardbanding the $V_{CC}$ = 4.5 V minimum limits to 1.5 ns. For propagation delay tests, all paths must be tested.

11/ This parameter shall be guaranteed, if not tested, to the limits in table I, herein.

| Device type | 01 | |
|---|---|---|
| Case outlines | E and F | 2 |
| Terminal number | Terminal symbol | |
| 1 | S | NC |
| 2 | Qa | S |
| 3 | I0a | Qa |
| 4 | I1a | I0a |
| 5 | I1b | I1a |
| 6 | I0b | NC |
| 7 | Qb | I1b |
| 8 | GND | I0b |
| 9 | CP | Qb |
| 10 | Qc | GND |
| 11 | I0c | NC |
| 12 | I1c | CP |
| 13 | I1d | Qc |
| 14 | I0d | I0c |
| 15 | Qd | I1c |
| 16 | $V_{CC}$ | NC |
| 17 | - - - | I1d |
| 18 | - - - | I0d |
| 19 | - - - | Qd |
| 20 | - - - | $V_{CC}$ |

NC = No internal connection.

| Terminal connections | |
|---|---|
| Terminal symbol | Description |
| S | Common Select Input |
| CP | Clock Pulse Input |
| Imn (m = 0 or 1), (n = a to d) | Data Inputs |
| Qn (n = a to d) | Data Outputs (non-inverting) |

FIGURE 1. Terminal connections.

| Inputs | | | | Outputs |
|---|---|---|---|---|
| S | I0n | I1n | CP | Qn |
| L | L | X | ↑ | L |
| L | H | X | ↑ | H |
| H | X | L | ↑ | L |
| H | X | H | ↑ | H |

H = High voltage level
L = Low voltage level
X = Irrelevant
↑ = Low-to-high clock transition

FIGURE 2. Truth table.

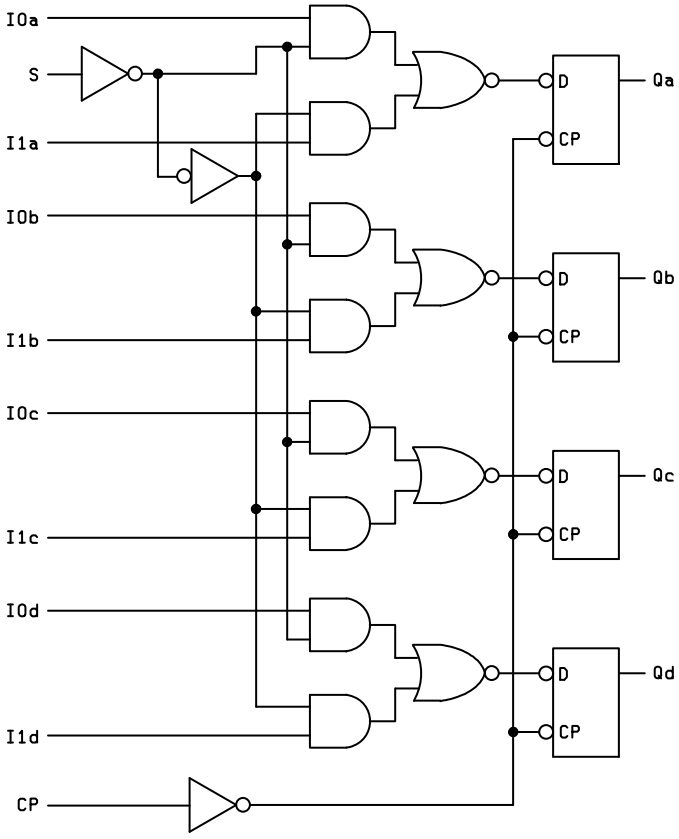



FIGURE 3. Logic diagram.

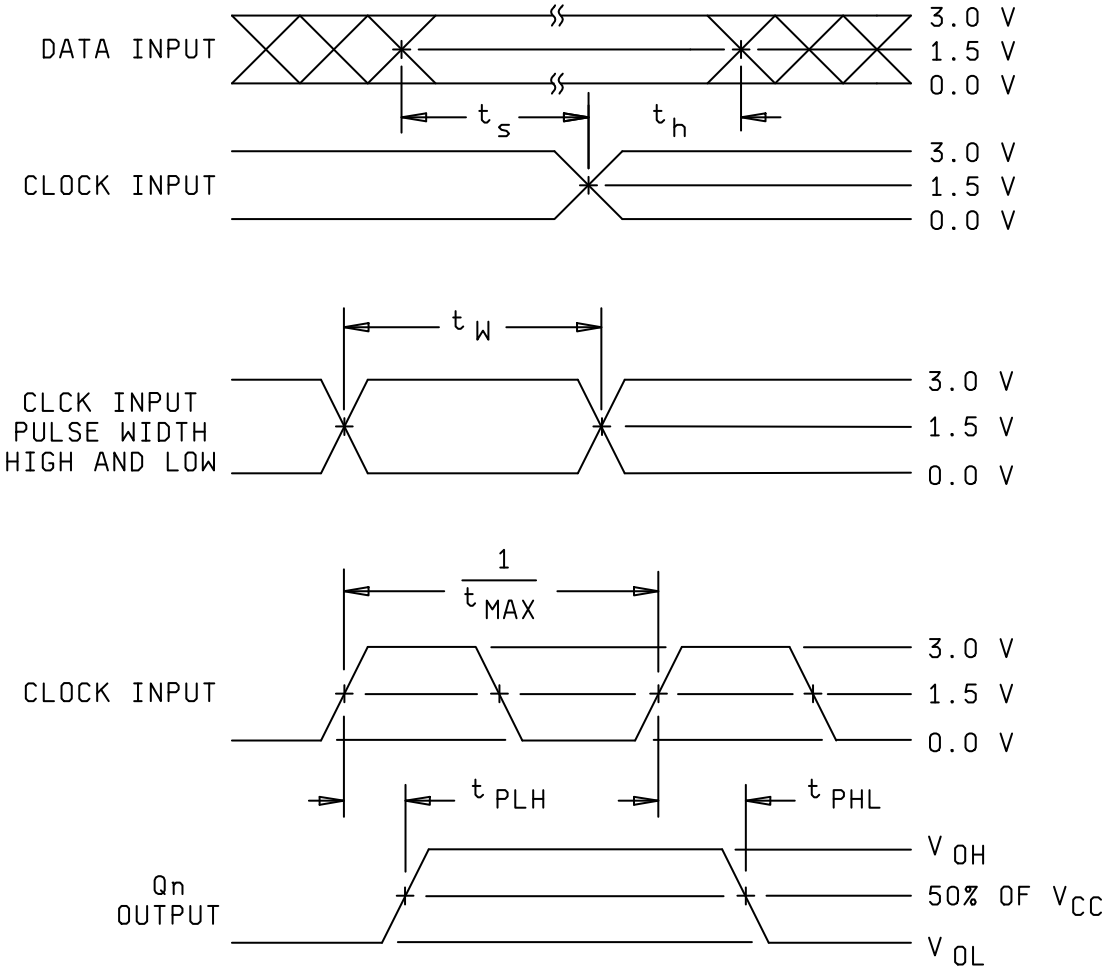
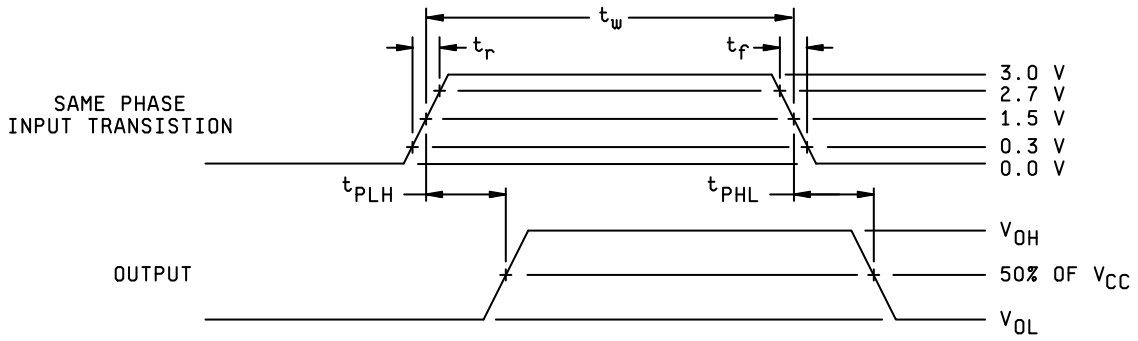
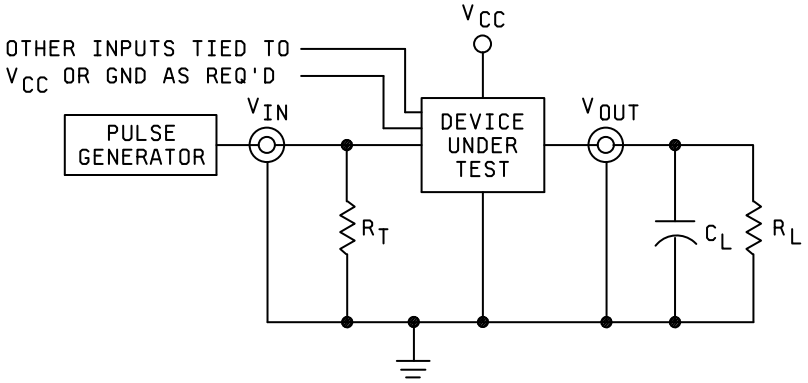



FIGURE 5. Switching waveforms and test circuit.




NOTES:

1. $C_L$ = 50 pF minimum (includes test jig and probe capacitance).
2. $R_T$ = 50Ω or equivalent, $R_L$ = 500Ω or equivalent.
3. Input signal from the pulse generator: $V_{IN}$ = 0.0 V to 3.0 V; PRR ≤ 10 MHz, $t_r$ = 3.0 ns, $t_f$ = 3.0 ns. $t_r$ and $t_f$ shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 5. Switching waveforms and test circuit – Continued.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. $C_{IN}$ and $C_{PD}$ shall be measured only for initial qualification and after process or design changes which may affect capacitance. $C_{IN}$ shall be measured between the designated terminal and GND at a frequency of 1 MHz. $C_{PD}$ shall be tested in accordance with the latest revision of JESD 20 and table I herein. For $C_{IN}$ and $C_{PD}$, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | 1 |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9 | 1/ 1, 2, 3, 7, 8, 9, 10, 11 | 2/ 1, 2, 3, 7, 8, 9, 10, 11 |
| Group A test requirements (see 4.4) | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 | 1, 2, 3, 4, 7, 8, 9, 10, 11 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3, 7, 8, 9, 10, 11 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

1. Inputs tested high, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 5.0 V dc +5%, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

2. Inputs tested low, $V_{CC}$ = 5.5 V dc +5%, $R_{CC}$ = 10Ω ±20%, $V_{IN}$ = 0.0 V dc, $R_{IN}$ = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table I herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 09-03-20

Approved sources of supply for SMD 5962-90934 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9093401M2A | 0C7V7 | 54ACT399LMQB |
| 5962-9093401MEA | 0C7V7 | 54ACT399DMQB |
| 5962-9093401MFA | 0C7V7 | 54ACT399FMQB |
| 5962-9093401Q2A | 0C7V7 | 54ACT399LMQB |
| 5962-9093401QEA | 0C7V7 | 54ACT399DMQB |
| 5962-9093401QFA | 0C7V7 | 54ACT399FMQB |
| 5962R9093401Q2A | 3/ | 54ACT399 |
| 5962R9093401QEA | 3/ | 54ACT399 |
| 5962R9093401QFA | 3/ | 54ACT399 |
| 5962R9093401V2A | 3/ | 54ACT399 |
| 5962R9093401VEA | 3/ | 54ACT399 |
| 5962R9093401VFA | 3/ | 54ACT399 |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 0C7V7 | QP Semiconductor<br>2945 Oakmead Village Court<br>Santa Clara, CA 95051 |

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Encoders, Decoders, Multiplexers & Demultiplexers ***category:***

***Click to view products by*** E2v ***manufacturer:***

Other Similar products are found below :

M38510/01406BEA MC74HC163ADTG 74HC253N HMC854LC5TR NLV74VHC1G01DFT1G NLVHC4851ADTR2G NLVHCT4851ADTR2G PI3B33X257BE M74HCT4052ADTR2G M74VHC1GT04DFT3G TC74AC138P(F) MC74LVX4051MNTWG HMC855LC5TR NLV14028BDR2G NLV14051BDR2G NLV74HC238ADTR2G 715428X COMX-CAR-210 5962-8607001EA 5962-8756601EA MAX3783UCM+D PI5C3253QEX 8CA3052APGGI8 TC74HC4051AF(EL,F) TC74VHC138F(EL,K,F PI3B3251LE PI5C3309UEX PI5C3251QEX PI3B3251QE 74VHC4052AFT(BJ) PI3PCIE3415AZHEX NLV74HC4851AMNTWG MC74LVX257DG M74HC151YRM13TR M74HC151YTTR PI5USB31213XEAEX M74HCT4851ADWR2G XD74LS154 AP4373AW5-7-01 QS3VH251QG8 QS4A201QG HCS301T-ISN HCS500-I/SM MC74HC151ADTG TC4066BP(N,F) 74ACT11139PWR HMC728LC3CTR 74VHC238FT(BJ) 74VHC4066AFT(BJ) 74VHCT138AFT(BJ)