REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Delete vendor CAGE 18714. Add vendor CAGE 27014. Technical and editorial changes throughout.	91-10-28	M. A. Frye
B	Add device class V criteria. Add RHA characterization data. Editorial changes throughout. - jak	97-07-21	Monica L. Poelking
C	Add vendor CAGE F8859. Add device type 03. Add radiation features section. Make corrections to table I to accommodate device type 03. Add notes to figure 4. Add table III. Update the boilerplate to MIL-PRF-38535 requirements. - jak	04-05-07	Thomas M Hess
D	Add appendix A, microcircuit die. Update the boilerplate to current MIL-PRF-38535 requirements and to include radiation hardness assurance requirements. - jak	07-09-13	Thomas M. Hess

REV																				
SHEET																				
REV	D	D	D	D	D	D	D	D	D											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS OF SHEETS	REV	D	D	D	D	D	D	D	D	D	D	D	D	D	D
	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
Marcia B. Kelleher

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thomas J. Ricciuti

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
89-08-22

REVISION LEVEL
D

MICROCIRCUIT, DIGITAL, ADVANCED CMOS, QUAD TWO-INPUT POSITIVE OR GATE, TTL COMPATIBLE INPUTS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-89736**

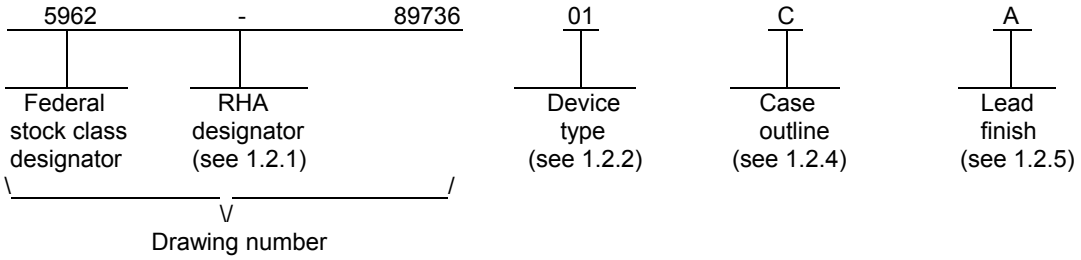
SHEET 1 OF 23

1. SCOPE

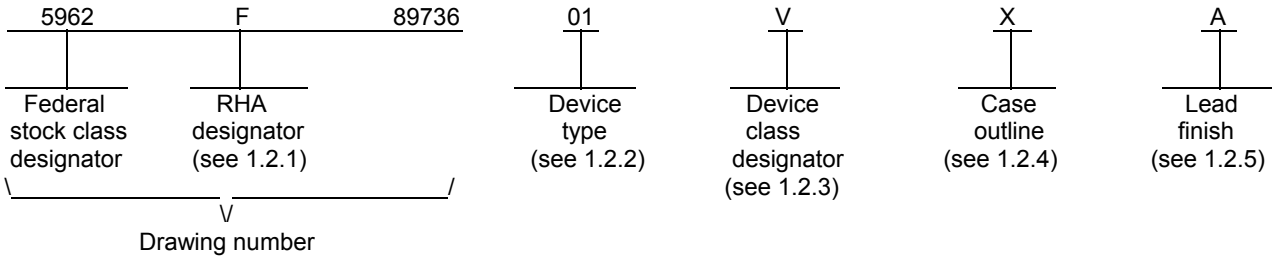
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:

For device classes M and Q:



For device class V:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACT32	Quad two-input OR gate, TTL compatible inputs
02	54ACT11032	Quad two-input OR gate, TTL compatible inputs
03	54ACT32	Quad two-input OR gate, TTL compatible inputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as listed below. Since the device class designator has been added after the original issuance of this drawing, device classes M and Q designators will not be included in the PIN and will not be marked on the device.

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
C	GDIP1-T14 or CDIP2-T14	14	Dual-in-line
D	GDFP1-F14 or CDFP2-F14	14	Flat pack
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
2	CQCC1-N20	20	Square leadless chip carrier
X	CDFP3-F14	14	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{CC}) ..... -0.5 V dc to +6.0 V dc
DC input voltage range (V_{IN}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC output voltage range (V_{OUT}) ..... -0.5 V dc to V_{CC} + 0.5 V dc
DC input diode current ..... ±20 mA
DC output diode current (per pin) ..... ±50 mA
DC output source or sink current ..... ±50 mA
DC V_{CC} or GND current ..... ±50 mA 4/
Maximum power dissipation (P_D) ..... 500 mW
Storage temperature range (T_{STG}) ..... -65°C to +150°C
Lead temperature (soldering, 10 seconds):
  Case outline X ..... +260°C
  All other case outlines except case X ..... +300°C
Thermal resistance, junction-to-case (Θ_{JC}) ..... See MIL-STD-1835
Junction temperature (T_J) ..... +175°C

1.4 Recommended operating conditions. 2/ 3/ 5/

Supply voltage range (V_{CC}) ..... 4.5 V dc to +5.5 V dc
Minimum high level input voltage (V_{IH}) ..... 2.0 V dc
Maximum low level input voltage (V_{IL}) ..... 0.8 V dc
Input voltage range (V_{IN}) ..... +0.0 V dc to V_{CC}
Output voltage range (V_{OUT}) ..... +0.0 V dc to V_{CC}
Maximum input rise or fall rate ($\Delta t/\Delta V$) ..... 0 to 8 ns/V
Case operating temperature range (T_C) ..... -55°C to +125°C

1.5 Radiation features.

Maximum total dose available (dose rate = 50 – 300 rads (Si)/s):
  Device type 01 ..... 100 krads (Si)
  Device type 03 ..... 300 krads (Si)
Single Event Latch-up (SEL):
  Device type 01 ..... ≥ 100 MeV-cm^2/ mg 6/
Single Event Latch-up (SEL) or single event upset (SEU):
  Device type 03 ..... ≥ 93 MeV-cm^2/ mg 6/

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to GND.
3/ The limits for the parameters specified herein shall apply over the full specified V_{CC} range and case temperature range of -55°C to +125°C.
4/ For packages with multiple V_{CC} and GND pins, this value represents the total current into all V_{CC} or GND.
5/ Unused inputs must be held high or low to prevent them from floating.
6/ Limits are guaranteed by design or process but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

ELECTRONIC INDUSTRIES ALLIANCE (EIA)

JESD 78 - IC Latch-Up Test

JEDEC Standard No. 20 - Standard for Description of 54/74ACXXXX and 54/74ACTXXXX Advanced High-Speed CMOS Devices.

(Copies of this document is available online at www.eia.org/ or from the Electronics Industries Alliance, 2500 Wilson Boulevard, Arlington, VA 22201-3834).

AMERICAN SOCIETY FOR TESTING AND MATERIALS (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of semiconductor Devices.

(Copies of these documents are available online at http://www.astm.org or from ASTM International, 100 Barr Harbor Drive, P.O. Box C700, West Conshohocken, PA, 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change that affects this drawing.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

TABLE IA. Electrical performance characteristics.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 4/		Unit
						Min	Max	
Positive input clamp voltage 3022	V_{IC+}	For input under test, I_{IN} = 18 mA	01, 02 V	GND	1, 2, 3		5.7	V
		M, D, P, L, R	01 V		1		5.7	
		For input under test, I_{IN} = 1 mA	03 Q, V		1, 2, 3	0.4	1.5	V
Negative input clamp voltage 3022	V_{IC-}	For input under test, I_{IN} = -18 mA	01, 02 V	Open	1, 2, 3		-1.2	V
		M, D, P, L, R	01 V		1		-1.2	
		For input under test, I_{IN} = -1 mA	03 Q, V		1, 2, 3	-0.4	-1.5	V
High level output voltage	V_{OH} 5/	V_{IN} = 2.0 V or 0.8 V I_{OH} = -50 µA	All All	4.5 V	1, 2, 3	4.4		V
		M, D, P, L, R	01 V	4.5 V	1	4.4		
			All All	5.5 V	1, 2, 3	5.4		
		M, D, P, L, R	01 V	5.5 V	1	5.4		
		V_{IN} = 2.0 V or 0.8 V I_{OH} = -24 mA	All All	4.5 V	1, 2, 3	3.7		
		M, D, P, L, R	01 V	4.5 V	1	3.7		
			All All	5.5 V	1, 2, 3	4.7		
		M, D, P, L, R	01 V	5.5 V	1	4.7		
		V_{IN} = 2.0 V or 0.8 V I_{OH} = -50 mA	All All	5.5 V	1, 2, 3	3.85		
		M, D, P, L, R	01 V	5.5 V	1	3.85		
Low level output voltage 3007	V_{OL} 5/	V_{IN} = 2.0 V or 0.8 V I_{OL} = 50 µA	All All	4.5 V	1, 2, 3		0.1	V
		M, D, P, L, R	01 V	4.5 V	1		0.1	
			All All	5.5 V	1, 2, 3		0.1	
		M, D, P, L, R	01 V	5.5 V	1		0.1	
		V_{IN} = 2.0 V or 0.8 V I_{OL} = 24 mA	All All	4.5 V	1, 2, 3		0.5	
		M, D, P, L, R	01 V	4.5 V	1		0.5	
			All All	5.5 V	1, 2, 3		0.5	
		M, D, P, L, R	01 V	5.5 V	1		0.5	
		V_{IN} = 2.0 V or 0.8 V I_{OL} = 50 mA	All All	5.5 V	1, 2, 3		1.65	
		M, D, P, L, R	01 V	5.5 V	1		1.65	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics – Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ -55°C ≤ T_C ≤ +125°C +4.5 V ≤ V_{CC} ≤ +5.5 V unless otherwise specified		Device type and Device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Input leakage current high 3010	I_{IH}	V_{IN} = 5.5 V		All All	5.5 V	1, 2, 3		1.0	µA
			M, D, P, L, R	01 V	5.5 V	1		1.0	
Input leakage current low 3009	I_{IL}	V_{IN} = 0.0 V		All All	5.5 V	1, 2, 3		-1.0	µA
			M, D, P, L, R	01 V	5.5 V	1		-1.0	
Quiescent supply current delta, TTL input levels	ΔI_{CC} 6/	For input under test, V_{IL} = V_{CC} - 2.1 V For all other inputs, V_{IN} = V_{CC} or GND		All All	5.5 V	1, 2, 3		1.6	mA
			M, D	01 V		1		1.6	
			P, L, R					3.5	
Quiescent supply current high 3005	I_{CCH}	V_{IN} = 5.5 V		01, 02 All	5.5 V	1, 2, 3		80	µA
			M	01 V		1		100	
			D					1.0	mA
			P, L, R					3.5	
		V_{IN} = 5.5 V		03 All	5.5 V	1		2.0	µA
						2, 3		80	
			M, D, P, L, R, F 7/	03 Q, V		1		50	
Quiescent supply current low 3005	I_{CCL}	V_{IN} = 0.0 V		01, 02 All	5.5 V	1, 2, 3		80	µA
			M	01 V		1		100	
			D					1.0	mA
			P, L, R					3.5	
		V_{IN} = 0.0 V		03 All	5.5 V	1		2.0	µA
						2, 3		80	
			M, D, P, L, R, F 7/	03 Q, V		1		50	
Input capacitance 3012	C_{IN}	See 4.4.1c T_C = +25°C		All All	GND	4		10.0	pF
Power dissipation capacitance	C_{PD} 8/	See 4.4.1c T_C = +25°C f = 1 MHz		01, 03 All	5.0 V	4		72	pF
				02 All				32	
Latch-up input/output over-voltage	I_{CC} (O/V1) 9/	$t_w \geq 100$ µs, $t_{cool} \geq t_w$ 5 µs ≤ t_r ≤ 5 ms 5 µs ≤ t_f ≤ 5 ms V_{test} = 6.0 V, V_{CCQ} = 5.5 V V_{over} = 10.5 V See 4.4.1d		All V	5.5 V	2		200	mA

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method 1/	Symbol	Test conditions 2/ 3/ $-55°C \le T_C \le +125°C$ $+4.5\ V \le V_{CC} \le +5.5\ V$ unless otherwise specified	Device type and Device class	V_{CC}	Group A subgroups	Limits 4/ Min	Limits 4/ Max	Unit
Latch-up input/output positive over-current	I_{CC} (O/I1+) 9/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = +120\ mA$ See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up input/output negative over-current	I_{CC} (O/I1-) 9/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $I_{trigger} = -120\ mA$ See 4.4.1d	All V	5.5 V	2		200	mA
Latch-up supply over-voltage	I_{CC} (O/V2) 9/	$t_w \ge 100\ \mu s$, $t_{cool} \ge t_w$ $5\ \mu s \le t_r \le 5\ ms$ $5\ \mu s \le t_f \le 5\ ms$ $V_{test} = 6.0\ V$, $V_{CCQ} = 5.5\ V$ $V_{over} = 9.0\ V$ See 4.4.1d	All V	5.5 V	2		100	mA
Functional tests 3014	10/	See 4.4.1b, $V_{IH} = 2.0\ V$, $V_{IL} = 0.8\ V$ Verify output V_{OUT}	All All	4.5 V	7, 8	L	H	
				5.5 V		L	H	
		M, D, P, L, R	01 V	4.5 V	7	L	H	
Propagation delay time, nA, nB to nY 3003	t_{PLH} 11/	$C_L = 50\ pF$ $R_L = 500\Omega$ See figure 4	01 All	4.5 V	9	1.5	7.0	ns
			02, 03 All			1.5	8.1	
		M, D, P, L, R	01 V		9	1.5	7.0	
			01 All		10, 11	1.5	7.5	
			02 All			1.5	9.6	
			03 All			1.5	9.0	
	t_{PHL} 11/	$C_L = 50\ pF$ $R_L = 500\Omega$ See figure 4	01 All	4.5 V	9	1.5	7.0	
			02 All			1.5	7.4	
			03 All			1.5	8.0	
		M, D, P, L, R	01 V		9	1.5	7.0	
			01 All		10, 11	1.5	7.5	
			02 All			1.5	8.4	
			03 All			1.5	9.0	

See footnotes on next sheet.

TABLE IA. Electrical performance characteristics - Continued.

1/ For tests not listed in the referenced MIL-STD-883, (e.g. ΔI_{CC}), utilize the general test procedure of 883 under the conditions listed herein. All inputs and outputs shall be tested, as applicable, to the tests in table IA herein.

2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table herein. Output terminals not designated shall be high level logic, low level logic, or open except for the I_{CC} and ΔI_{CC} tests, the output terminal shall be open. When performing the I_{CC} and ΔI_{CC} tests, the current meter shall be placed in the circuit such that all current flows through the meter.

3/ RHA parts for device type 01 supplied to this drawing are tested through all levels M, D, P, L, and R of irradiation. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

RHA parts for device type 03 supplied to this drawing have been characterized through all levels M, D, P, L, R, and F of irradiation. However, this device is only tested at the 'F' level. Pre and Post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C.

4/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

5/ The V_{OH} and V_{OL} tests shall be tested at V_{CC} = 4.5 V. The V_{OH} and V_{OL} tests are guaranteed, if not tested, for V_{CC} = 5.5 V. Limits shown apply to operation at V_{CC} = 5.0 V ±0.5 V. Transmission driving tests are performed at V_{CC} = 5.5 V with a 2 ms duration maximum. Transmission driving tests may be performed using $V_{IN} = V_{CC}$ or GND. When $V_{IN} = V_{CC}$ or GND is used, the test is guaranteed for V_{IN} = 2.0 V or 0.8 V.

6/ This test may be performed either one input at a time (preferred method) or with all input pins simultaneously at V_{IN} = - 2.1 V (alternate method). Classes Q and V shall use the preferred method. When the test is performed using the alternate test method, the maximum limit is equal to the number of inputs at a high TTL input level times ΔI_{CC} maximum; and the preferred method and limits are guaranteed.

7/ The maximum limit for this parameter at 100 krads (Si) is 2 μA.

8/ Power dissipation capacitance (C_{PD}) determines both the power consumption (P_D) and current consumption (I_S).
Where: $P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC}) + (n \times d \times \Delta I_{CC} \times V_{CC})$
$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC} + (n \times d \times \Delta I_{CC})$
f is the frequency of the input signal; n is the number of device inputs at TTL levels; d is the duty cycle of the input signal; and C_L is the external output load capacitance.

9/ See EIA/JEDEC STD. 78 for electrically induced latch-up test methods and procedures. The values listed for $I_{trigger}$ and V_{over}, are to be accurate within ±5 percent.

10/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. After incorporating allowable tolerances per MIL-STD-883, V_{IL} = 0.4 V and V_{IH} = 2.4 V. For outputs, L ≤ 0.8 V H ≥ 2.0 V.

11/ For propagation delay tests, all paths must be tested. AC limits at V_{CC} = 5.5 V are equal to limits at V_{CC} = 4.5 V and guaranteed by testing at V_{CC} = 4.5 V. Minimum AC limits are guaranteed for V_{CC} = 5.5 V by guardbanding the V_{CC} = 4.5 V minimum limits to 1.5 ns.

TABLE IB. SEP test limits. 1/ 2/

Device type	SEP	T_C = temperature ±10°C	V_{CC}	Effective LET
03	SEL	+25°C	5.5 V	≥ 93 MeV-cm^2/mg

1/ For SEP test conditions, see 4.4.4.2 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.

Device types	01, 03		02	
Case outlines	C, D, X	2	E	2
Terminal number	Terminal symbol			
1	1A	NC	1A	NC
2	1B	1A	1Y	V_{CC}
3	1Y	1B	2Y	2B
4	2A	1Y	GND	2A
5	2B	NC	GND	1B
6	2Y	2A	3Y	NC
7	GND	NC	4Y	1A
8	3Y	2B	4B	1Y
9	3B	2Y	4A	2Y
10	3A	GND	3B	GND
11	4Y	NC	3A	NC
12	4B	4Y	V_{CC}	GND
13	4A	4B	V_{CC}	3Y
14	V_{CC}	4A	2B	4Y
15	- - -	NC	2A	4B
16	- - -	3Y	1B	NC
17	- - -	NC	- - -	4A
18	- - -	3B	- - -	3B
19	- - -	3A	- - -	3A
20	- - -	V_{CC}	- - -	V_{CC}

NC = No connection.

Pin description	
Terminal symbol	Description
nA (n = 1 to 4)	Data inputs
nB (n = 1 to 4)	Data inputs
nY (n = 1 to 4)	Data outputs

FIGURE 1. Terminal connections.

Inputs		Outputs
nA	nB	nY
L	L	L
L	H	H
H	L	H
H	H	H

H = High voltage level
L = Low voltage level

FIGURE 2. Truth table.

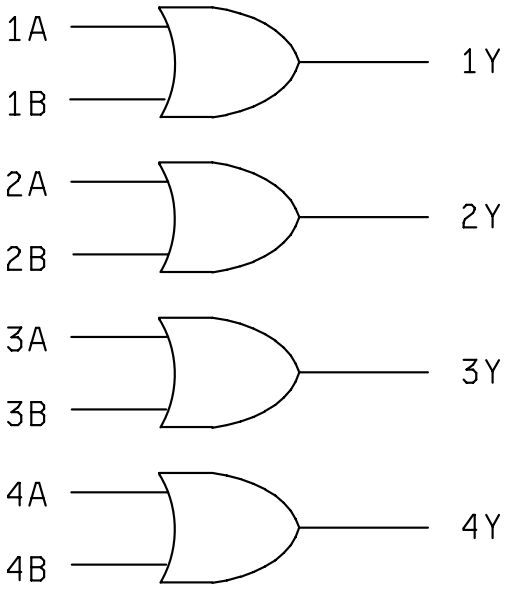
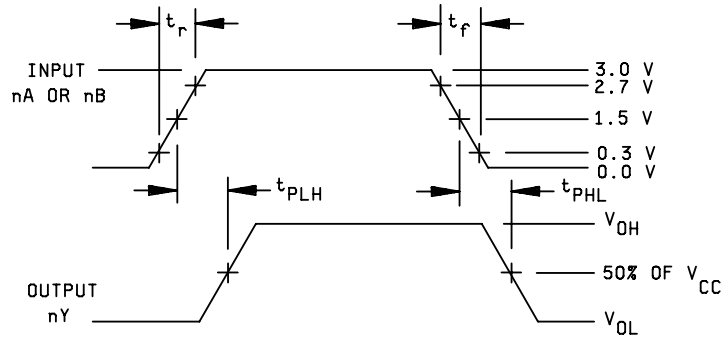
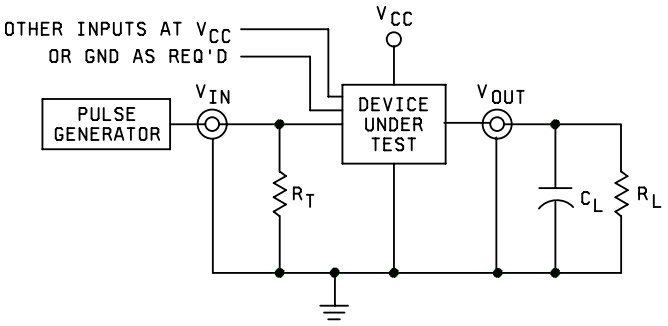


FIGURE 3. Logic diagram.





NOTES:

1. C_L = 50 pF (includes test jig and probe capacitance).
2. R_T = 50Ω or equivalent, R_L = 500Ω or equivalent.
3. Input signal from pulse generator: V_{IN} = 0.0 V to 3.0 V; PRR ≤ 10 MHz; Z_O = 50Ω, t_r ≤ 3.0 ns; t_f ≤ 3.0 ns; t_r and t_f shall be measured from 0.3 V to 2.7 V and from 2.7 V to 0.3 V, respectively; duty cycle = 50 percent.
4. Timing parameters shall be tested at a minimum input frequency of 1MHz.
5. The outputs are measured one at a time with one transition per measurement.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table IA)	Subgroups (in accordance with MIL-PRF-38535, table IIB)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	- - -	- - -	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9	1/ 1, 2, 3, 7, 8, 9	2/ 3/ 1, 2, 3, 7, 8, 9
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	3/ 1, 2, 3, 7,8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta limits shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, Delta parameters (+25°C).

Parameter 1/	Symbol	Device type	Delta limits
Quiescent supply current	I_{CCH}, I_{CCL}	01	±100 nA 2/
		03	±150 nA
Supply current delta	ΔI_{CC}	03	±0.4 mA
Input current low level	I_{IL}	03	±20 nA
Input current high level	I_{IH}	03	±20 nA
Output voltage low level (V_{CC} = 5.5 V, I_{OL} = 24 mA)	V_{OL}	03	±0.04 V
Output voltage high level (V_{CC} = 5.5 V, I_{OH} = -24 mA)	V_{OH}	03	±0.2 V

1/ These parameters shall be recorded before and after the required burn-in and life tests to determine the delta limits.

2/ This limit may not be production tested.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{PD} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and GND at a frequency of 1 MHz. C_{PD} shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. For C_{IN} and C_{PD}, test all applicable pins on five devices with zero failures.

d. Latch-up tests are required for device class V. These tests shall be performed only for initial qualification and after process or design changes that may affect the performance of the device. Latch-up tests shall be considered destructive. For latch-up tests, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the post irradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C +5°C, after exposure, to the subgroups specified in table IIA herein.

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883 method 1019, condition A and as specified herein. Prior to and during total dose irradiation characterization and testing, the devices for characterization shall be biased so that 50 percent are at inputs high and 50 percent are at inputs low, and the devices for testing shall be biased to the worst case condition established during characterization. Devices shall be biased as follows:

a. Device type 01:

(1) Inputs tested high, V_{CC} = 5.5 V dc +5%, R_{CC} = 10 Ω +20%, V_{IN} = 5.0 V dc +5%, R_{IN} = 1 kΩ +20%, and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc +5%, R_{CC} = 10 Ω +20%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ+20%, and all outputs are open.

b. Device type 03:

(1) Inputs tested high, V_{CC} = 5.5 V dc ±5%, V_{IN} = 5.0 V dc +10%, R_{IN} = 1 kΩ ±20%, and all outputs are open.

(2) Inputs tested low, V_{CC} = 5.5 V dc ±5%, V_{IN} = 0.0 V dc, R_{IN} = 1 kΩ ±20%, and all outputs are open.

4.4.4.1.1 Accelerated annealing test. Accelerated annealing tests shall be performed on all devices requiring a RHA level greater than 5k rads (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limit at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. 0° ≤ angle ≤ 60°). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be ≥ 100 errors or ≥ 10^7 ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be ≥ 20 microns in silicon.

e. The upset test temperature shall be +25°C and the latchup test temperature is maximum rated operating temperature ±10°C.

f. Bias conditions shall be defined by the manufacturer for latchup measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus (DSCC) when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , P.O. Box 3990, Columbus, Ohio 43218-3990, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA upset levels.

b. Test conditions (SEP).

c. Number of upsets (SEP).

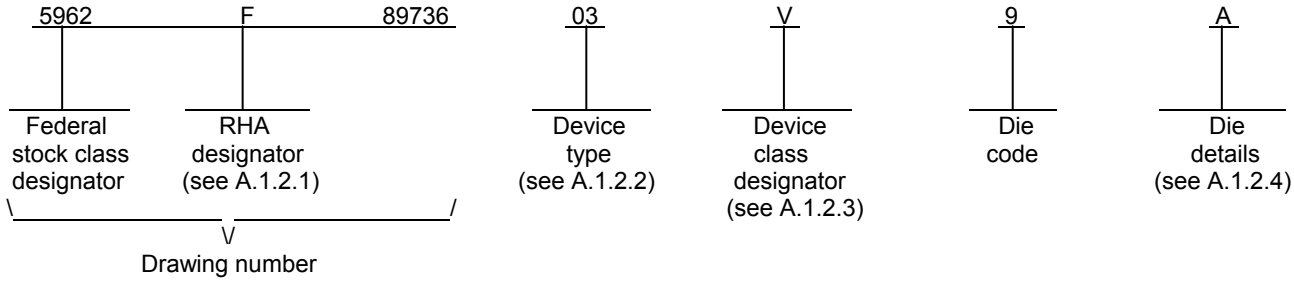
d. Number of transients (SEP).

e. Occurrence of latch-up (SEP).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardiness Assurance (RHA) levels are reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
03	54ACT32	Quad 2-input OR gate, TTL compatible inputs

A.1.2.3 Device class designator. Device class Q designator will not be included in the PIN and will not be marked on the device since the device class designator has been added after the original issuance of this drawing.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
03	A-1

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
03	A-1

A.1.2.4.3 Interface materials.

Die type	Figure number
03	A-1

A.1.2.4.4 Assembly related information.

Die type	Figure number
03	A-1

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2. APPLICABLE DOCUMENTS

A.2.1 Government specification, standards, and handbooks. The following specification, standard, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://assist.daps.dla.mil/quicksearch/ or http://assist.daps.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figure A-1.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figure A-1.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figure A-1.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figure A-1.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table II herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DSCC-VA, P.O. Box 3990, Columbus, Ohio, 43218-3990 or telephone (614) 692-0547.

A.6.3 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DSCC-VA and have agreed to this drawing.

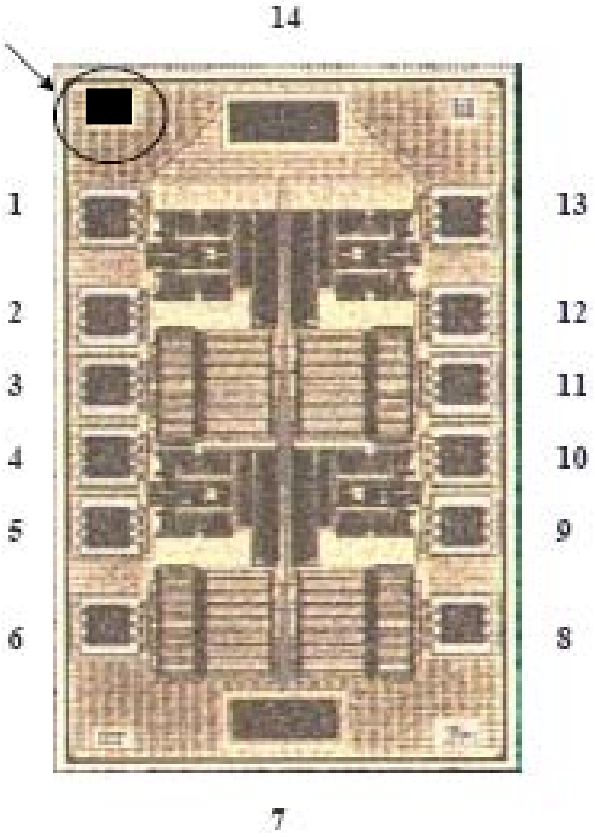
Die physical dimensions.

Die size: 1991 x 1281 μm

Die thickness: 285 ±25 μm

Die bonding pad locations and electrical functions.

Optional manufacturer's logo



Pad size: Pad numbers 1 to 6 and 8 to 13: 100 x 100 μm
Pad numbers 7 (GND) and 14 (V_{CC}): 100 x 280 μm

NOTE: Pad numbers reflect terminal numbers when placed in case outline X (see figure 1).

FIGURE A-1

Interface materials.

Top metallization:	Al Si Cu	0.85 μm
Backside metallization:	None	
Glassivation.		
Type:	P. Vapox + Nitride	
Thickness:	5000Å – 7000Å	
Substrate:	Silicon	

Assembly related information.

Substrate potential:	Floating or tied to GND
Special assembly instructions:	Bond pad #14 (V_{CC}) first

FIGURE A-1 – Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 07-09-13

Approved sources of supply for SMD 5962-89736 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DSCC maintains an online database of all current sources of supply at http://www.dscc.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor Similar PIN 2/
5962-8973601CA	27014 0C7V7	54ACTQ32DMQB
5962-8973601DA	0C7V7	54ACTQ32FMQB
5962-89736012A	27014 0C7V7	54ACTQ32LMQB
5962-8973602EA	3/	54ACT11032
5962-89736022A	3/	54ACT11032
5962R8973601VCA	27014	54ACTQ32JRQMLV
5962R8973601VDA	27014	54ACTQ32WRQMLV
5962R8973601V2A	3/	54ACTQ32ERQMV
5962-8973603XA	3/	54ACT32K02Q
5962-8973603VXA	3/	54ACT32K02V
5962F8973603CA	F8859	RHFACT32D04Q
5962F8973603CC	F8859	RHFACT32D03Q
5962F8973603VCA	F8859	RHFACT32D04V
5962F8973603VCC	F8859	RHFACT32D03V
5962F8973603VXC	F8859	RHFACT32K01V
5962F8973603XA	F8859	RHFACT32K02Q
5962F8973603VXA	F8859	RHFACT32K02V
5962F8973603XC	F8859	RHFACT32K01Q
5962F8973603V9A	F8859	ACT32DIE2V

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
F8859	ST Microelectronics 3 rue de Suisse BP4199 35041 RENNES cedex2 - FRANCE
0C7V7	QP Semiconductor 2945 Oakmead Village Court Santa Clara, CA 95051

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