HARRIS

HA-4902/883

January 1989

Precision Quad Comparator

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Fast Response Time (+25°C) ..... 215ns (Max) 180ns (Typ)**
- **Low Offset Voltage (+25°C) ..... 5mV (Max) 2mV (Typ)**
- **Low Input Sensitivity ..... 0.5mV (Max) 0.05mV (Typ)**
- **Low Offset Current (+25°C) ..... 35nA (Max) 10nA (Typ)**
- **Single or Dual-Voltage Supply Operation**
- **Selectable Output Logic Levels**
- **Active Pull-Up/Pull-Down Output Circuit — No External Resistors Required**

Applications

- **Threshold Detector**
- **Zero-Crossing Detector**
- **Window Detector**
- **Analog Interfaces for Microprocessors**
- **High Stability Oscillators**
- **Logic System Interface**

Description

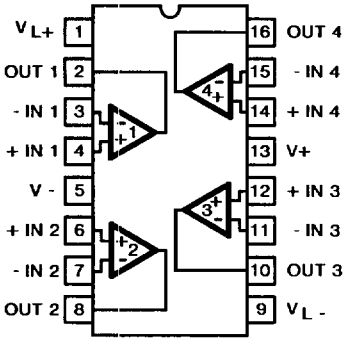
The HA-4902/883 is a monolithic, quad, precision comparator offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. This comparator can sense signals at ground level while being operated from either single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4902/883 contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC+} and V_{LOGIC-}) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4902/883 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

This comparator's combination of features makes it an ideal component for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface network.

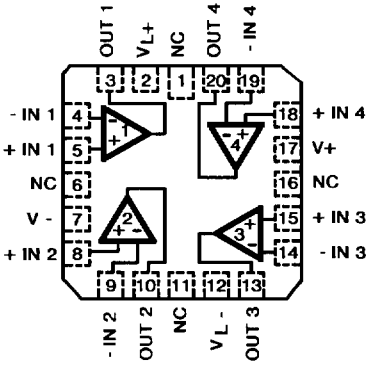
The HA-4902/883 is available in a 16 pin Ceramic DIP package and in a 20 pin Ceramic LCC package and is specified over the military, -55°C to +125°C, temperature range.

Pinouts

HA1-4902/883 (CERAMIC DIP)
TOP VIEW



HA4-4902/883 (CERAMIC LCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 33V
Differential Input Voltage ..... ±15V
Peak Output Current ..... ±50mA
Output Short Circuit Current Duration ..... Indefinite
(One Amplifier Shorted to GND)
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
ESD Rating ..... < 2000V
Lead Temperature (Soldering 10 sec) ..... +275°C

CAUTION: Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	76°C/W	17°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation at +75°C
Ceramic DIP Package 1.31W
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 13.1mW/°C
Ceramic LCC Package ..... 13.1mW/°C

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage ..... ±15V
Logic Supply Voltage (V_L+) ..... +5V
Logic Reference Voltage (V_L-) 0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = ±15V, V_L = 0V, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Input Offset Voltage	V_{IO}	V_{CM} = 0V, V_{OUT} = 1.4V See Note 3	1	+25°C	-5	5	mV
			2,3	+125°C, -55°C	-8	8	mV
Input Bias Current	$+I_B$	V_{CM} = 0V	1	+25°C	-150	150	nA
			2,3	+125°C, -55°C	-200	200	nA
	$-I_B$	V_{CM} = 0V	1	+25°C	-150	150	nA
			2,3	+125°C, -55°C	-200	200	nA
Input Offset Current	I_{IO}	V_{CM} = 0V	1	+25°C	-35	35	nA
			2,3	+125°C, -55°C	-45	45	nA
Input Sensitivity	IN_{SEN}	See Note 3	1	+25°C	-0.5	0.5	mV
			2,3	+125°C, -55°C	-0.6	0.6	mV
Output Voltage Levels	V_{OL}	I_{SINK} = 3mA	1	+25°C	-	0.4	V
			2,3	+125°C, -55°C	-	0.4	V
	V_{OH}	I_{SOURCE} = 3mA	1	+25°C	3.5	-	V
			2,3	+125°C, -55°C	3.5	-	V
Output Current	I_{SINK}	$V_{OUT} \leq 0.4V$	1	+25°C	3	-	mA
			2,3	+125°C, -55°C	3	-	mA
	I_{SOURCE}	$V_{OUT} \geq 3.5V$	1	+25°C	-	-3	mA
			2,3	+125°C, -55°C	-	-3	mA
Supply Current	$+I_{CC}$	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	20	mA
			2,3	+125°C, -55°C	-	20	mA
	$-I_{CC}$	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	8	mA
			2,3	+125°C, -55°C	-	10	mA
Logic Current	I_L	$V_{OUT} = V_{OL}, V_{OH}$	1	+25°C	-	6	mA
			2,3	+125°C, -55°C	-	8	mA

CAUTION: This device is sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

TABLE 2. A.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Table 2 Intentionally Left Blank. See A.C. Specifications on Table 3.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, V_L = GND, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Response Time	t_{pd0}	+100mV Input Step, 10mV Overdrive	1, 2	+25°C	-	200	ns
	t_{pd1}	-100mV Input Step, -10mV Overdrive	1, 2	+25°C	-	215	ns
Common Mode Range	+CMR		1	+25°C	-	12.4	V
	-CMR		1	+25°C	-15	-	V

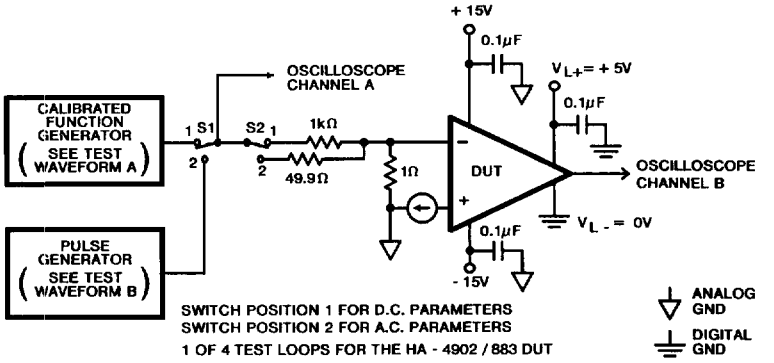
NOTES:
1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
2. F ≈ 100Hz, duty cycle ≈ 50%, inverting input driven, all unused inverting inputs tie to +5V.
3. Refer to enlarged area of test waveform A. Offset voltage is measured when V_{OUT} = 1.4V. Sensitivity is measured on the transition edge at 0.4V and 3.5V. Sensitivity is the change in differential input voltage required to change the output state. Sensitivity includes the effects of offset voltage, offset current, common mode rejection and voltage gain.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 2)
Interim Electrical Parameters (Pre Burn-in)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

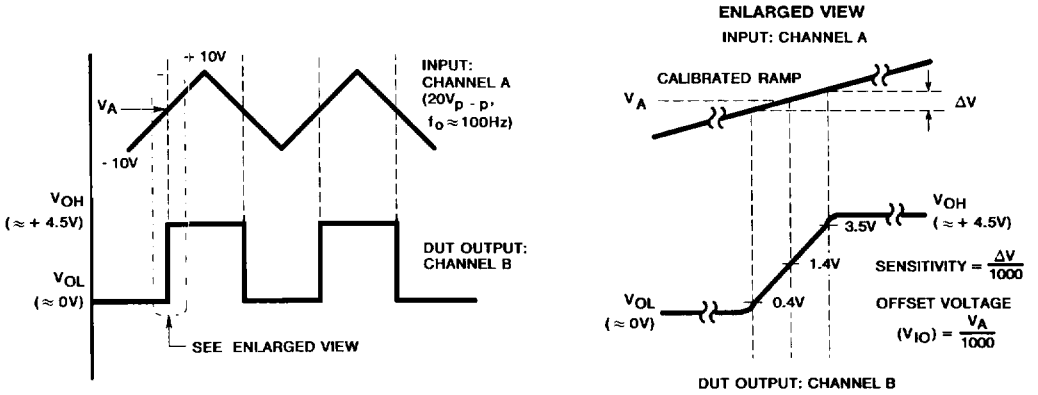
* PDA applies to Subgroup 1 only.

Test Circuit (Applies to Tables 1 and 3)

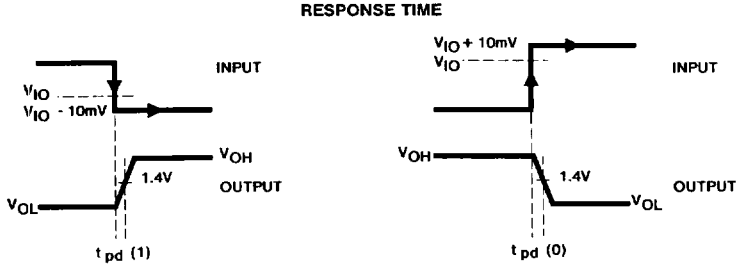


For Detailed Information, Refer to HA-4902/883 Test Tech Brief

Test Waveform A (Applies to Table 1)



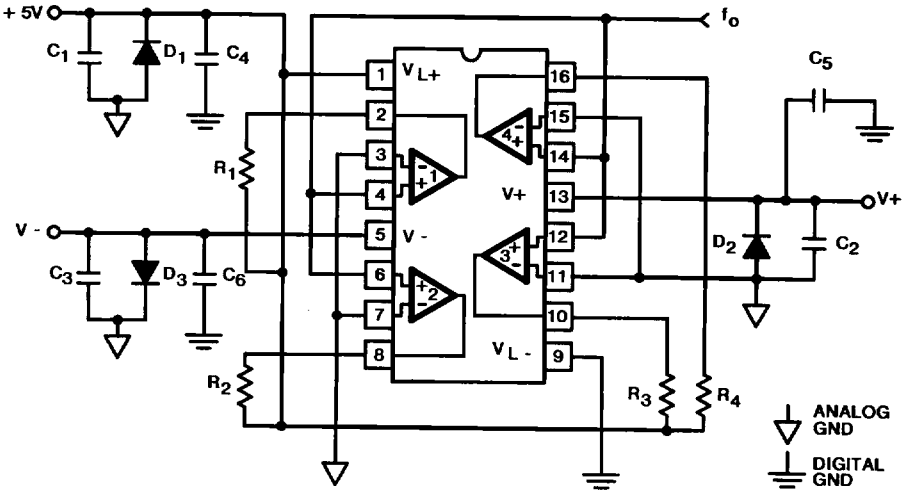
Test Waveform B (Applies to Table 3)



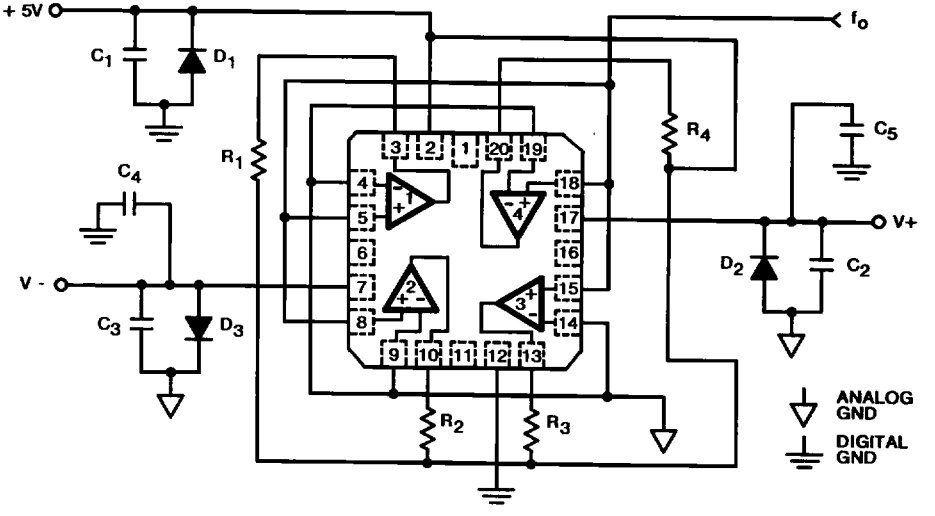
NOTE: Response time testing is done after V_{IO} testing to acquire the actual device offset voltage. 10mV overdrive is then added (or subtracted depending on state) to this measured V_{IO} value.

Burn-In Circuits

HA1-4902/883 CERAMIC DIP



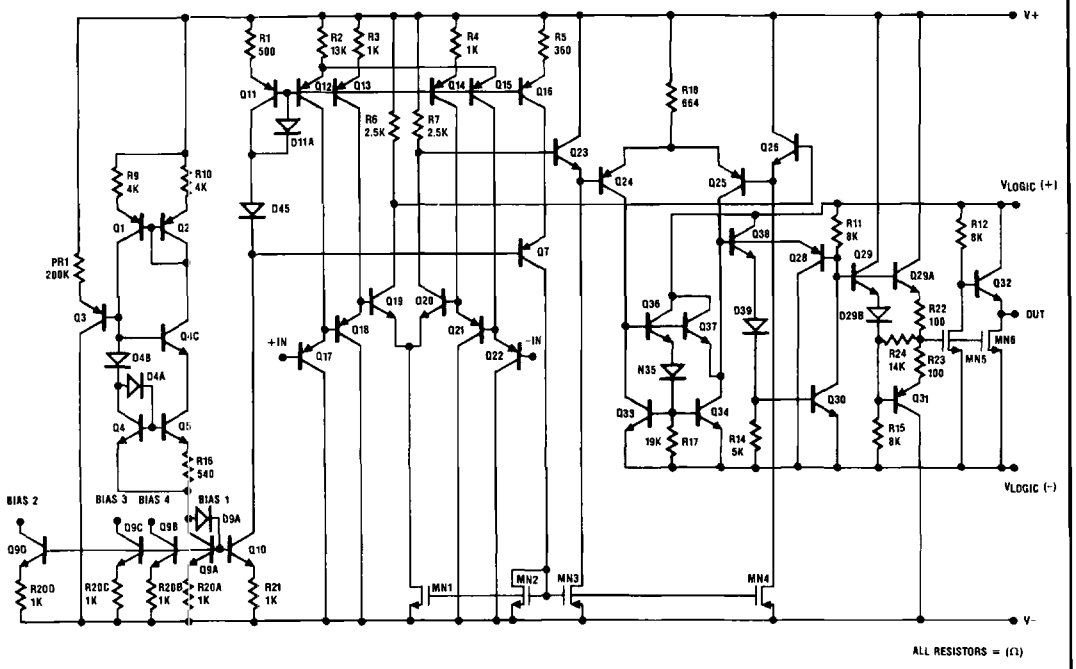
HA4-4902/883 CERAMIC LCC



NOTES:

R_1 = 5kΩ, ±5%
C_1 = C_2 = C_3 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
C_4 = C_5 = C_6 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
D_1 = D_2 = D_3 = IN4002 or Equivalent/Board
| (V+) - (V-) | = 30V
V_{L-} = 0V, V_{L+} = 5V
f_o = 5V (Static Burn-In)

Schematic Diagram (1/4 of HA-4902/883)



Die Characteristics

DIE DIMENSIONS:
95 x 105 x 19 mils
(2420 x 2670 x 483 µm)

METALLIZATION:
Type: Aluminum
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$0.4 \times 10^5 A/cm^2$

SUBSTRATE POTENTIAL (Powered Up): V-

GLASSIVATION:
Type: Nitride
Thickness: 7kÅ ± 0.7kÅ

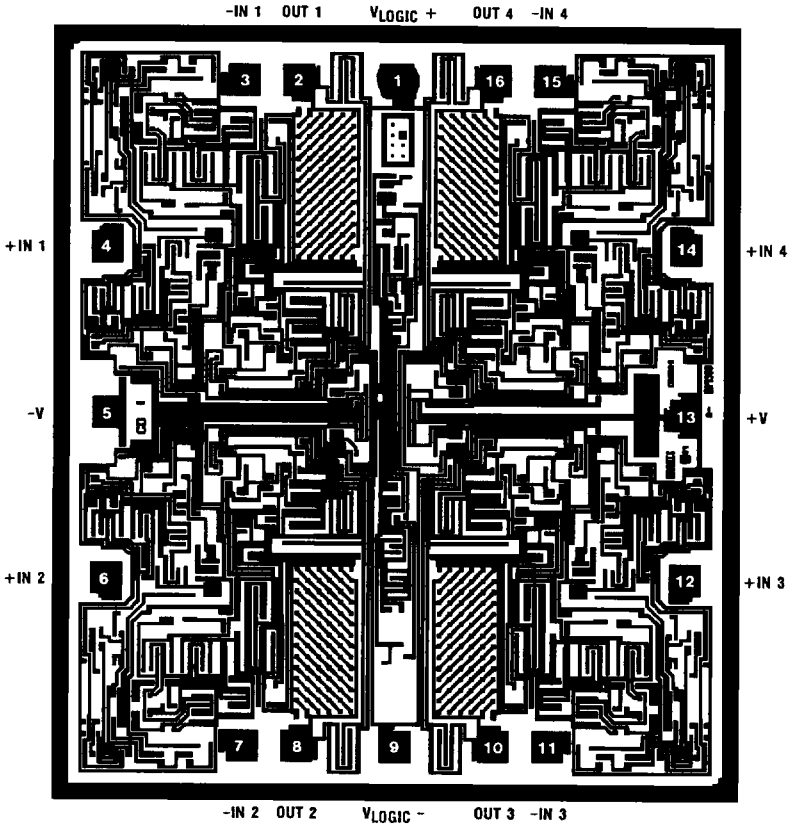
TRANSISTOR COUNT: 137

PROCESS: Combination of Std. Linear and MOS Dielectric Isolation

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

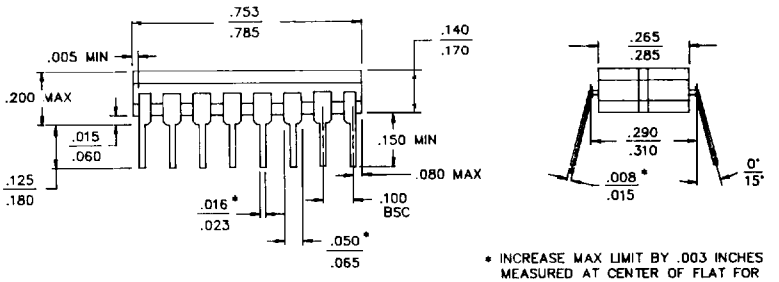
HA-4902/883



NOTE: Bond Pad Numbers Correspond to 16 Pin Ceramic DIP Only.

Packaging†

16 PIN CERAMIC DIP

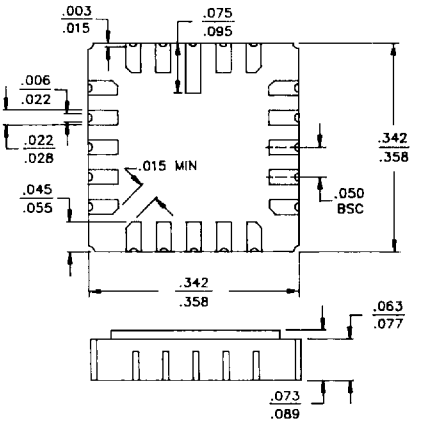


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-2

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

† Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

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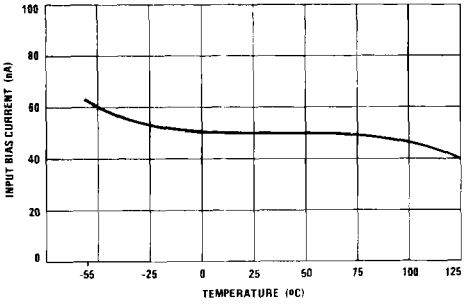
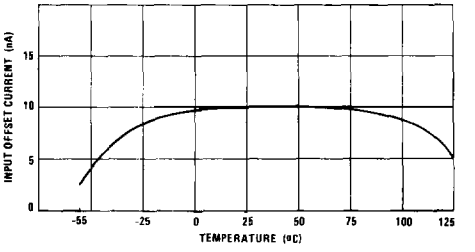
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$

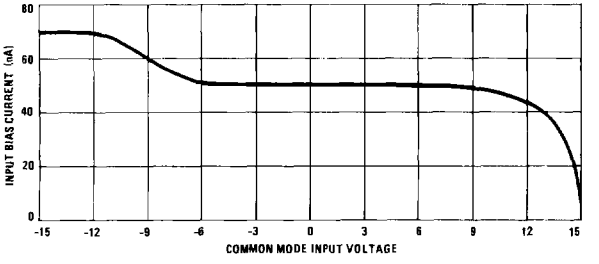
INPUT BIAS CURRENT vs. TEMPERATURE



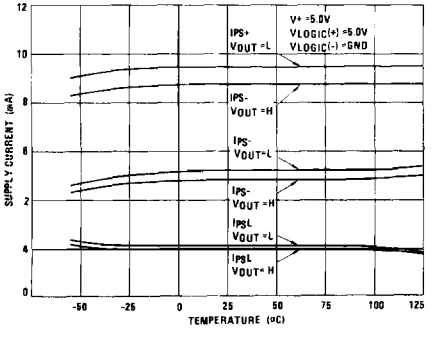
INPUT OFFSET CURRENT vs. TEMPERATURE



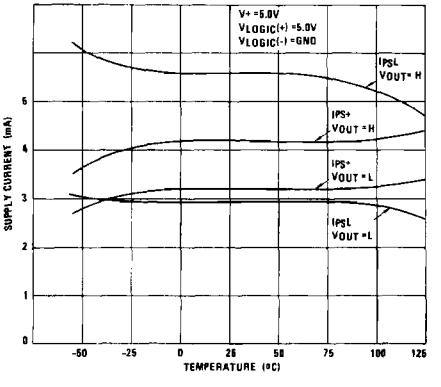
INPUT BIAS CURRENT vs. COMMON MODE INPUT VOLTAGE (V_{DIFF} = 0V)



SUPPLY CURRENT vs. TEMPERATURE FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY



SUPPLY CURRENT vs. TEMPERATURE FOR SINGLE +5V OPERATION



DESIGN INFORMATION (Continued)

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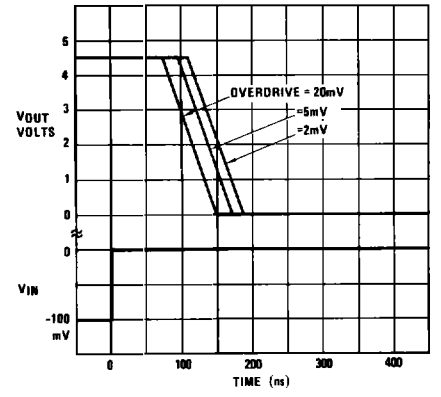
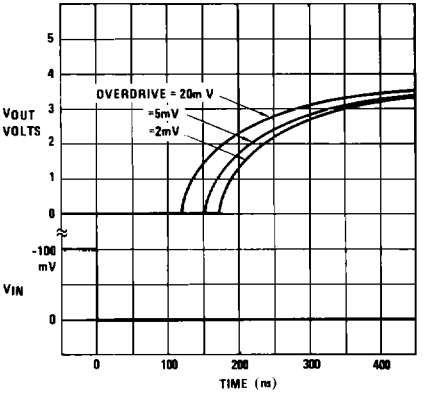
Typical Performance Curves Unless Otherwise Specified: $T_A = +25^oC$, $V_{SUPPLY} = \pm15V$, $V_{LOGIC}+ = 5V$, $V_{LOGIC}- = 0V$

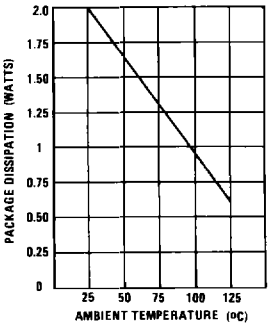
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



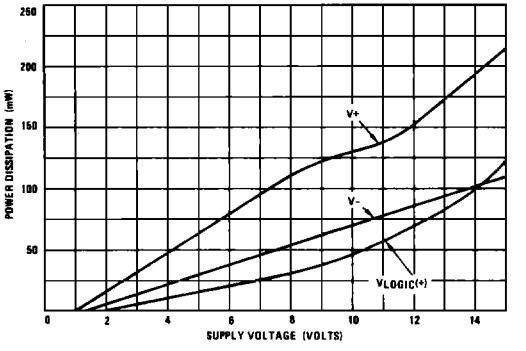
RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES



MAXIMUM PACKAGE DISSIPATION vs. $T_{AMBIENT}$



MAXIMUM POWER DISSIPATION vs. SUPPLY VOLTAGE
(No Load Condition)



NOTE: Total Power Dissipation (TPD) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs. Supply Voltages. The calculated TPD is then located on the graph of Maximum Allowable Package Dissipation vs. Ambient Temperature to determine ambient temperature operating limits imposed by the calculated TPD (See Performance Curves). For instance, the combination of ±15V, 5V, 0V (±V, V_{LOGIC} +, V_{LOGIC} −) gives a TPD of 350mW, the combination ±15V, 0V gives a TPD of 450mW.

DESIGN INFORMATION (Continued)

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TYPICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: Supply Voltage = ±15V, V_L+ = 5V, V_L- = 0V, Unless Otherwise Specified.

PARAMETERS	CONDITIONS	TEMP	TYPICAL	DESIGN LIMIT	UNITS
Offset Voltage	Note 3	Full	0.5	Table 1	mV
Input Bias Current		+25°C	50	Table 1	nA
		Full	90	Table 1	nA
Input Offset Current		+25°C	10	Table 1	nA
		Full	20	Table 1	nA
Input Sensitivity	Note 3	Full	50	Table 1	µV
Output Level	V_{OL}; I_{SINK} = 3mA	Full	0.15	Table 1	V
	V_{OH}; I_{SOURCE} = 3mA	Full	4.3	Table 1	V
Supply Current	$+I_{CC}$; $V_{OUT} = V_{OH}$	Full	10	Table 1	mA
	$+I_{CC}$; $V_{OUT} = V_{OL}$	Full	15	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OH}$	Full	-6	Table 1	mA
	$-I_{CC}$; $V_{OUT} = V_{OL}$	Full	-8	Table 1	mA
Logic Current	I_L; $V_{OUT} = V_{OH}$	Full	2	Table 1	mA
	I_L; $V_{OUT} = V_{OL}$	Full	4	Table 1	mA
Response Time	t_{pd0}	Full	150	Table 3	ns
	t_{pd1}	Full	150	Table 3	ns

Applying The HA-4902 Comparator

Supply Connections

This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range, while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{LOGIC} + and V_{LOGIC} -. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings ($15V_{p-p}$, max.) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to +15V), V+ and V_{LOGIC} + may be connected together to the positive supply while V- and V_{LOGIC} - are grounded. If an input signal could swing negative with respect to the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

Unused Inputs

Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter" ($V_{DIFF} \geq V_{IO}$). All unused inverting inputs may be tied to +5V and non-inverting inputs tied to ground.

Crosstalk

Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{IO}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

Power Supply Decoupling

Decouple all power supply lines with 0.01µF ceramic capacitors to a ground line located near the package to reduce coupling between channels or from external sources.

Response Time

Fast rise time (< 200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

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