

High Performance Schottky Rectifier, 2 x 3.5 A


D-PAK (TO-252AA)


FEATURES

- Popular D-PAK outline
- Center tap configuration
- Small foot print, surface mountable
- Low forward voltage drop
- High frequency operation
- Guard ring for enhanced ruggedness and long term reliability
- Meets MSL level 1, per J-STD-020, LF maximum peak of 260 °C
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912


RoHS
COMPLIANT

PRODUCT SUMMARY	
Package	D-PAK (TO-252AA)
$I_{F(AV)}$	2 x 3.5 A
V_R	30 V
V_F at I_F	See Electrical table
I_{RM}	50 mA at 125 °C
T_J max.	150 °C
Diode variation	Common cathode
E_{AS}	8 mJ

DESCRIPTION

The VS-6CWQ03FNPbF surface mount, center tap, Schottky rectifier series has been designed for applications requiring low forward drop and small foot prints on PC board. Typical applications are in disk drives, switching power supplies, converters, freewheeling diodes, battery charging, and reverse battery protection.

MAJOR RATINGS AND CHARACTERISTICS			
SYMBOL	CHARACTERISTICS	VALUES	UNITS
$I_{F(AV)}$	Rectangular waveform	7	A
V_{RRM}		30	V
I_{FSM}	$t_p = 5 \mu s$ sine	535	A
V_F	3 A_{pk} , $T_J = 125 \text{ °C}$ (per leg)	0.35	V
T_J	Range	-40 to +150	°C

VOLTAGE RATINGS			
PARAMETER	SYMBOL	VS-6CWQ03FNPbF	UNITS
Maximum DC reverse voltage	V_R	30	V
Maximum working peak reverse voltage	V_{RWM}		

ABSOLUTE MAXIMUM RATINGS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum average forward current See fig. 5	$I_{F(AV)}$	50 % duty cycle at $T_C = 134 \text{ °C}$, rectangular waveform		3.5	A
				7	
Maximum peak one cycle non-repetitive surge current per leg See fig. 7	I_{FSM}	5 μs sine or 3 μs rect. pulse	Following any rated load condition and with rated V_{RRM} applied	535	
		10 ms sine or 6 ms rect. pulse		90	
Non-repetitive avalanche energy per leg	E_{AS}	$T_J = 25 \text{ °C}$, $I_{AS} = 2 \text{ A}$, $L = 4 \text{ mH}$		8	mJ
Repetitive avalanche current per leg	I_{AR}	Current decaying linearly to zero in 1 μs Frequency limited by T_J maximum $V_A = 1.5 \times V_R$ typical		1	A



ELECTRICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum forward voltage drop per leg See fig. 1	V _{FM} ⁽¹⁾	3 A	T _J = 25 °C	0.45	V
		6 A		0.52	
		3 A	T _J = 125 °C	0.35	
		6 A		0.46	
Maximum reverse leakage current per leg See fig. 2	I _{RM} ⁽¹⁾	T _J = 25 °C	V _R = Rated V _R	2	mA
		T _J = 125 °C		50	
Threshold voltage	V _{F(TO)}	T _J = T _J maximum		0.22	V
Forward slope resistance	r _t			32.86	mΩ
Typical junction capacitance per leg	C _T	V _R = 5 V _{DC} , (test signal range 100 kHz to 1 MHz), 25 °C		290	pF
Typical series inductance per leg	L _S	Measured lead to lead 5 mm from package body		5.0	nH
Maximum voltage rate of change	dV/dt	Rated V _R		10 000	V/μs

Note

(1) Pulse width < 300 μs, duty cycle < 2 %

THERMAL - MECHANICAL SPECIFICATIONS					
PARAMETER	SYMBOL	TEST CONDITIONS		VALUES	UNITS
Maximum junction and storage temperature range	T _J ⁽¹⁾ , T _{Stg}			-40 to +150	°C
Maximum thermal resistance, junction to case	R _{thJC}	DC operation See fig. 4	per leg	4.7	°C/W
			per device	2.35	
Approximate weight				0.3	g
				0.01	oz.
Marking device		Case style D-PAK (similar to TO-252AA)		6CWQ03FN	

Note

(1) $\frac{dP_{tot}}{dT_J} < \frac{1}{R_{thJA}}$ thermal runaway condition for a diode on its own heatsink

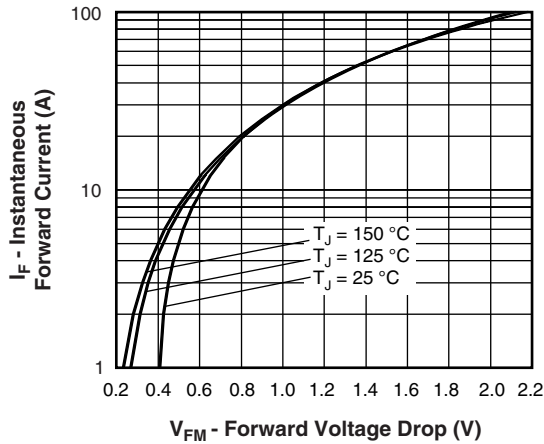


Fig. 1 - Maximum Forward Voltage Drop Characteristics (Per Leg)

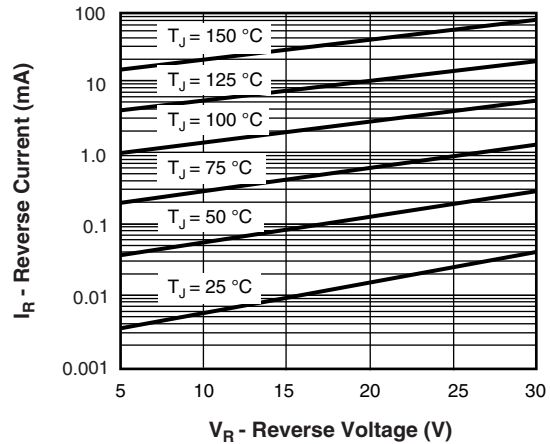


Fig. 2 - Typical Values of Reverse Current vs. Reverse Voltage (Per Leg)

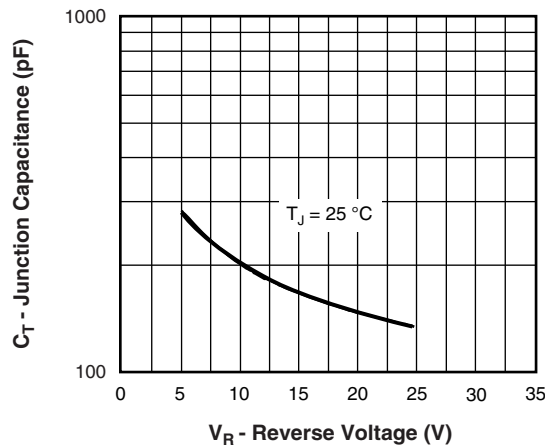


Fig. 3 - Typical Junction Capacitance vs. Reverse Voltage (Per Leg)

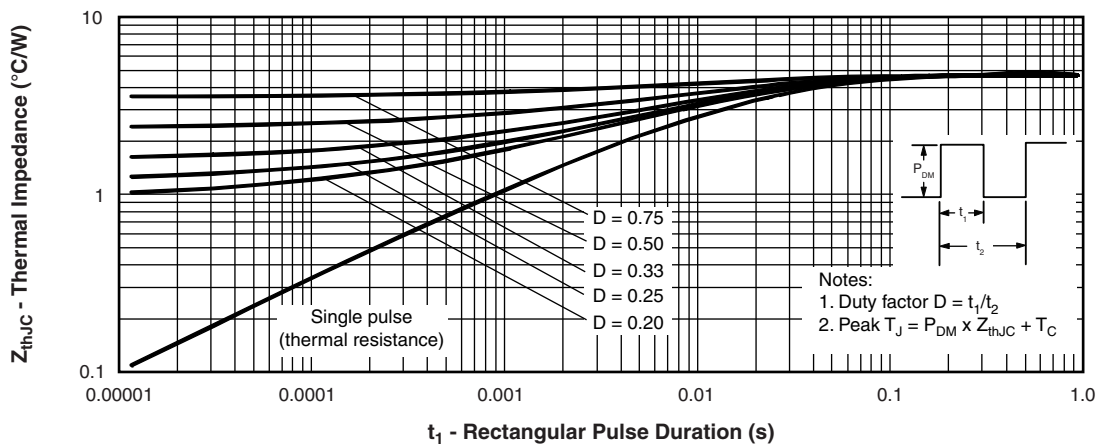


Fig. 4 - Maximum Thermal Impedance Z_{thJC} Characteristics (Per Leg)

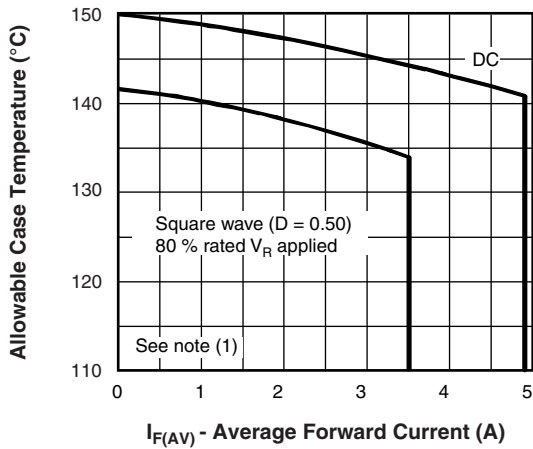


Fig. 5 - Maximum Allowable Case Temperature vs. Average Forward Current (Per Leg)

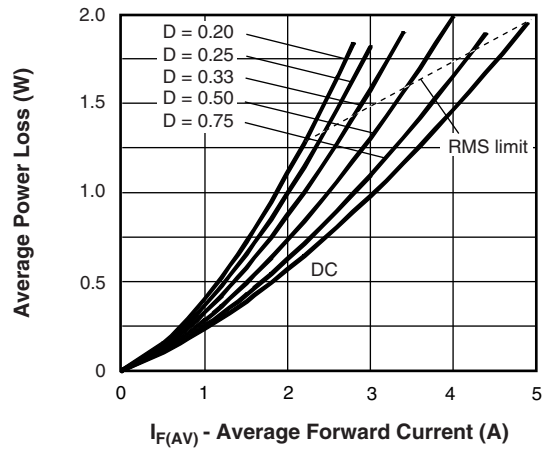


Fig. 6 - Forward Power Loss Characteristics (Per Leg)

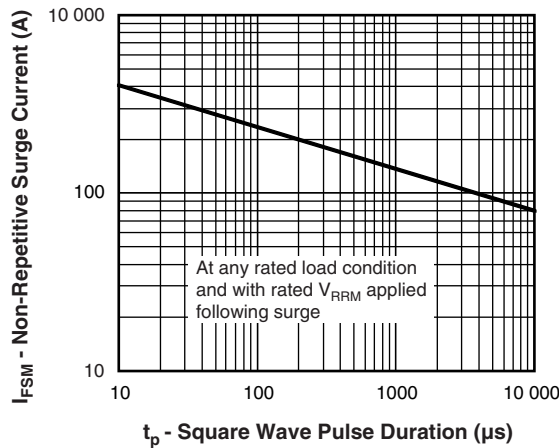


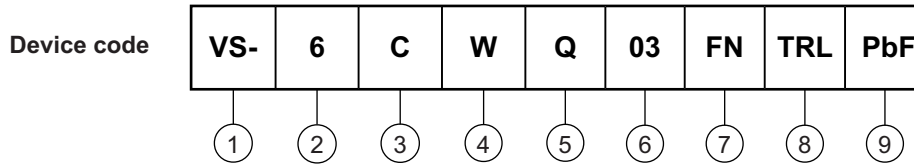
Fig. 7 - Maximum Non-Repetitive Surge Current (Per Leg)

Note

- (1) Formula used: $T_C = T_J - (P_d + P_{d_{REV}}) \times R_{thJC}$;
 P_d = forward power loss = $I_{F(AV)} \times V_{FM}$ at $(I_{F(AV)}/D)$ (see fig. 6);
 $P_{d_{REV}}$ = inverse power loss = $V_{R1} \times I_R (1 - D)$; I_R at $V_{R1} = 80\%$ rated V_R



ORDERING INFORMATION TABLE



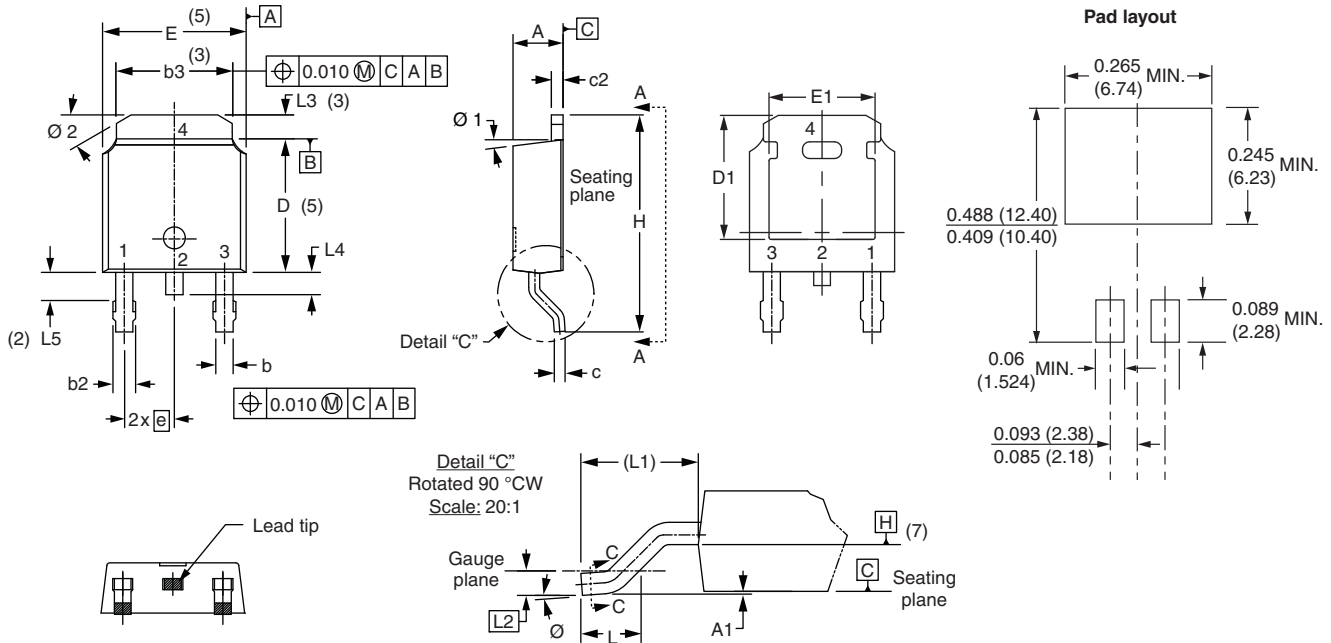
- 1** - Vishay Semiconductors product
- 2** - Current rating (7 A)
- 3** - Center tap configuration
- 4** - Package identifier:
W = D-PAK
- 5** - Schottky "Q" series
- 6** - Voltage rating (03 = 30 V)
- 7** - FN = TO-252AA (D-PAK)
- 8** -
 - None = tube (50 pieces)
 - TR = tape and reel
 - TRL = tape and reel (left oriented)
 - TRR = tape and reel (right oriented)
- 9** - PbF = lead (Pb)-free

LINKS TO RELATED DOCUMENTS	
Dimensions	www.vishay.com/doc?95016
Part marking information	www.vishay.com/doc?95059
Packaging information	www.vishay.com/doc?95033
SPIICE model	www.vishay.com/doc?95437



D-PAK (TO-252AA)

DIMENSIONS in millimeters and inches



SYMBOL	MILLIMETERS		INCHES		NOTES	SYMBOL	MILLIMETERS		INCHES		NOTES
	MIN.	MAX.	MIN.	MAX.			MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	0.094		e	2.29 BSC		0.090 BSC		
A1	-	0.13	-	0.005		H	9.40	10.41	0.370	0.410	
b	0.64	0.89	0.025	0.035		L	1.40	1.78	0.055	0.070	
b2	0.76	1.14	0.030	0.045		L1	2.74 BSC		0.108 REF.		
b3	4.95	5.46	0.195	0.215	3	L2	0.51 BSC		0.020 BSC		
c	0.46	0.61	0.018	0.024		L3	0.89	1.27	0.035	0.050	3
c2	0.46	0.89	0.018	0.035		L4	-	1.02	-	0.040	
D	5.97	6.22	0.235	0.245	5	L5	1.14	1.52	0.045	0.060	2
D1	5.21	-	0.205	-	3	∅	0°	10°	0°	10°	
E	6.35	6.73	0.250	0.265	5	∅1	0°	15°	0°	15°	
E1	4.32	-	0.170	-	3	∅2	25°	35°	25°	35°	

Notes

- (1) Dimensioning and tolerancing as per ASME Y14.5M-1994
- (2) Lead dimension uncontrolled in L5
- (3) Dimension D1, E1, L3 and b3 establish a minimum mounting surface for thermal pad
- (4) Section C - C dimension apply to the flat section of the lead between 0.13 and 0.25 mm (0.005 and 0.10") from the lead tip
- (5) Dimension D, and E do not include mold flash. Mold flash shall not exceed 0.127 mm (0.005") per side. These dimensions are measured at the outermost extremes of the plastic body
- (6) Dimension b1 and c1 applied to base metal only
- (7) Datum A and B to be determined at datum plane H
- (8) Outline conforms to JEDEC outline TO-252AA



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