Clock OSC

SG7050CAN

Product name SG7050CAN 29.491200 MHz TJGA Product Number / Ordering code X1G0044810056xx

Please refer to the 8.Packing information about xx (last 2 digits)

Output waveform CMOS

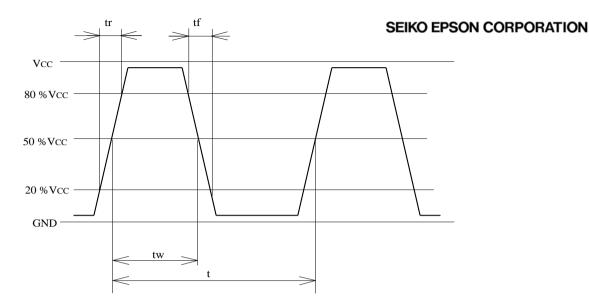
Pb free / Complies with EU RoHS directive

Reference weight Typ. 147 mg

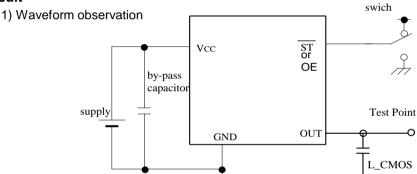
1.Absolute maximum ratings									
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks			
Maximum supply voltage	Vcc-GND	-0.3	-	4	V	-			
Storage temperature	T_stg	-40	-	+125	٥C	Storage as single product			
Input voltage	Vin	-0.3	-	Vcc+0.3	V	ST terminal			

2.Specifications(characteristics)									
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions / Remarks			
Output frequency	f0		29.4912		MHz				
Supply voltage	Vcc	1.6	-	3.63	V	-			
Operating temperature	T_use	-40	-	+85	٥C	-			
Frequency tolerance	f_tol	-50	-	50	x10 ⁻⁶	T_use			
Current consumption	Icc	-	-	3	mA	No load condition			
Stand-by current	I_std	-	-	2.7	μΑ	ST = GND			
Disable current	l_dis	-	-	-	mA	-			
Symmetry	SYM	45	-	55	%	50% Vcc Level L_CMOS=<15pF			
Output voltage	V _{OH}	Vcc-0.4	-	-		-			
	V_{OL}	-	-	0.4		-			
Output load condition	L_CMOS	-	-	15	pF	CMOS Load			
Input voltage	V_{IH}	0.8Vcc	-	-		ST terminal			
	V_{IL}	-	-	0.2Vcc		ST terminal			
Rise time	t _r	-	-	4	ns	Vcc1.6V : 0.2Vcc to 0.8Vcc Level, L_CMOS=15pF			
Fall time	tf	-	-	4	ns	Vcc1.6V : 0.2Vcc to 0.8Vcc Level, L_CMOS=15pF			
Start-up time	t str	-	-	3	ms	t = 0 at 0.9Vcc			
Jitter	t _{DJ}	-	0	-	ps	Deterministic Jitter Vcc=3.3V			
	t _{RJ}	-	2.4	-	ps	Random Jitter Vcc=3.3V			
	t _{RMS}	-	2.3	-	ps	δ(RMS of total distribution) Vcc=3.3V			
	t _{p-p}	-	20	-	ps	Peak to Peak Vcc=3.3V			
	t _{acc}	-	2.5	-	ps	Accumulated Jitter(δ) n=2 to 50000 cycles, Vcc=3.3V			
Phase jitter	t _{PJ}	-	0.34	-	ps	Off set Frequency: 12kHz to 20MHz, Vcc=3.3V			
Phase noise	L(f)	-	-	-	dBc/Hz	-			
	, i	-	-94	-	dBc/Hz	Off set 10Hz Vcc=3.3V			
		-	-123	-	dBc/Hz	Off set 100Hz Vcc=3.3V			
		-	-145	-	dBc/Hz	Off set 1kHz Vcc=3.3V			
		-	-155	-	dBc/Hz	Off set 10kHz Vcc=3.3V			
		-	-158	-	dBc/Hz	Off set 100kHz Vcc=3.3V			
		-	-159	-	dBc/Hz	Off set 1MHz Vcc=3.3V			
Frequency aging	f_age	-3	-	3	x10 ⁻⁶	@+25°C first year			
	90	_	_	-		<u>_</u>			

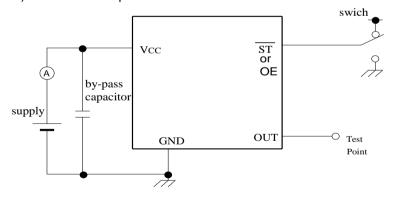
3.Timing chart



4.Test circuit



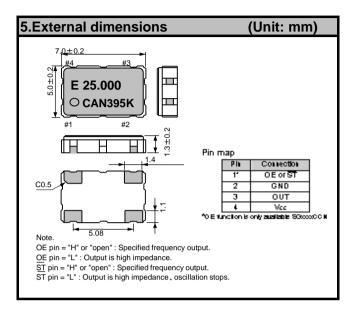
2) Current consumption

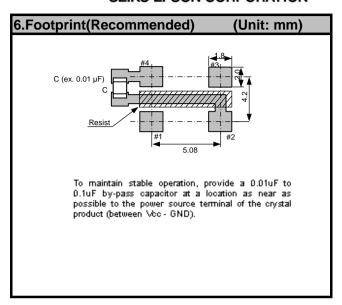


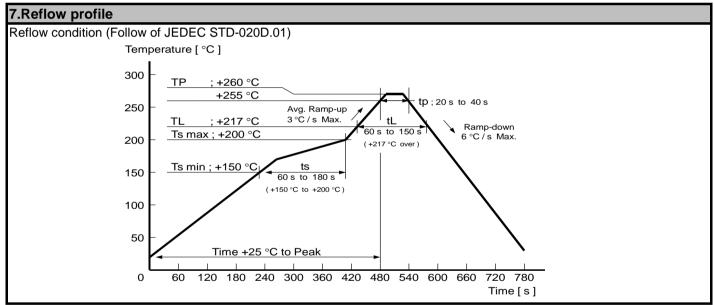
*Current consumption under the disable function should be = GND.

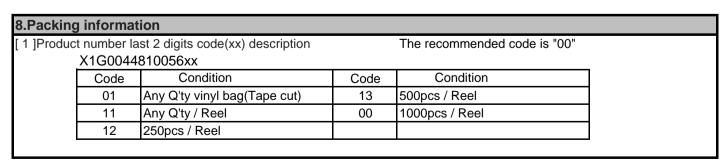
- 3) Condition
- (1) Oscilloscope
- · Band width should be minimum 5 times higher (wider) than measurement frequency.
- · Probe earth should be placed closely from test point and lead length should be as short as possible
- * Recommendable to use miniature socket. (Don't use earth lead.)
- (2) L_CMOS also includes probe capacitance.
- (3) By-pass capacitor (0.01 µF to 0.1 µF) is placed closely between VCC and GND.
- (4) Use the current meter whose internal impedance value is small.
- (5) Power supply
- \cdot Start up time (0 %VCC to 90 %VCC) of power source should be more than 150 μs .
- · Impedance of power supply should be as lowest as possible.

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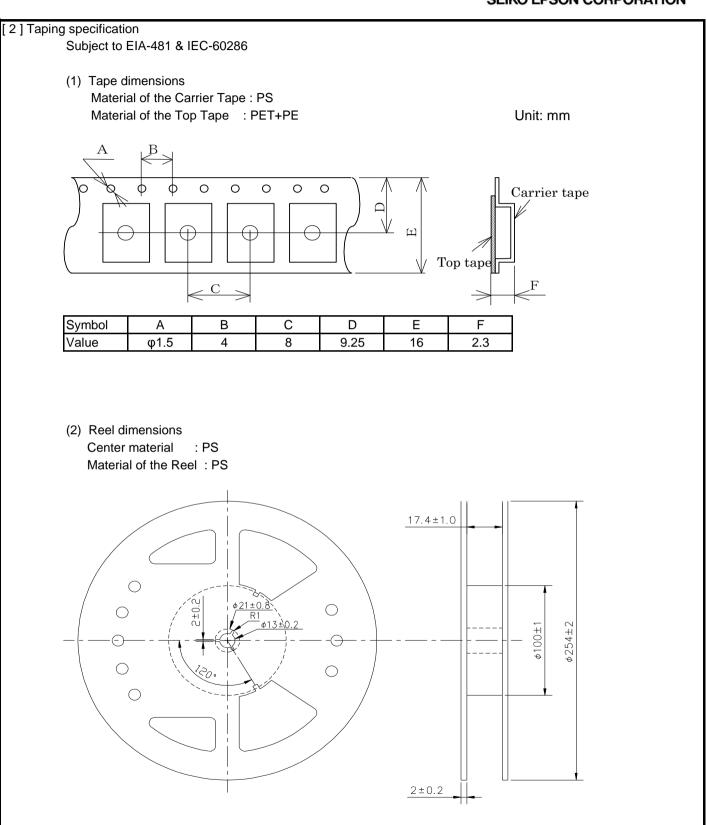








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