SC338(A)
Ultra Low Output Voltage Dual Linear FET Controller

Description

The SC338(A) is an ultra low output voltage dual power supply controller designed to simplify power management for notebook PCs. It is part of Semtech's Smart LDO™ family of products. The SC338(A) has two user adjustable outputs that can be set anywhere between 0.5V and 3.3V (V_{IN} = 12V, anywhere between 0.5V and 1.8V for V_{IN} = 5V) using two external resistors per output.

SC338(A) features for each output include tight output voltage regulation (±2.5% over -40°C to +85°C for SC338, ±1.5% over 0°C to +85°C for SC338A), enable controls, open drain power good signals, under-voltage protection and soft start. The enable pins allow the part to enter a very low power standby mode. Pulling them high enables the outputs. The power good pins are open drain and assert low when the voltage at their respective adjust pins is below 88% (typ.) of nominal. If the voltage at the adjust pin is below 50% (typ.) of nominal, the under voltage protection circuitry will shut down that output. The SC338(A) is available in an MSOP-10 surface mount package.

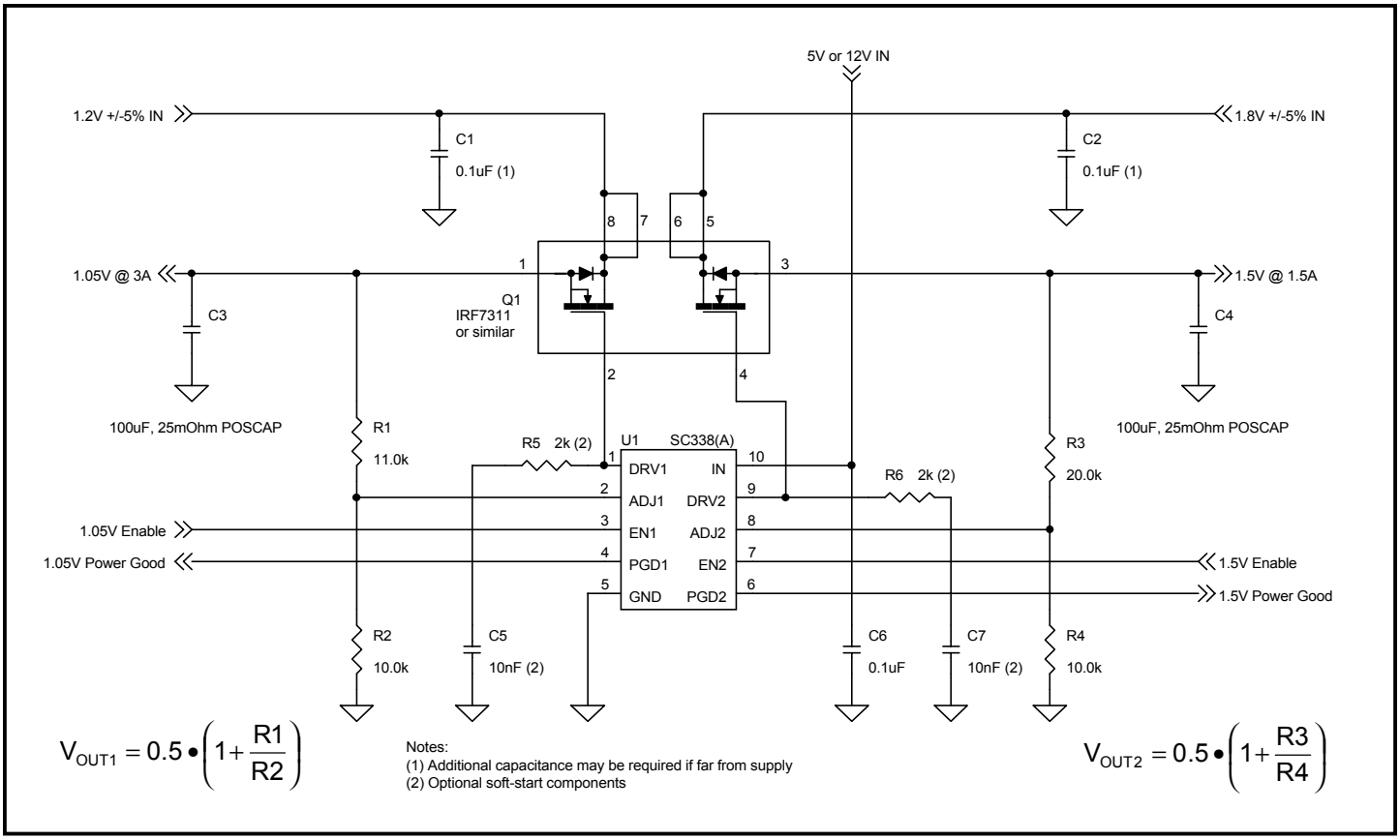
Features

- ±1.5% and ±2.5% reference voltage options available
- Two independant and fully adjustable outputs
- Wide supply voltage range permits operation from 5V or 12V rails
- Very low quiescent current (500µA typical with both outputs enabled and 5V input)
- Indivdual Enable control for each output
- Individual Power Good monitoring and signalling for each output
- Gate drives from input supply enable use of N-channel MOSFETs
- User selectable dropout voltage
- Individual under-voltage protection for each output
- MSOP-10 surface mount package

Applications

- Notebook PCs
- Simple dual power supplies

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied. Exposure to Absolute Maximum rated conditions for extended periods of time may affect device reliability.

Parameter	Symbol	Maximum	Units
Input Supply Voltage	V_{IN}	-0.3 to +13.2	V
Drive Pins	V_{DRV}	-0.3 to +8.0	V
Adjust and Power Good Pins	V_{ADJ}, V_{PGD}	-0.3 to +5.5 (1)	V
Enable Pins	V_{EN}	-0.3 to V_{IN}	V
Thermal Impedance Junction to Ambient	θ_{JA}	113	°C/W
Thermal Impedance Junction to Case	θ_{JC}	42	°C/W
Operating Ambient Temperature Range	T_A	-40 to +85	°C
Operating Junction Temperature Range	T_J	-40 to +125	°C
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C
ESD Rating (Human Body Model)	V_{ESD}	2	kV

Note:
(1) Or V_{IN}, if V_{IN} = 5V.

Electrical Characteristics

Unless specified: T_A = 25°C, V_{IN} = V_{EN} = 5V ± 5%, V_{PWR} (1) = 1.5V ± 5%, 0A ≤ I_{OUT} ≤ 3A.
Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
IN						
Supply Voltage	V_{IN}		**4.5**		**13.2**	V
Quiescent Current	I_Q	V_{IN} = 5V		500	**700**	µA
		V_{IN} = 12V		600	**900**	µA
Standby Current	$I_{Q(OFF)}$	Both EN low		0.1	**1.0**	µA
		Both EN low, V_{IN} = 12V			**15.0**	
Undervoltage Lockout						
Start Threshold	V_{UVLO}	V_{IN} rising		3.75		V
Hysteresis	V_{HYST}	V_{IN} falling		0.50		V
EN						
Enable Input Threshold	V_{IH}	Output on	**1.3**			V
	V_{IL}	Output off			**0.7**	

Electrical Characteristics (Cont.)

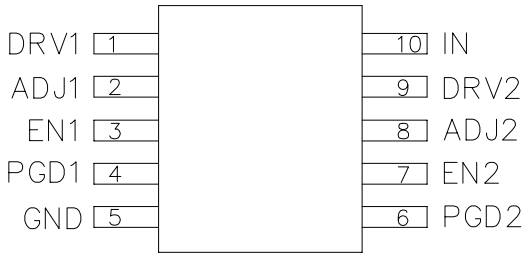
Unless specified: T_A = 25°C, V_{IN} = V_{EN} = 5V ± 5%, V_{PWR}[1] = 1.5V ± 5%, 0A ≤ I_{OUT} ≤ 3A.
Values in **bold** apply over full operating ambient temperature range.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
EN (Cont.)						
Enable Input Bias Current	I_{EN}	V_{EN} = 0V		0		µA
		V_{IN} = V_{EN} = 5V or 12V	**-1**		**+1**	
ADJ						
Adjust Input Bias Current	I_{ADJ}	V_{ADJ} = 0.5V	**-100**	0	**+100**	nA
Reference Voltage	V_{ADJ}		**-2.5%**	0.500	**+2.5%**	V
		SC338A only: 0°C ≤ T_A ≤ +85°C	**-1.5%**		**+1.5%**	
DRV						
Output Current	I_{DRV}	Sourcing, startup (until $V_{TH(PGD)}$ is reached)		10		µA
		Sourcing, after startup	**0.7**	2.0		mA
		Sinking	**400**	750		µA
Output Voltage	V_{DRV}	Full On, I_{DRV} = 0mA, V_{IN} = 12V	**6.6**	6.9		V
		Full On, I_{DRV} = 0mA, V_{IN} = 5V	**4.70**	4.85		
Under Voltage Protection						
Trip Threshold [2]	$V_{TH(UV)}$	Measured at ADJ pin	**40**	50	**60**	%V_{ADJ}
PGD						
Power Good Threshold [3]	$V_{TH(PGD)}$	Measured at ADJ pin	**-15**	-12	**-9**	%V_{ADJ}
Output Logic Low Voltage	V_{PGD}	V_{ADJ} = 0.4V, I_{PGD} = -1mA			**0.4**	V
Power Good Leakage Current	I_{PGD}	V_{ADJ} = 0.5V, 0V ≤ V_{PGD} ≤ V_{IN}	**-1**	0	**+1**	µA
Soft Start						
Output Rise Time 10% V_{OUT} to 90% V_{OUT}, V_{OUT} = 1.05V	t_r	$C_{DRV-GND}$ = not placed		150		µs
		$C_{DRV-GND}$ = 10nF		850		

Notes:
(1) V_{PWR} = input voltage to pass device drains (or sources depending upon orientation of FETs).
(2) If $V_{TH(UV)}$ is exceeded for longer than 50µs (nom.) the protection circuitry will shut down that output.
(3) During startup only, $V_{TH(PGD)}$ is -6% (typ.), then switches to -12% (typ.).

Pin Configuration

Top View



(MSOP-10)

Ordering Information

Part Number[1]	Output Voltage[2]	Package
SC338IMSTR[3]	Both outputs adjustable from 0.5V to 3.3V	MSOP-10
SC338IMSTRT[3][5]		
SC338AIMSTR[4]		
SC338AIMSTRT[4][5]		

Notes:

(1) Only available in tape and reel packaging. A reel contains 2500 devices.

(2) V_{IN} = 12V (0.5V to 1.8V for V_{IN} = 5V).

(3) V_{ADJ} is ±2.5% over -40°C ≤ T_A ≤ +85°C.

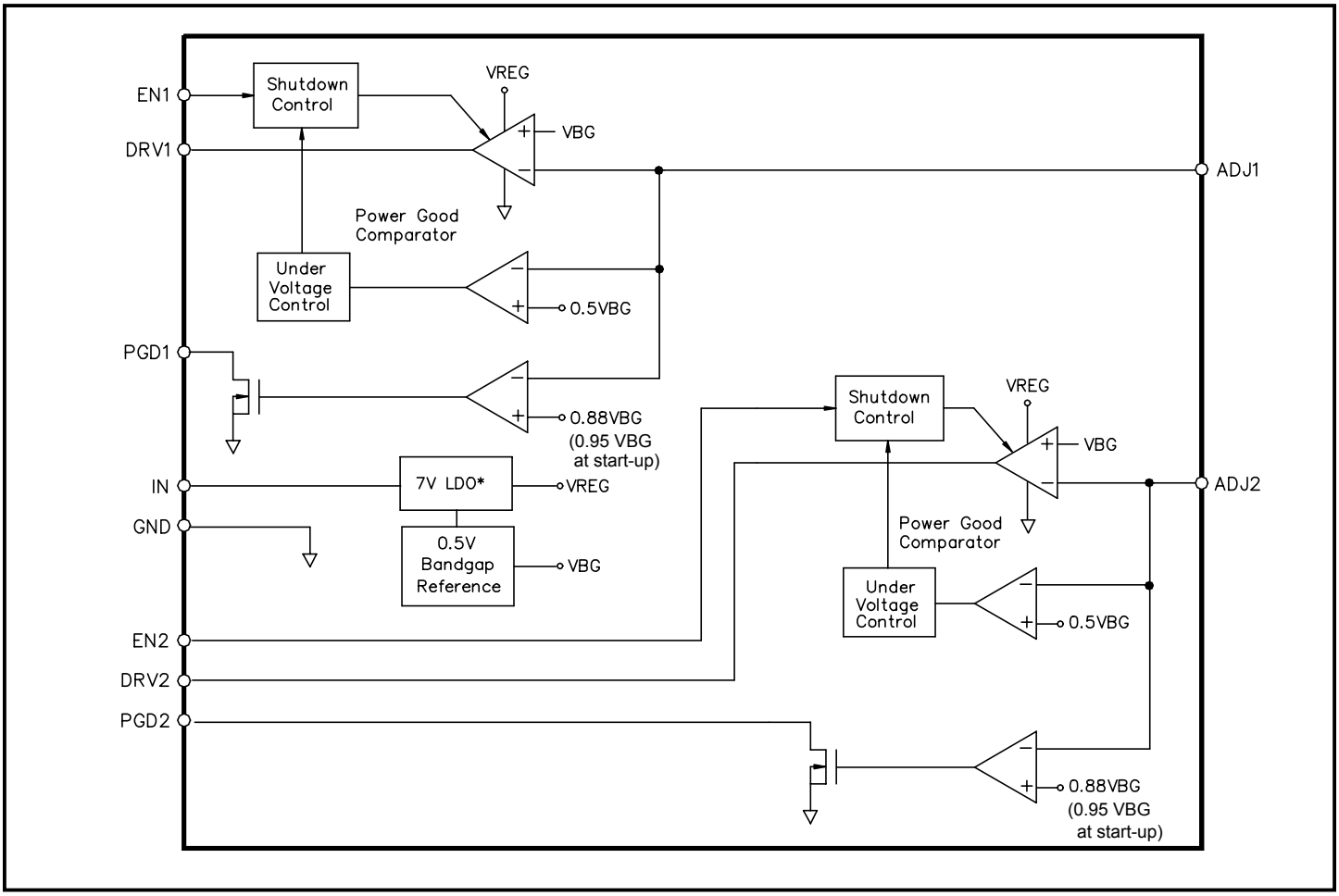
(4) V_{ADJ} is ±1.5% over 0°C ≤ T_A ≤ +85°C.

(5) Lead free product. This product is fully WEEE and RoHS compliant.

Pin Descriptions

Pin	Pin Name	Pin Function
1	DRV1	Output of regulator #1. Drives the gate of an N-channel MOSFET to maintain V_{OUT1} set by R1 and R2.
2	ADJ1	Regulator #1 sense input. Used for sensing the output voltage for power good and under-voltage, and to set the output voltage as follows (refer to application circuit on page 1): $V_{OUT1} = 0.5 \bullet \left(1 + \frac{R1}{R2}\right)$ $V_{OUT(MAX)}$ = 3.3V for V_{IN} = 12V, 1.8V for V_{IN} = 5V.
3	EN1	Active high enable control. Connect to IN if not being used. Do not allow to float.
4	PGD1	Power good signal output for V_{OUT1}. Open drain output pulls low when V_{OUT1} is below ($V_{OUT1(NOM)}$ -12%).
5	GND	Ground.
6	PGD2	Power good signal output for V_{OUT2}. Open drain output pulls low when V_{OUT2} is below ($V_{OUT2(NOM)}$ -12%).
7	EN2	Active high enable control. Connect to IN if not being used. Do not allow to float.
8	ADJ2	Regulator #2 sense input. Used for sensing the output voltage for power good and under-voltage, and to set the output voltage as follows (refer to application circuit on page 1): $V_{OUT2} = 0.5 \bullet \left(1 + \frac{R3}{R4}\right)$ $V_{OUT(MAX)}$ = 3.3V for V_{IN} = 12V, 1.8V for V_{IN} = 5V.
9	DRV2	Output of regulator #2. Drives the gate of an N-channel MOSFET to maintain V_{OUT2} set by R3 and R4.
10	IN	+5V or +12V supply.

Block Diagram

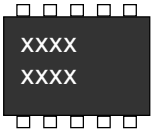


Marking Information

SC338

Top Mark

Bottom Mark



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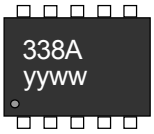
yyww: Date code (Example: 0012)
xxxx: Semtech Lot # (Example: E901
xxxx: 01-1)

SC338A

Top Mark



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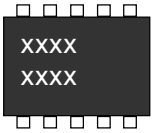

338A: Identifier for SC338A
yyww: Date code (Example: 0012)
xxxx: Semtech Lot # (Example: E901
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Theory Of Operation

The SC338(A) dual linear FET controller provides a simple way to drive two N-channel MOSFETs to produce tightly regulated output voltages from one or two available, higher, supply voltages. It takes its power from either a 5V or 12V supply, drawing typically 500µA while operating.

It contains an internal bandgap reference which is compared to the output voltages via resistor dividers. These resistor dividers are external and user selectable . Depending upon the input voltage used for the device, the drive pin (DRV1, DRV2) can pull up to a guaranteed minimum of 6.6V (from 12V supply) or 4.7V (from 5V supply). Thus the device can be used to regulate a large range of output voltages by careful selection of the external MOSFETs (see component selection, below).

The SC338(A) includes an active high enable control (EN1, EN2) for each output. If this pin is pulled low, the related drive pin is pulled low, turning off the N-channel MOSFET. If the pin is pulled up to $1.8V \le V_{EN} \le V_{IN}$, the drive pin will be enabled. This pin should not be allowed to float.

Each output has a power good output (PGD1, PGD2) which are open drain outputs that pull low if the related output is below the power good threshold (-12% of the programmed output voltage typical, -6% typical at start-up). The power good circuitry is active if the device is enabled, regardless of the state of the over current latch. The power good circuitry is not active if that particular output is disabled.

Also included for each output is an overcurrent protection circuit that monitors the output voltage. If the output voltage drops below 50% (typ.) of nominal, as would occur during an overcurrent or short condition, the device will pull the drive pin low and latch off. The device will need to have the power supply or enable pin toggled to reset the latch condition. Each output latches independently (i.e. if one output latches off, the other output will function normally).

Drive Outputs and Soft Start

The drive outputs for each output are source and sink capable. The sink current is typically 0.8mA at 5V in (1mA at 12V in). The source current is typically 2mA at 5V in and 3.75mA at 12V in during normal operation. The high side drive voltage is generated from V_{IN} by a 7V (nominal) low dropout regulator, thus at 12V in, 6.9V is available and at 5V in, 4.85V is available (since the LDO will be in dropout).

At start-up, the source current available from the drive pins is limited to 10µA (typical) until the power good threshold is reached, at approximately 6% below nominal output voltage. At this point the full drive capability is enabled. With this constant current source at start-up, it is a simple matter to use a small capacitor on the drive pin to slow this rate of rise. The rate of rise of the **drive pin** voltage will be:

$$\frac{dV_{DRV}}{dt} = \frac{I_{DRV}}{C_{SS}} \ V/s$$

A 10nF soft start capacitor will give a 1ms **output** rise time for V_{IN} = 12V and V_{OUT} = 1.05V, for example. The output rise time will of course depend upon the gate threshold of the MOSFET being used. Please refer to the Output Rise Time chart on Page 13 showing typical output rise times. For very low ESR output capacitors (<5mΩ) **and** very high soft start capacitance (>100nF), it may be necessary to add a resistor in series with the soft start capacitor to ensure stability. Generally, however, this resistor is not required, as this is a very unlikely situation.

The soft start capacitance does not adversely affect transient response since the drive current capability is 200 times higher once the device has started.

OCP and Power Supply Sequencing

The SC338(A) has output undervoltage protection that looks at a particular output to see if it is a) less than 50% (typical) of it's nominal value and b) V_{DRV} for that output is within 350mV (typical) of maximum. If both of these criteria are met, there is a 50µs (typical) delay and then the output is shut down. This provides inherent immunity to UV shutdown at start-up (which may occur while the output capacitors are being charged) since V_{DRV} has a very slow rate of rise with I_{DRV} limited to 10µA.

At start-up, it is necessary to ensure that the power supplies and enables are sequenced correctly to avoid erroneous latch-off. For UV latch-off not to occur at start-up due to sequencing issues, the key is that the voltage

Applications Infomation (Cont.)

supplied to the MOSFET drain should be greater than the output undervoltage threshold when that output is enabled. This assumes that the drop through the pass MOSFET is negligible. If not, then this drop needs to be taken into account also since:

$V_{OUT} = V_{DRAIN} - (I_{OUT} \times R_{DS(ON)})$.

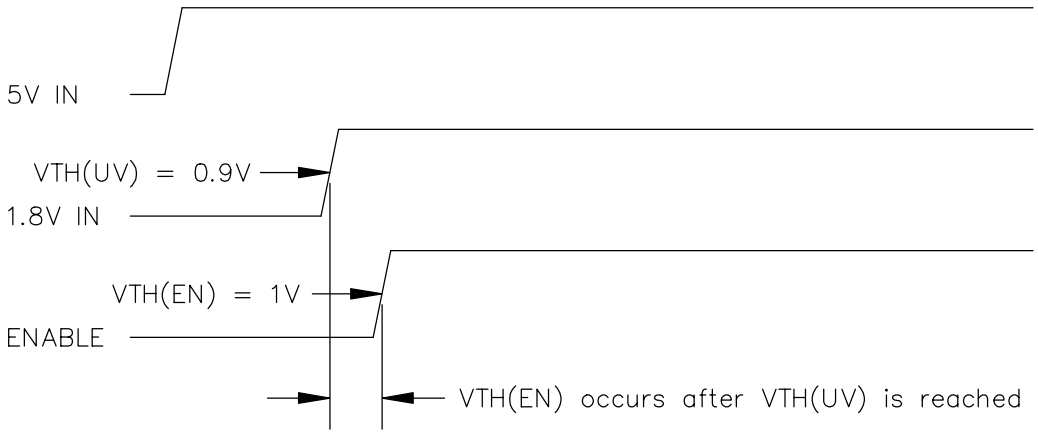
If the supply to the SC338(A) IN pin comes up before the supply to the MOSFET drain, then that output should be enabled as the supply to the MOSFET drain is applied - the Power Good signal for this rail would be ideal. If the power supply to the MOSFET drain comes up before the power supply to the SC338(A) IN pin, then the output can either be enabled with the supply to the IN pin or afterwards. Please see the example below.

Example: SC338(A) powered from 5V, output 1 powered from 1.8V set for 1.5V out, output 2 not shown for simplicity. Worst case undervoltage threshold is 60% (over temperature) of 1.5V, or 0.9V. The typical enable threshold is ~1V. See Figure 1 below.

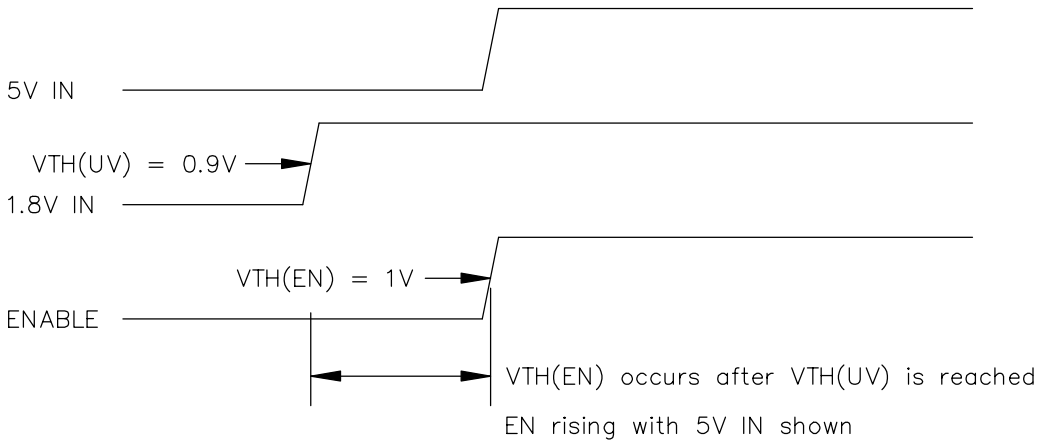
Component Selection

Output Capacitors: low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps are recommended for bulk capacitance, with ceramic bypass capacitors for decoupling high frequency transients.

Input Capacitors: placement of low ESR capacitors such as Sanyo POSCAPs or Panasonic SP-caps at the input to the MOSFET (V_{DRAIN}) will help to hold up the power supply during fast load changes, thus improving overall transient response. If V_{DRAIN} is located at the bulk capacitors for the upstream voltage regulator, additional capacitance



SC338(A) Supply Comes Up Before MOSFET Drain Supply



MOSFET Drain Supply Comes Up Before SC338(A) Supply

Figure 1: Power Supply Sequencing

Applications Infomation (Cont.)

may not be required. In this case a 0.1µF ceramic capacitor will suffice. The input supply to the SC338(A) should be bypassed with a 0.1µF ceramic capacitor.

MOSFETs: very low or low threshold N-channel MOSFETs are required. Selecting FETs rated for V_{GS} of 2.7V or 4.5V will depend upon the available drive voltage (6.9V from 12V in or 4.85V from 5V in), the output voltage and output current. For the device to work under all operating conditions, a maximum $R_{DS(ON)}$ must be met to ensure that the output will never go into dropout:

$$R_{DS(ON)(MAX)} = \frac{V_{IN(MIN)} - V_{OUT(MAX)}}{I_{OUT(MAX)}} \quad \Omega$$

Note that $R_{DS(ON)}$ must be met at all temperatures and at the minimum V_{GS} condition.

Setting The Output Voltage: the adjust pins connect directly to the inverting input of the error amplifiers, and the output voltage is set using external resistors (please refer to the Typical Application Circuit on page 1).

Using output 1 as an example, the output voltage can be calculated as follows:

$$V_{OUT} = 0.5 \bullet \left(1 + \frac{R1}{R2}\right)$$

The input bias current for the adjust pin is so low that it can be safely ignored. To avoid picking up noise, it is recommended that the total resistance of the feedback chain be less than 100kΩ.

Please see Table 1 on this page for recommended resistor values for some standard output voltages. All resistors are 1%, 1/10W.

The maximum output voltage that can be obtained from each output is determined by the input supply voltage and the $R_{DS(ON)}$ and gate threshold voltage of the external MOSFET. Assuming that the MOSFET gate threshold voltage is sufficiently low for the output voltage chosen and the worst-case drive voltage, $V_{OUT(MAX)}$ is given by:

$$V_{OUT(MAX)} = V_{DRAIN(MIN)} - I_{OUT(MAX)} \bullet R_{DS(ON)(MAX)}$$

VOUT (V)	R1 or R3 (kΩ)	R2 or R4 (kΩ)
1.05	11.0	10.0
1.2	14.0	10.0
1.5	20.0	10.0
2.5	45.3	11.3
3.3	63.4	11.3

Table 1: Recommended Resistor Values For SC338(A)

Design Example

Goal: 1.05V±5% @ up to 2.5A from 1.2V±5% and 5V±5%

Solution 1: no passive droop.

Total window for DC error, ripple and transient is ±52.5mV

Since this device is linear, and assuming that it has been designed to not ever enter dropout, we do not have ripple on the output.

The DC error for this output is the sum of:

V_{REF} accuracy = ±2.5% = ±26.3mV

Feedback chain tolerance = ±1% = ±10.5mV

Load regulation = ±0.25% = ±2.6mV

Set resistors per Table 1 should be 11.0kΩ (top) and 10.0kΩ (bottom).

Total DC error = ±3.75% = 39.4mV

This leaves ±1.25% = 13.1mV for the load transient ESR spike, therefore:

$$R_{ESR(MAX)} = \frac{13.1mV}{2.5A} = 5.2m\Omega$$

Bulk capacitance required is given by:

$$C_{BULK(MIN)} = \frac{dI \bullet t}{dV} \mu F$$

Where dI is the maximum load current step, t is the maximum regulator response time and dV is the

Applications Infomation (Cont.)

allowable voltage droop. Therefore with dI = 2.5A, t = 1µs, and dV = 13.1mV:

$$C_{BULK(MIN)} = \frac{2.5 \bullet 1 \bullet 10^{-6}}{13.1 \bullet 10^{-3}} = 191\mu F$$

So if we use 1% V_{OUT} set resistors we would select 2 x >100µF, 12mΩ POSCAPs for output capacitance (which assumes that local ceramic bypass capacitors will absorb the balance of the (6 - 5.3)mΩ ESR requirement - otherwise 10mΩ capacitors should be used).

If we use 0.1% set resistors, then the total DC error becomes ±2.85% = ±29.9mV, leaving ±2.15% = 22.6mV for the ESR spike. In this case:

$$R_{ESR(MAX)} = \frac{22.6mV}{2.5A} = 9.0m\Omega \quad \text{and}$$

$$C_{BULK(MIN)} = \frac{2.5 \bullet 1 \bullet 10^{-6}}{22.6 \bullet 10^{-3}} = 111\mu F$$

So for 0.1% resistors we could use 2 x 100µF, 18mΩ POSCAPs for output capacitance, or 1 x >100µF, 10mΩ POSCAP.

Obviously this is a very severe example, since the output voltage is so low and therefore the allowable window is very small. See solution 2 below for an alternate solution. For higher output voltages the components required will be less stringent.

The input capacitance needs to be large enough to stop the input supply from collapsing below -5% (i.e. the design minimum) during output load steps. If the input to the pass MOSFET is not local to the supply bulk capacitance then additional bulk capacitance may be required.

MOSFET selection: since the input voltage to the SC338(A) is 5V±5%, the minimum available gate drive is:

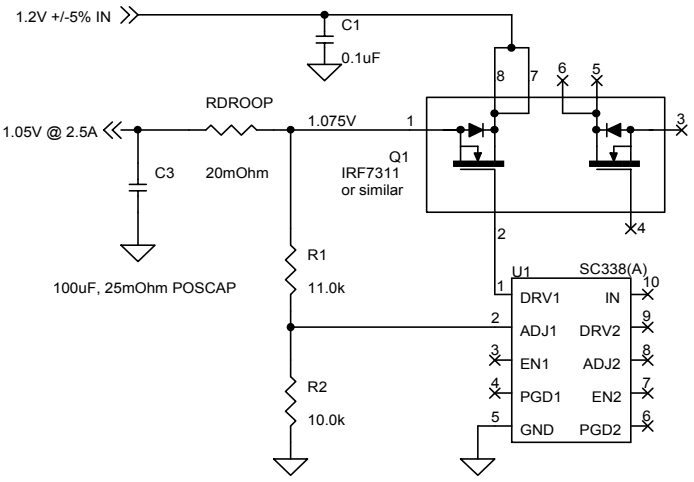
$$V_{GS} = (4.4 - 1.1025) = 3.3V$$

So a MOSFET rated for V_{GS} = 2.7V will be required, with an $R_{DS(ON)(MAX)}$ (over temp.) given by:

$$R_{DS(ON)MAX)} = \frac{(V_{IN(MIN)} - V_{OUT})}{I_{OUT(MAX)}} = \frac{(1.14 - 1.05)}{2.5} = 36m\Omega$$

Obviously, if a 12V rail is available to power the SC338(A), the number of FET options increases dramatically.

Solution 2: using passive droop.



Passive droop allows us to use almost the full output tolerance window for transients, hence making the output capacitor selection simpler and (hopefully) cheaper. The trade-offs are the cost of the droop resistor versus the reduction in output capacitor cost, and the reduction in headroom which impacts MOSFET selection. The top of the feedback chain connects to the "input" side of R_{DROOP}, and the output is set for 1.075V. Thus at no load, V_{OUT} will be 1.075V (or 1.05V + 2.4%) and at I_{OUT} = 2.5A, V_{OUT} will be 1.025V (or 1.05V - 2.4%).

If 1% set resistors are used, the total DC error will be ±3.75% = 39mV. Thus at no load, the minimum output voltage will be given by:

$$V_{OUT(MIN\_NO\_LOAD)} = 1.075 - 0.039 = 1.036V$$

This leaves 38.5mV for transient response, giving:

$$R_{ESR(MAX)} = \frac{38.5mV}{2.5A} = 15.4m\Omega \quad \text{and}$$

$$C_{BULK(MIN)} = \frac{2.5 \bullet 1 \bullet 10^{-6}}{38.5 \bullet 10^{-3}} = 65\mu F$$

Instead of 2 x 100µF, 12mΩ capacitors, we can use 1 x 100µF, 15mΩ capacitor.

Layout Guidelines

The advantages of using the SC338(A) to drive external MOSFETs are a) that the bandgap reference and control circuitry are in a die that does not contain high power dissipating devices and b) that the device itself does not

Applications Infomation (Cont.)

need to be located right next to the power devices. Thus very accurate output voltages can be obtained since changes due to heating effects will be minimal.

The 0.1µF bypass capacitor should be located close to the supply (IN) and GND pins, and connected directly to the ground plane.

The feedback resistors should be located at the device, with the sense line from the output routed from the load (or top end of the droop resistor if passive droop is being used) directly to the feedback chain. If passive droop is being used, the droop resistor should be located right at the load to avoid adding additional unplanned droop.

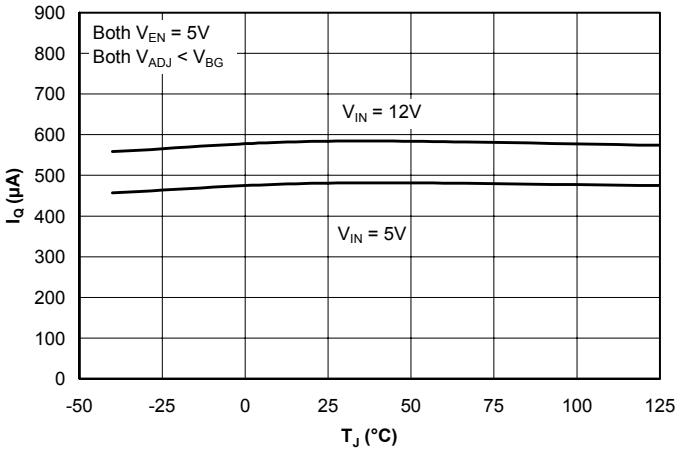
Sense and drive lines should be routed away from noisy traces or components.

For very low input to output voltage differentials, the input to output / load path should be as wide and short as possible. Where greater headroom is available, wide traces may suffice.

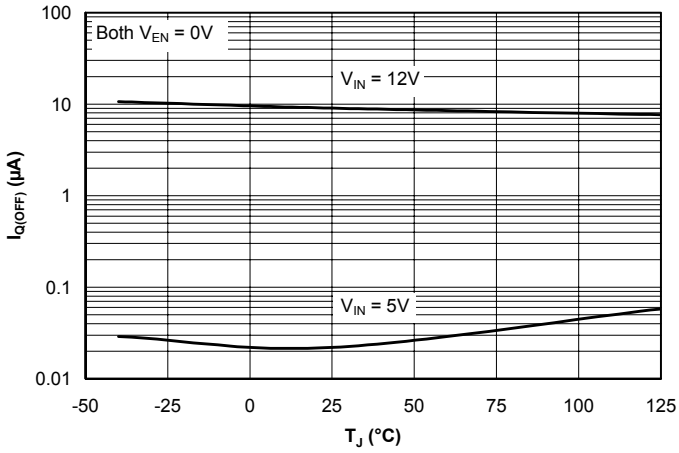
Power dissipation within the device is practically negligible, thus requiring no special consideration during layout. The MOSFET pass devices should be laid out according to the manufacturer's guidelines for the power being dissipated within them.

Typical Characteristics

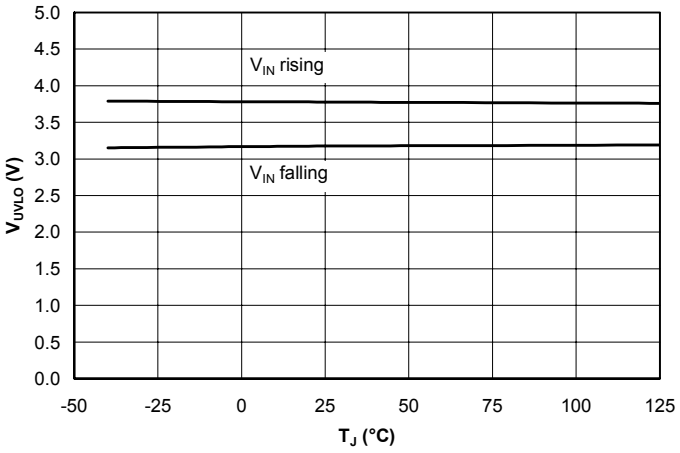
Quiescent Current vs. Junction Temperature vs. Input Voltage



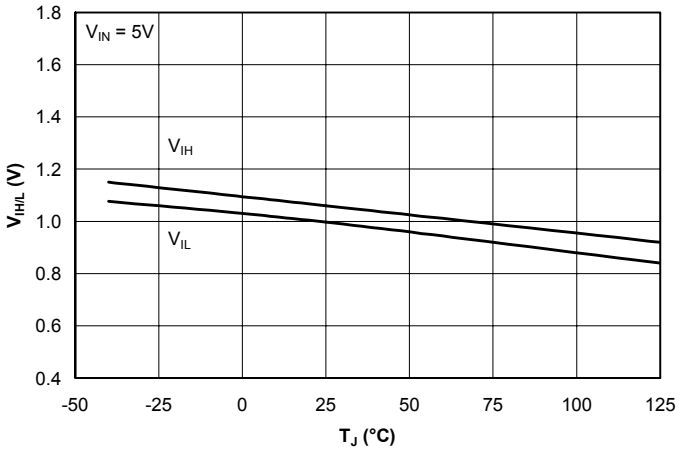
Standby Current vs. Junction Temperature vs. Input Voltage



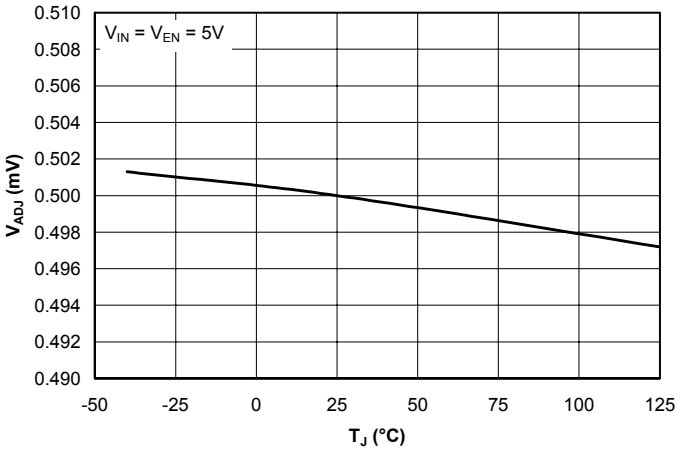
Start Threshold vs. Junction Temperature



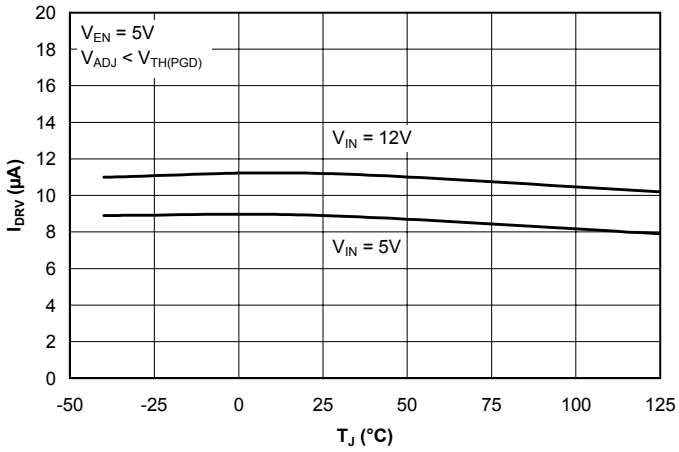
Enable Input Threshold Voltage vs. Junction Temperature



Reference Voltage vs. Junction Temperature

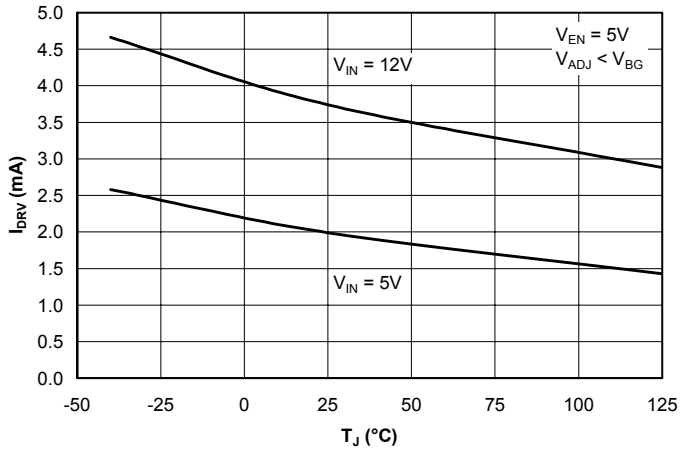


Drive Pin Output Current (Sourcing) at Startup vs. Junction Temperature vs. Input Voltage

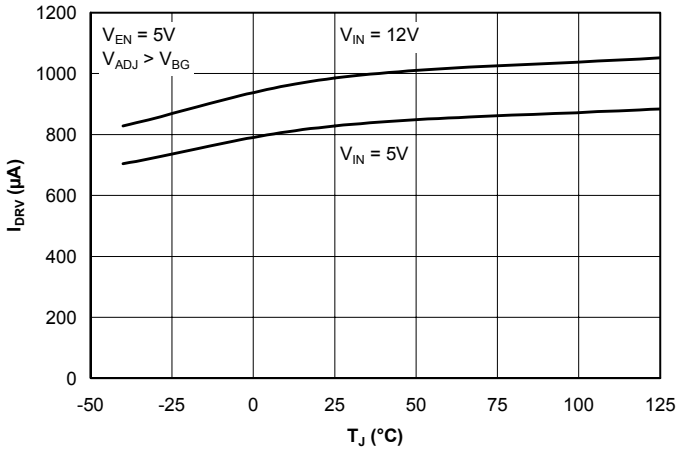


Typical Characteristics (Cont.)

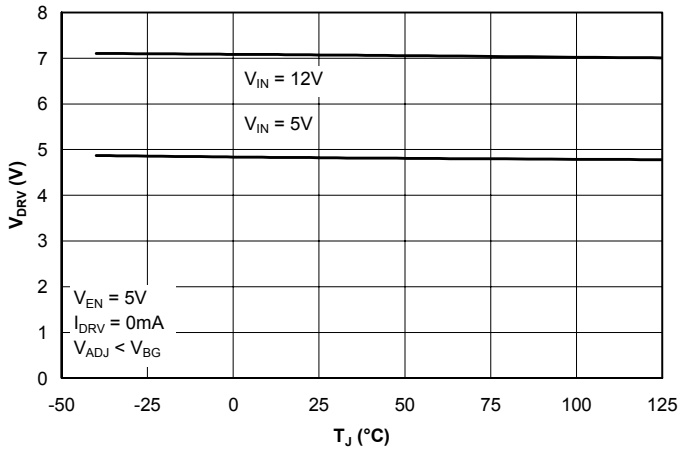
Drive Pin Output Current (Sourcing) vs. Junction Temperature vs. Input Voltage



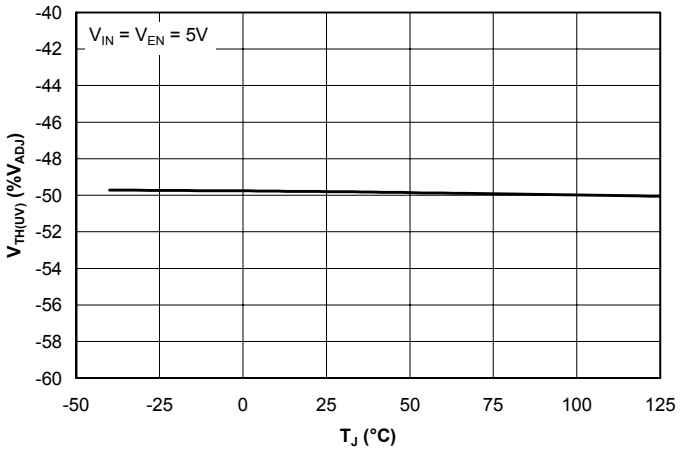
Drive Pin Output Current (Sinking) vs. Junction Temperature vs. Input Voltage



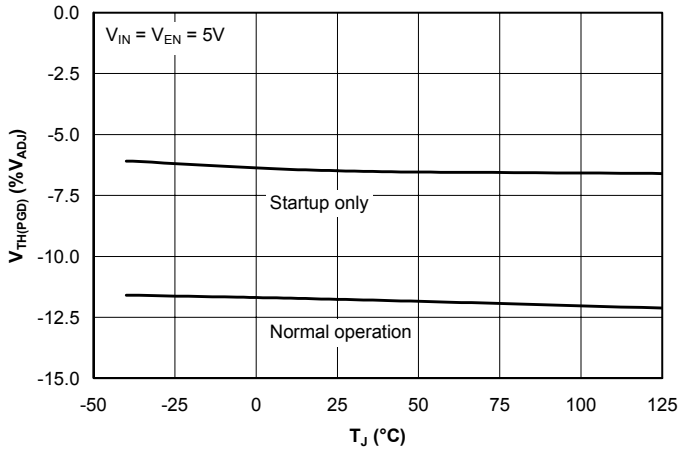
Drive Pin Output Voltage (Full On) vs. Junction Temperature vs. Input Voltage



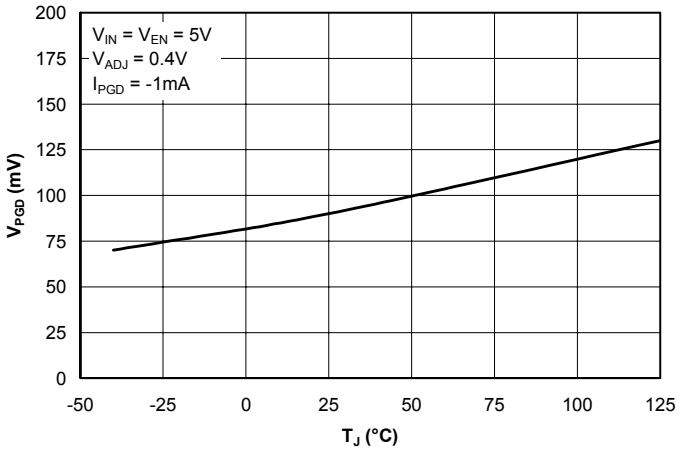
Under Voltage Trip Threshold vs. Junction Temperature



Power Good Threshold vs. Junction Temperature

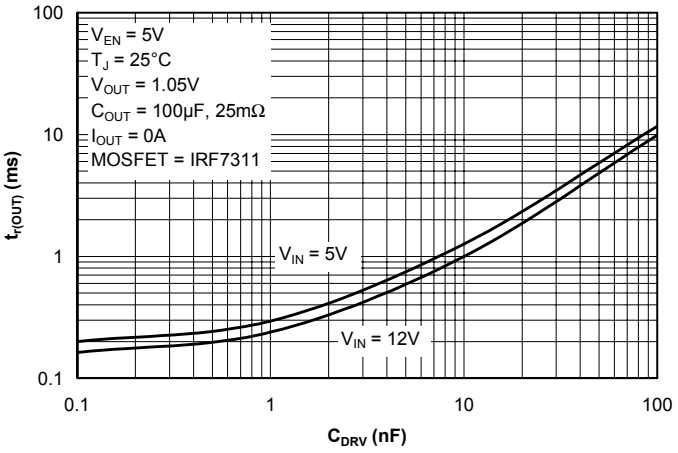


Power Good Logic Low Output Voltage vs. Junction Temperature

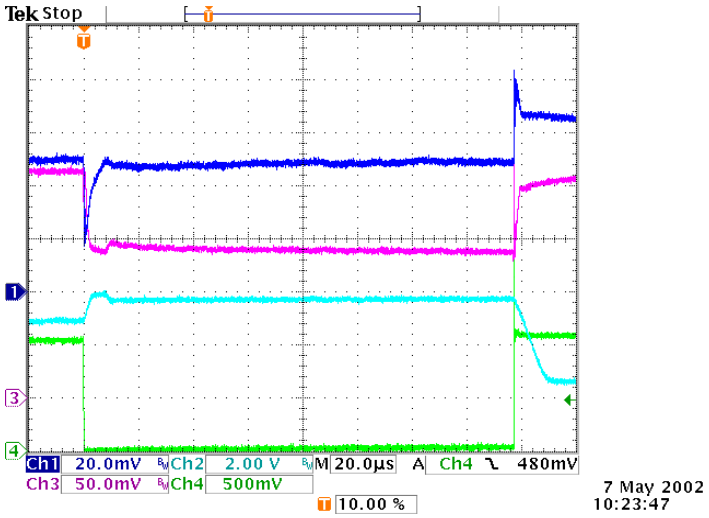


Typical Characteristics (Cont.)

Output Rise Time At Startup vs. Soft Start Capacitance vs. Input Voltage

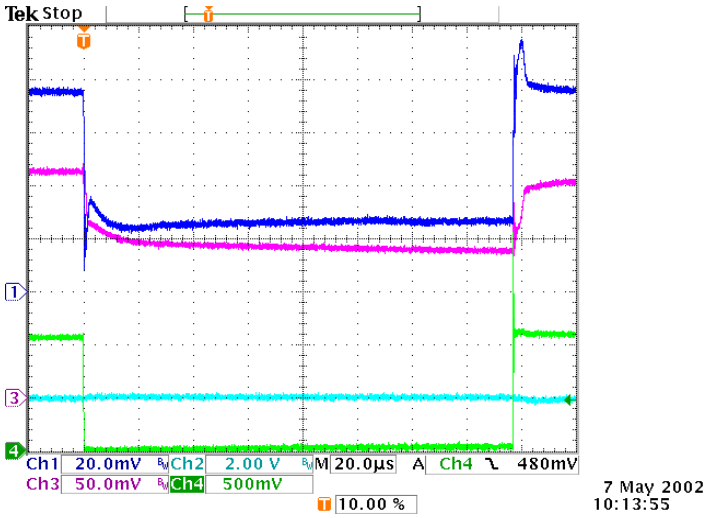


Load Transient Response, No Passive Droop



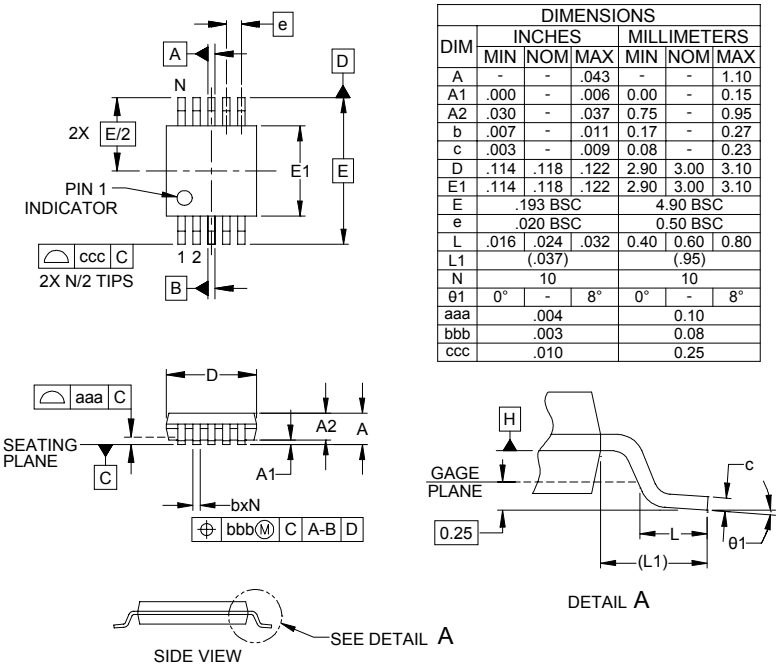
V_{IN} = 5V, 1.2V in to 1.05V out
I_{OUT} = 0.01A to 2.51A to 0.01A
C_{OUT} = 2 x 100µF, 25mΩ
Trace 1: V_{OUT}, 20mV/div., offset 1V
Trace 2: V_{DRV}, 2V/div.
Trace 3: 1.2V in, 50mV/div., offset 1V
Trace 4: load FET drain
Timebase: 20µs/div.
Load rise/fall times ≥ 35A/µs

Load Transient Response, With Passive Droop



V_{IN} = 5V, 1.2V in to 1.05V out
I_{OUT} = 0.01A to 2.51A to 0.01A
C_{OUT} = 1 x 100µF, 25mΩ
R_{DROOP} = 20mΩ
Trace 1: V_{OUT}, 20mV/div., offset 1V
Trace 2: not connected
Trace 3: 1.2V in, 50mV/div., offset 1V
Trace 4: load FET drain
Timebase: 20µs/div.
Load rise/fall times ≥ 35A/µs

Outline Drawing - MSOP-10

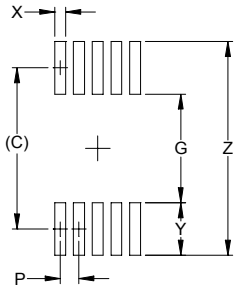


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.043	-	-	1.10
A1	.000	-	.006	0.00	-	0.15
A2	.030	-	.037	0.75	-	0.95
b	.007	-	.011	0.17	-	0.27
c	.003	-	.009	0.08	-	0.23
D	.114	.118	.122	2.90	3.00	3.10
E1	.114	.118	.122	2.90	3.00	3.10
E	.193 BSC			4.90 BSC		
e	.020 BSC			0.50 BSC		
L	.016	.024	.032	0.40	0.60	0.80
L1	(.037)			(.95)		
N	10			10		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.003			0.08		
ccc	.010			0.25		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-187, VARIATION BA.

Land Pattern - MSOP-10



DIM	INCHES	MILLIMETERS
C	(.161)	(4.10)
G	.098	2.50
P	.020	0.50
X	.011	0.30
Y	.063	1.60
Z	.224	5.70

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

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