

## High Voltage Buck LED Driver with Open Detection

### General Description

The RT8474A is a current-mode LED driver supporting wide input voltage range from 4.5V to 50V and output voltage up to 50V. With internal 500kHz operating frequency, the size of the external PWM inductor and input/output capacitors can be minimized. High efficiency is achieved by a 100mV current sensing control. LED dimming control can be done from either analog or PWM signal. The RT8474A provides an internal soft-start function to avoid inrush current and thermal shutdown to prevent the device from overheat.

The RT8474A is available in the SOP-8 (Exposed pad) package.

### Ordering Information

RT8474A	□	□
	—	Package Type
	SP	: SOP-8 (Exposed-Option 2)
	—	Lead Plating System
	G	: Green (Halogen Free and Pb Free)

Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

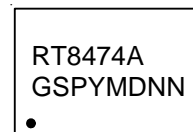
### Features

- High Voltage :  $V_{IN}$  Up to 50V,  $V_{OUT}$  Up to 50V
- Built-In 2A Power Switch
- Current-Mode PWM Control
- 500kHz Fixed Switching Frequency
- Analog or PWM Control Signal for LED Dimming
- Internal Soft-Start to Avoid Inrush Current
- Adjustable OVP for LED Open Protection
- Under-Voltage Lockout
- Thermal Shutdown
- RoHS Compliant and Halogen Free

### Applications

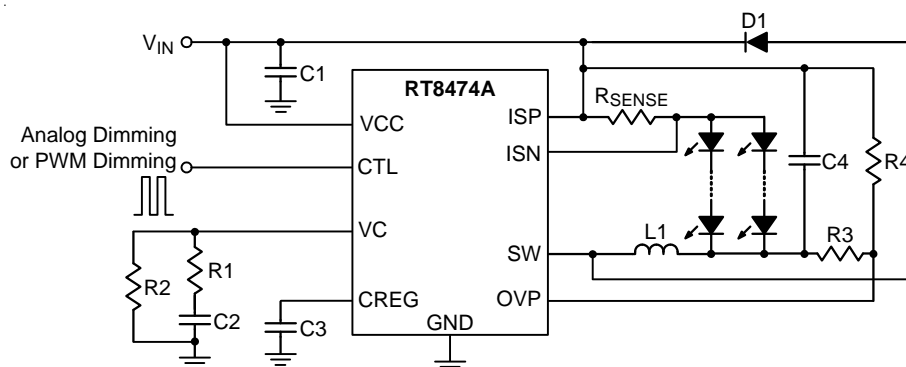
- Desk Lights and Room Lighting
- Industrial Display Backlight

### Marking Information

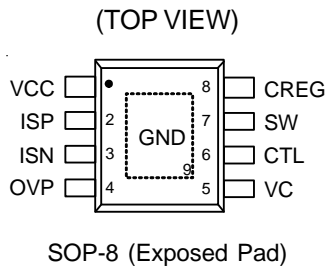


RT8474AGSP : Product Number  
YMDNN : Date Code

### Simplified Application Circuit



Pin Configurations



Functional Pin Description

Pin No.	Pin Name	Pin Function
1	VCC	Supply Voltage Input. For good bypass, connect a low ESR capacitor between this pin and GND.
2	ISP	Positive Current Sense Input.
3	ISN	Negative Current Sense Input. Voltage threshold between ISP and ISN is 100mV.
4	OVP	Over-Voltage Protection Sense Input.
5	VC	Compensation Node for Current Loop.
6	CTL	Analog Dimming Control Input. Effective programming range is 0.2V to 1.2V.
7	SW	Switch Node of the PWM Converter.
8	CREG	Regulator Output for Internal Circuit. Place a 1μF capacitor to stabilize the 5V output regulator.
9 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.



## Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VCC ----- -0.3V to 60V
- SW Pin Voltage at Switching off, ISP, ISN, OVP ----- -0.3V to 60V
- CREG Voltage ----- -0.3V to 6V
- CTL Voltage (Note 2) ----- -0.3V to 20V
- Power Dissipation, P<sub>D</sub> @ T<sub>A</sub> = 25°C
  - SOP-8 (Exposed Pad) ----- 3.44W
- Package Thermal Resistance (Note 3)
  - SOP-8 (Exposed Pad), θ<sub>JA</sub> ----- 29°C/W
  - SOP-8 (Exposed Pad), θ<sub>JC</sub> ----- 2°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 4)
  - HBM (Human Body Model) ----- 2kV
  - MM (Machine Model) ----- 200V

## Recommended Operating Conditions (Note 5)

- Supply Input Voltage ----- 4.5V to 50V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

(V<sub>CC</sub> = 5V, C<sub>IN</sub> = 1μF, T<sub>A</sub> = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Overall</b>						
Regulator Output Voltage	V <sub>CREG</sub>	I <sub>CREG</sub> = 20mA	4.5	5	5.5	V
Supply Current	I <sub>VCC</sub>	V <sub>C</sub> ≤ 0.4V	--	--	3	mA
VIN Under-Voltage Lockout Threshold	V <sub>UVLO</sub>	V <sub>IN</sub> Rising	--	4.2	4.5	V
		V <sub>IN</sub> Falling	3.9	4.1	--	
<b>Current Sense Amplifier</b>						
Input Threshold (V <sub>ISP</sub> – V <sub>ISN</sub> )		V <sub>CTL</sub> ≥ 1.25V	97	100	103	mV
Input Current	I <sub>ISP</sub>	V <sub>ISP</sub> = 24V	--	200	--	μA
Input Current	I <sub>ISN</sub>	V <sub>ISN</sub> = 24V	--	20	--	μA
Output Current	I <sub>VC</sub>	2.4V > V <sub>C</sub> > 0.3V	--	±10	--	μA
VC Threshold for CTL Switch Off			--	0.4	--	V
<b>LED Dimming</b>						
Input Current of CTL Pin	I <sub>CTL</sub>	0.2V ≤ V <sub>CTL</sub> ≤ 1.2V	--	1	2	μA
LED Current Off Threshold at CTL	V <sub>CTL_OFF</sub>		0.15	0.2	0.25	V
LED Current On Threshold at CTL	V <sub>CTL_ON</sub>		--	1.2	1.5	V

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>PWM Converter</b>						
Switch Frequency	f <sub>SW</sub>		440	500	540	kHz
Maximum Duty Cycle	D <sub>MAX</sub>		--	--	100	%
Minimum On-Time			--	100	200	ns
SW R <sub>DS(ON)</sub>			--	0.15	--	Ω
SW Current Limit	I <sub>LIM_SW</sub>		2	2.5	--	A
<b>Over-Voltage Protection and Soft-Start</b>						
OVP Threshold	V <sub>OVP</sub>	V <sub>ISP</sub> – V <sub>OVP</sub>	1.15	1.2	1.25	V
OVP Recovery		V <sub>OVP</sub> = 1.2V	--	1	--	V
OVP Input Current	I <sub>OVP</sub>	V <sub>OVP</sub> ≤ 1.5V	--	30	--	μA
Soft-Start Time		(Note 6)	--	5.7	--	ms
<b>Over-Temperature Protection</b>						
Thermal Shutdown Threshold	T <sub>SD</sub>		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT <sub>SD</sub>		--	20	--	°C

**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.** If connected with a 20kΩ serial resistor, PWM can go up to 40V.

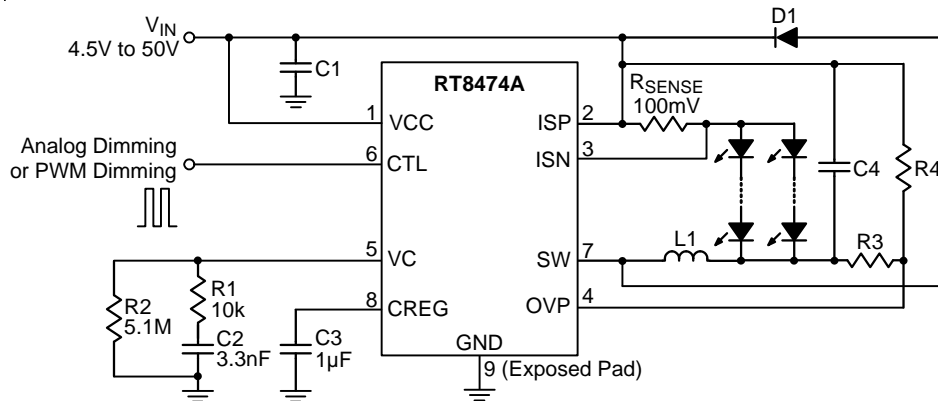
**Note 3.** θ<sub>JA</sub> is measured at T<sub>A</sub> = 25°C on a high effective thermal conductivity four-layer test board per JEDEC 51-7. θ<sub>JC</sub> is measured at the exposed pad of the package.

**Note 4.** Devices are ESD sensitive. Handling precaution is recommended.

**Note 5.** The device is not guaranteed to function outside its operating conditions.

**Note 6.** Guarantee by design, not subject to production testing.

## Typical Application Circuit

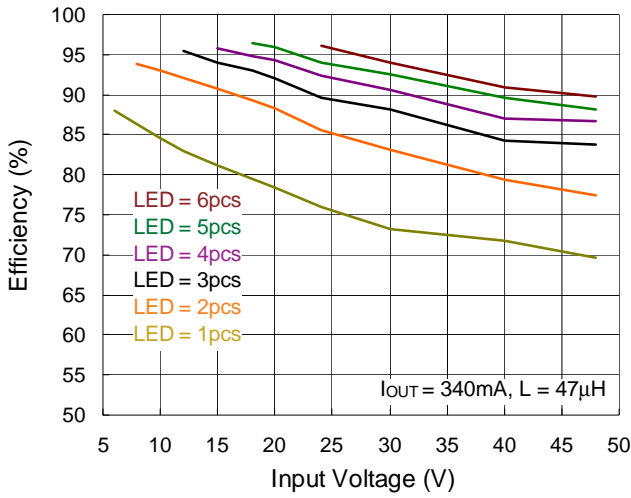


**Table 1. Suggested Components Selection**

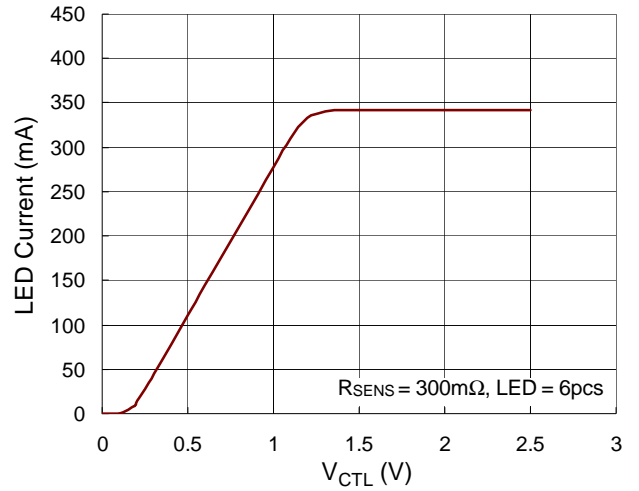
VIN	LED (pcs)	OVP SET (V)	R3	R4	I <sub>LED_spike</sub> (mA)	V <sub>OUT</sub> (V)
12V	3	0.9	150k	10k	1100	10
		1	120k	10k	1100	
		1.1	110k	10k	1000	
24V	6	0.9	316k	10k	1200	20
		1	270k	10k	1200	
		1.1	232k	10k	1150	
32V	9	0.9	470k	10k	700	30
		1	402k	10k	700	
		1.1	360k	10k	650	
42V	12	0.9	649k	10k	650	40
		1	560L	10k	650	
		1.1	499k	10k	600	

**Typical Operating Characteristics**

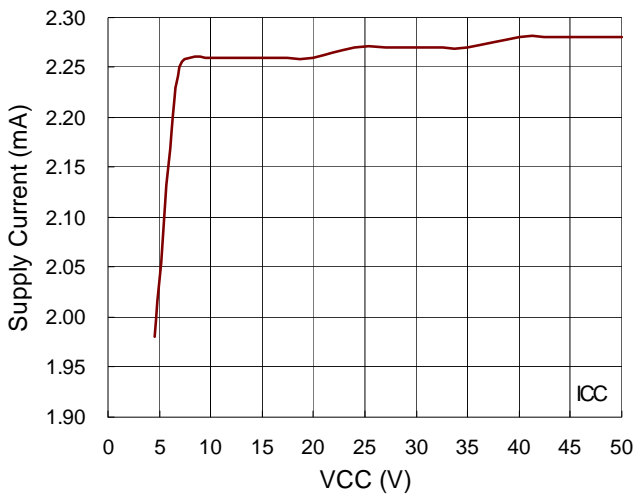
**Efficiency vs. Input Voltage**



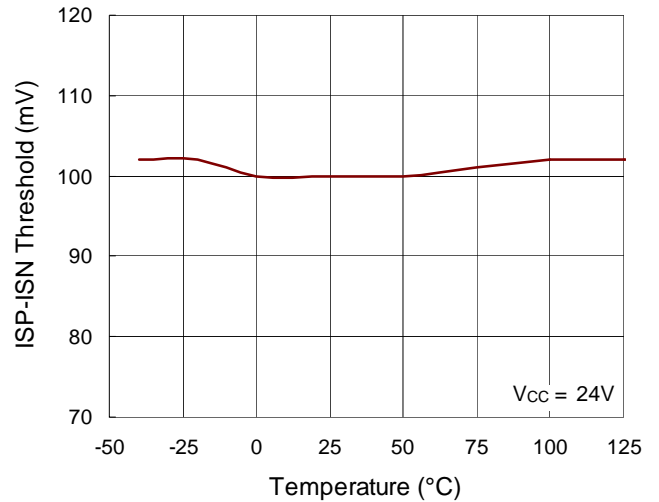
**LED Current vs.  $V_{CTL}$**



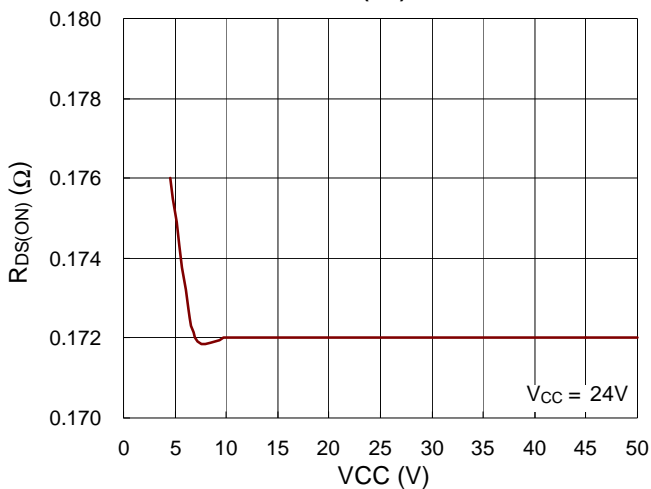
**Supply Current vs. VCC**



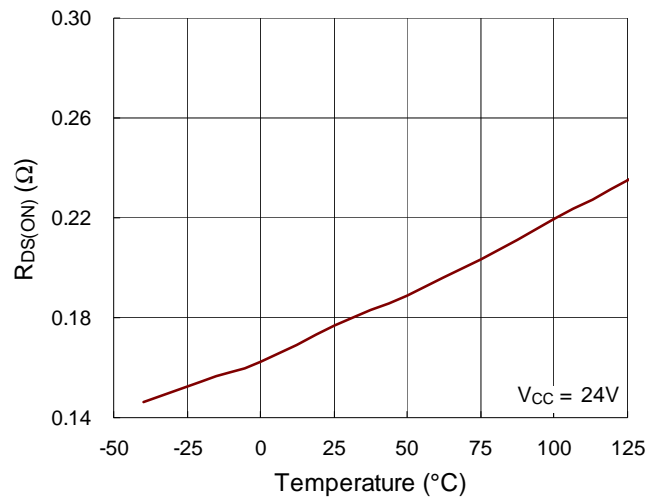
**ISP-ISN Threshold vs. Temperature**



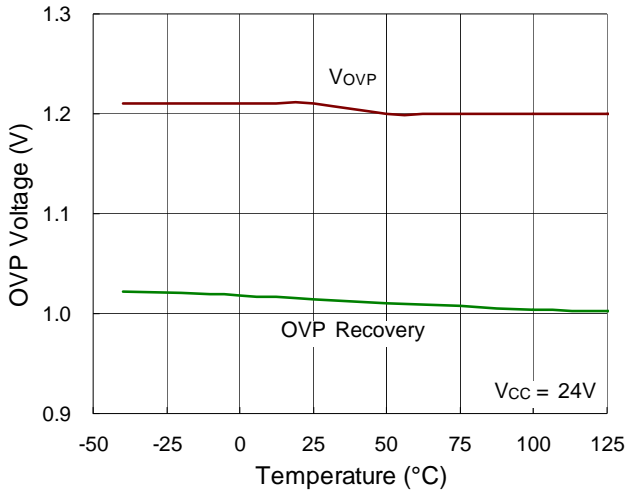
**SW  $R_{DS(ON)}$  vs. VCC**



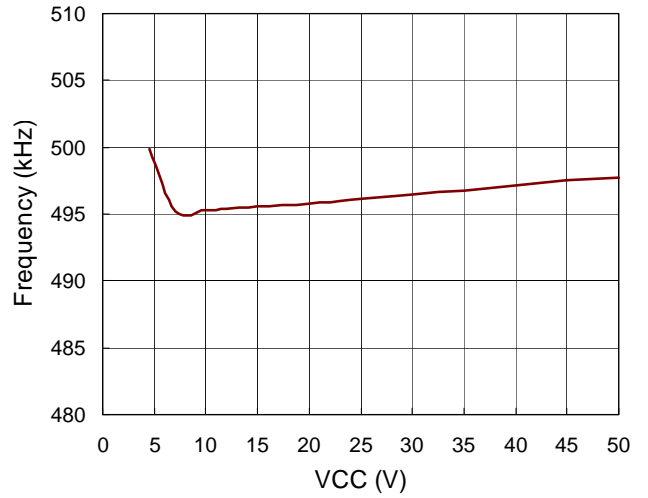
**SW  $R_{DS(ON)}$  vs. Temperature**



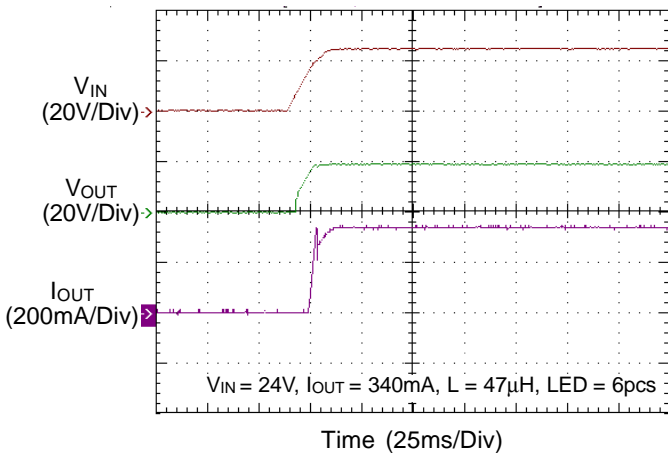
OVP Voltage vs. Temperature



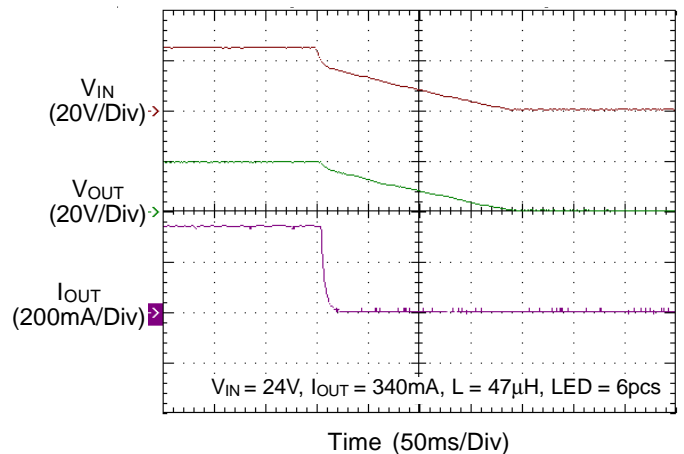
Frequency vs. VCC



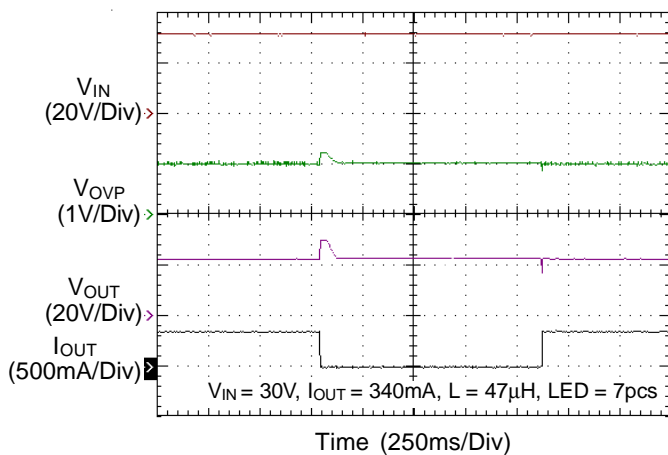
Power On from VCC



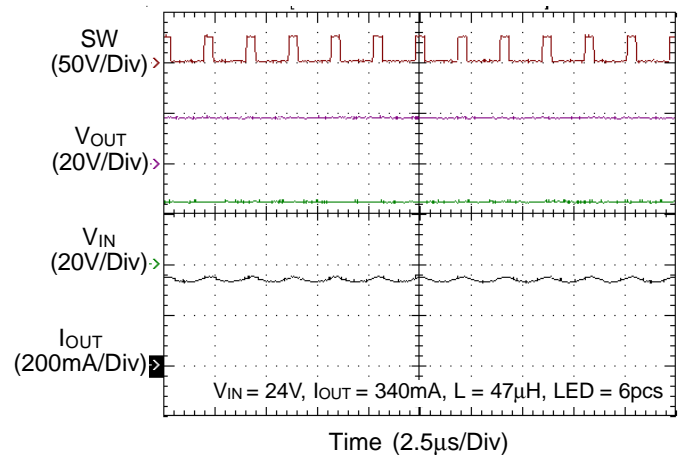
Power Off from VCC



OVP Turn On when LED Take Off and Restore



Switching





## Application Information

The RT8474A is specifically designed to be operated in Buck converter applications. This device uses a fixed frequency, current-mode control scheme to provide excellent line and load regulation. The control loop has a current sense amplifier which senses the voltage between the ISP and ISN pins and provides an output voltage at the VC pin. A PWM comparator then turns off the internal power switch when the sensed power switch current exceeds the compensated VC pin voltage. The power switch will not be reset by the oscillator clock in each cycle. If the comparator does not turn off the switch in a cycle, the power switch will be on for more than a full switching period until the comparator is tripped. In this manner, the programmed voltage across the sense resistor is regulated by the control loop.

### Frequency Compensation

The RT8474A has an external compensation pin, allowing the loop response to be optimized for specific applications. An external resistor in series with a capacitor is connected from the VC pin to GND to provide a pole and a zero for proper loop compensation. The typical value for the RT8474A is 10k and 3.3nF.

### LED Current Setting

The LED current can be calculated by the following equation :

$$I_{LED(MAX)} = \frac{(V_{ISP} - V_{ISN})}{R_{SENSE}}$$

where  $(V_{ISP} - V_{ISN})$  is the voltage between the ISP and ISN pins (100mV typ. if CTL dimming is not applied) and the  $R_{SENSE}$  is the resistor between the ISP and ISN pins.

### Current Limit

The RT8474A can limit the peak switch current with its internal over-current protection feature. In normal operation, the power switch is turned off when the switch current hits the loop-set value. The over-current protection function will turn off the power switch independent of the loop control when the peak switch current reaches around 2A.

### Output Over-Voltage Setting

When using constant current to drive LEDs, removed or turned LEDs on instantly can be dangerous for both the LED and the LED driver. Harmful spikes are generated when large currents are instantaneously turned on. The RT8474A provided the Over-Voltage Protection (OVP) function to detect the spike and switch off LED driver immediately. When the voltage between the OVP pin and ISP pin exceeds a threshold of approximately 1.2V, the power switch is turned off. The power switch can be turned on again once the voltage between the OVP pin and ISP pin drops below 1V. For typical LED driver application, the output voltage could be clamped at a certain voltage level. If OVP happened,

$$ISP - V_{OVP} > 1.2V$$

Where the  $V_{OUT}$  is the terminal voltage between LED string, R3 and R4 are the voltage divider from  $V_{OUT}$  with the divider center node connected to the OVP pin. Normally, set R4 for 10kΩ in typical application.

When OVP happened between  $V_{OUT}$ ,  $ISP - V_{OVP}$  is 1.2V.

To avoid the inrush current during over-voltage protection, we set the ISP-OVP voltage from 0.9 to 1.1V. Refer the table 1, the R3 could be selected for different inrush current concern.

### Over-Temperature Protection

The RT8474A has Over-Temperature Protection (OTP) function to prevent the excessive power dissipation from overheating. The OTP function will shut down switching operation when the die junction temperature exceeds 150°C. The chip will automatically start to switch again when the die junction temperature cools off.

### Inductor Selection

Choose an inductor that can handle the necessary peak current without saturating and ensure that the inductor has a low DCR (copper-wire resistance) to minimize  $I^2R$  power losses. A 4.7μH to 22μH inductor will meet the demand of most of the RT8474A applications. Inductor manufacturers specify the maximum current rating as the

current where the inductance falls to certain percentage of its nominal value, typically 65%. In Buck application where the transition between discontinuous and continuous modes occurs, the value of the required output inductor, L, can be approximated by the following equation :

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L(MAX)} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN(MAX)}} \right]$$

The ripple current  $\Delta I_L$  can be calculated :

$$\Delta I_L = \left[ \frac{V_{OUT}}{f \times L} \right] \times \left[ 1 - \frac{V_{OUT}}{V_{IN}} \right]$$

where,

$V_{OUT}$  = output voltage.

$V_{IN}$  = input voltage.

f = switching frequency.

### Schottky Diode Selection

The Schottky diode, with their low forward voltage drop and fast switching speed, is necessary for RT8474A applications. In addition, power dissipation, reverse voltage rating and pulsating peak current are important parameters of the Schottky diode that must be considered. The diode's average current rating must exceed the average output current. The diode conducts current only when the power switch is turned off (typically less than 50% duty cycle).

### Capacitor Selection

The input capacitor reduces current spikes from the input supply and minimizes noise injection to the converter. For most RT8474A applications, a 4.7 $\mu$ F ceramic capacitor is sufficient. A value higher or lower may be used depending on the noise level from the input supply and the input current to the converter. In Buck application, the output capacitor is typically ceramic and selection is mainly based on the output voltage ripple requirements. The output ripple,  $\Delta V_{OUT}$ , is determined by the following equation :

$$\Delta V_{OUT} \leq \Delta I_L \times \left[ ESR + \frac{1}{8 \times f \times C_{OUT}} \right]$$

### Thermal Considerations

For continuous operation, do not exceed the maximum operation junction temperature 125°C. The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum operation junction temperature,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating conditions specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOP-8 (Exposed Pad) package, the thermal resistance  $\theta_{JA}$  is 29°C/W on the standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (29^\circ\text{C/W}) = 3.44\text{W for SOP-8 (Exposed Pad) package}$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance  $\theta_{JA}$ . The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

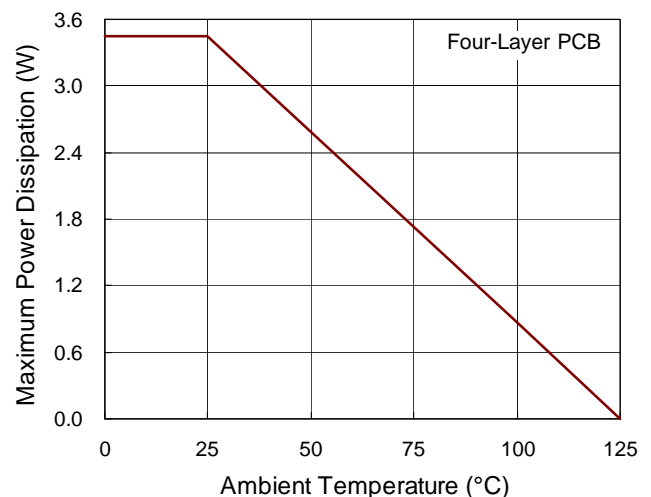


Figure 1. Derating Curve of Maximum Power Dissipation

**Layout Considerations**

PCB layout is very important when designing power switching converter circuits. Some recommended layout guide lines are as follows :

▶ The power components L1, D1 and C4 must be placed as close to each other as possible to reduce the ac current loop area. The PCB trace between power components must be as short and wide as possible due to large current flow through these traces during operation.

- ▶ Place L1 and D1 as close to each other as possible. The trace should be as short and wide as possible.
- ▶ The input capacitor C1 must be placed as close to the VCC pin as possible.
- ▶ Place the compensation components to the VC pin as close as possible to avoid noise pickup.

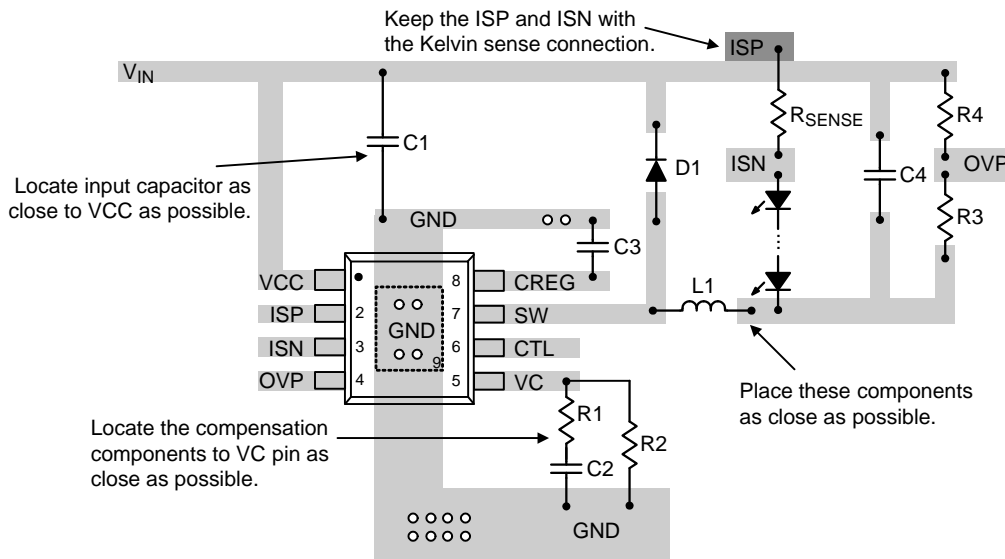
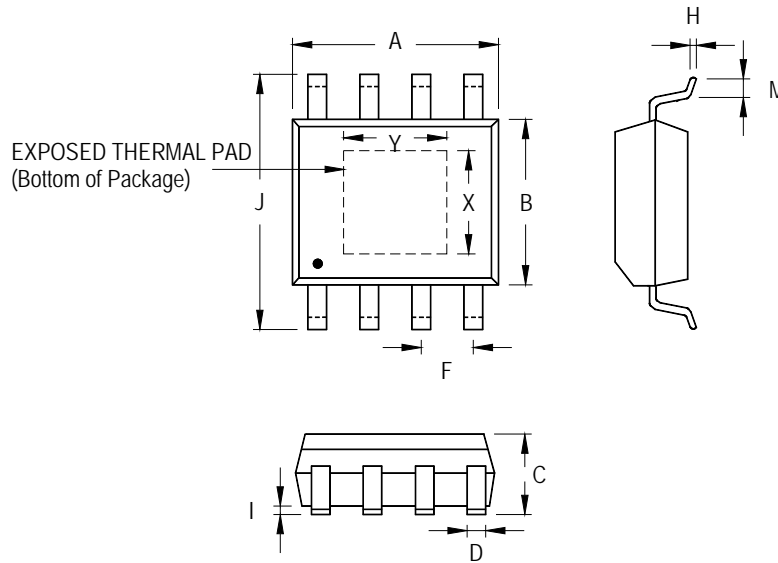


Figure 2. PCB Layout Guide

Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches		
	Min	Max	Min	Max	
A	4.801	5.004	0.189	0.197	
B	3.810	4.000	0.150	0.157	
C	1.346	1.753	0.053	0.069	
D	0.330	0.510	0.013	0.020	
F	1.194	1.346	0.047	0.053	
H	0.170	0.254	0.007	0.010	
I	0.000	0.152	0.000	0.006	
J	5.791	6.200	0.228	0.244	
M	0.406	1.270	0.016	0.050	
Option 1	X	2.000	2.300	0.079	0.091
	Y	2.000	2.300	0.079	0.091
Option 2	X	2.100	2.500	0.083	0.098
	Y	3.000	3.500	0.118	0.138

8-Lead SOP (Exposed Pad) Plastic Package

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