RTL8305SC

SINGLE-CHIP 5-PORT 10/100MBPS SWITCH CONTROLLER WITH DUAL MII INTERFACES

DataSheet

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USING THIS DOCUMENT

This document is intended for use by the software engineer when programming for Realtek RTL8305SC controller chips. Information pertaining to the hardware design of products using these chips is contained in a separate document.

Though every effort has been made to assure that this document is current and accurate, more information may have become available subsequent to the production of this guide. In that event, please contact your Realtek representative for additional information that may help in the development process.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2004/06/17	First release.
1.1	2004/06/30	Removed QoS function IPv6 differentiated services and removed Table 147, page 113.
		Revised LEDMODE[1:0]=00, in Table 4, page 14, Table 7, page 20, Table 19, page 30, and Table 69, page 59. Changed four combinations of LED mode to three combinations of LED display mode, page 3.
1.2	2005/03/02	Corrected section 7.3.10 PHY 2 Register 23: "Port 2 Control Register 1" to "Global Option 1 Register", page 71.
		Revised pull low resister to 1k ohm, Table 5, page 16.
		Revised PHY register in Table 64, page 55.
		Changed Table 139's name from PHY 0 to PHY 5, page 87.
		Changed Table 140's name from PHY 8 to PHY 5, page 88.
		Add P4PHY_MODE select, in Table 143, page 103.
		Corrected Pin52 MTXEN/PRXDV/EN_TRUNK to MTXEN/PRXDV, Pin92 LED_ACT[4]/DISFCAUTOOFF to LED_ACT[4], and Pin115 ENAGBACK/LED_DUP[0] to LED_DUP[0], in Figure 2, page 7, and Table 1, page 8.
		Canceled the description of Pin92 LED_ACT[4]/DISFCAUTOOFF and Pin115 ENAGBACK/LED_DUP[0], section 1, page 2, in Table 9, page 22, and section 8.3.10, page 123.
		Reserved PHY 0 Register 18.7 and 18.15, in Table 68, page 58.
		Reserved EEPROM Register 4.7, in Table 16, page 28 and Register 5.7, Table 17, page 29.
		Corrected QoS based features, section 2, page 4.
		Corrected 2SB1188K to 2SB1188 and HVDD18 to DVDD18, in Figure 24, page 132, and Table 151, page 132.
		Corrected "24LC02 must be 1.8Vcompatible" to "24LC02 must be 3.3Vcompatible", section 8.3.3, page 117.
		Corrected TTL Input High Voltage 1.5V to 2.0V and TTL Input Low Voltage 1.0V to 0.8V, section 9.3, page 134.
		Corrected PHY 4 register 18 description, in Table 124, page 81.
		Add 100Base-TX TD and RD Differential Output Impedance (return loss) columns and delete 10Base-TX TD and RD Differential Output Impedance (return loss) columns, in Section 9.4 AC Characteristics, page 135.

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1. General Description

The RTL8305SC is a 5-port Fast Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. All ports support 100Base-FX, which shares pins (TX+-/RX+-) with UTP ports and needs no SD+/- pins, a development using Realtek proprietary technology. To compensate for the lack of auto-negotiation in 100Base-FX applications, the RTL8305SC can be forced into 100Base-FX half or full duplex mode, and can enable or disable flow control in fiber mode.

The five ports are separated into three groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select port members in GroupX and GroupY. When the port members have been determined, you may use a mode selection pin (GxMode/Gymode/P4Mode[1:0]) to select operating interfaces such as 10/100Base-TX, 100Base-FX. Each group has four pins for selecting initial port status upon reset (ANEG/Force, 100/10, Full/Half, Enable/Disable Flow Control). Upon reset, in addition to using strapping pins, a CPU can also configure the RTL8305SC via the MDC/MDIO interface.

The fifth port (port 4) supports an external MAC and an external PHY interface. The external MAC interface can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with a routing engine, HomePNA, or VDSL transceiver. The external PHY interface can be set to PHY mode MII in the digital interface, and UTP or fiber in the differential interface. In order to accomplish diagnostics in complex network systems, the RTL8305SC also provides a loopback feature in each port for a variable CPU system.

The RTL8305SC contains a 1K-entry address lookup table and supports a 16-entry CAM to avoid hash collisions and to maintain forwarding performance. The 1K-entry table provides read/write access from the SMI interface, and each of the entries can be configured as a static entry. A static entry indicates that this entry is controlled by the external management processor and automatic aging and learning of the entry will not take place. The RTL8305SC supports IEEE 802.3x full-duplex flow control and back-pressure half-duplex flow control. A broadcast storm filtering function is provided to filter unusual broadcast storm issues, and an intelligent switch engine prevents Head-Of -Line blocking problems.

The RTL8305SC supports 16 VLAN groups. These can be configured as port-based VLANs and/or IEEE 802.1Q tag-based VLANs. Two ingress filtering and egress filtering options provide flexible VLAN configuration:

- Ingress filtering option 1: The Acceptable Frame Type of the Ingress Process can be set to 'Admit All' or 'Admit All Tagged'.
- Ingress filtering option 2: 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set.
- Egress filtering option 1: 'Forward' or 'Discard' ARP broadcast frames.
- Egress filtering option 2: 'Forward' or 'Discard' Leaky VLAN frames.

The RTL8305SC supports several types of QoS functions with two-level priority queues to improve multimedia or real-time networking applications. The QoS functions are based on:

- Port-based priority
- 802.1Q VLAN priority tag
- The TOS/DS (DiffServ) field of TCP/IP

When the QoS function is enabled, a VLAN tag can be inserted or removed at the output port. The RTL8305SC will insert a Port VID (PVID) for untagged frames or remove the tag from tagged frames. The RTL8305SC also supports a special insert VLAN tag function to separate traffic from WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8305SC supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8305SC also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

Maximum packet length can be 1536 or 1552 bytes according to the initial configuration (strapping upon reset). The filtering function is supported for the 802.1D specified reserved multicast addresses (01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F).

The RTL8305SC provides flexible LED functions for diagnostics. These include: Three combinations of link, activity, speed, duplex and collision, that are ideal for bi-color LED displays. The RTL8305SC also provides a loop detection function and alarm, for network existence notification, with an output pin that can be designed as a visual LED or a status input pin for a CPU.

A power saving mode is implemented on a per-port basis. Each port automatically enters power saving mode 10 seconds after the cable is disconnected from it. The RTL8305SC also implements a power down mode on a per-port basis. Users can set MII Reg.0.11 to force the corresponding port to enter power down mode, which disables all transmit/receive functions, except SMI (MDC/MDIO management interface).

Each physical layer channel of the RTL8305SC consists of a 4B5B encoder/decoder, a Manchester encoder/decoder, a scrambler/de-scrambler, a transmit output driver, output wave shaping filters, a digital adaptive equalizer, a PLL circuit, and a DC restoration circuit for clock/data recovery. Friendly crossover auto detection and correction functions are also supported for easy cable connection.

The integrated chip benefits from low power consumption, advanced functions with flexible configuration for 5-port SOHO switch, Home Gateway, xDSL/Cable router, and other IA applications.

2. Features

- 5-port integrated switch controller with memory and transceiver for 10Base-T and 100Base-TX with:
  - 5-port 10/100M UTP or
  - 4-port 10/100M UTP + 1-port MII/SNI or
  - 4-port 10/100M UTP + 1-port MAC MII/SNI + 1-port PHY MII
- Supports the fifth port MAC circuit as PHY mode MII, SNI for router applications, and MAC mode MII for HomePNA or VDSL solutions
- Supports the fifth port PHY circuit as PHY mode MII for router and Gateway applications
- All ports support 100Base-FX with optional flow control enable/disable and full/half-duplex setting
- Supports FEFI function for fiber application
- Non-blocking wire-speed reception and transmission and non-head-of-line-blocking forwarding
- Fully compliant with IEEE 802.3/802.3u auto-negotiation function
- Built-in high-efficiency SRAM for packet buffer, with 1K-entry lookup table and 16-entry CAM
- Supports broadcast storm filtering function
- Flow control fully supported:
  - Half duplex: back pressure flow control
  - Full duplex: IEEE 802.3x flow control
- Supports SMI (Serial Management Interface: MDC/MDIO) for programming and diagnostics
- Supports loop detection function with one LED to indicate the existence of a loop
- Supports MAC and PHY loopback function for diagnosis
- Supports up to 16 VLAN groups
- Flexible 802.1Q port/tag-based VLAN
- ARP VLAN for broadcast packets
- Leaky VLAN for unicast packets
- VLAN tag Insert/Remove function
- Supports QoS function on each port:
  - QoS based on: (1) Port-based, (2) VLAN tag, (3) TCP/IP header's TOS/DS
  - Supports two-level priority queues
  - Weighted round robin service

- Supports special VLAN tag insert or remove function on per-port basis (egress) to separate WAN traffic from LAN traffic
- Optional 1536 or 1552 byte maximum packet length
- Supports reserved control frames (DID=0180C2000003~0180C200000F) filtering function
- Flexible LED indicators for link, activity, speed, full/half duplex, and collision
- LEDs blink upon reset for LED diagnostics
- Supports two power reduction methods:
  - Power saving mode by cable detection
  - Power down mode (via PHY register 0.11)
- Robust baseline wander correction for improved 100Base-TX performance
- Optional MDI/MDIX auto crossover for plug-and-play
- Physical layer port Polarity Detection and Correction function
- Optional EEPROM interface for configuration
- 25MHz crystal or 3.3V OSC input
- Single 3.3V power input can be transformed to 1.8V via a low-cost external BJT transistor
- Low power, 1.8/3.3V, 0.18µm CMOS technology, 128-pin PQFP package

3. Block Diagram

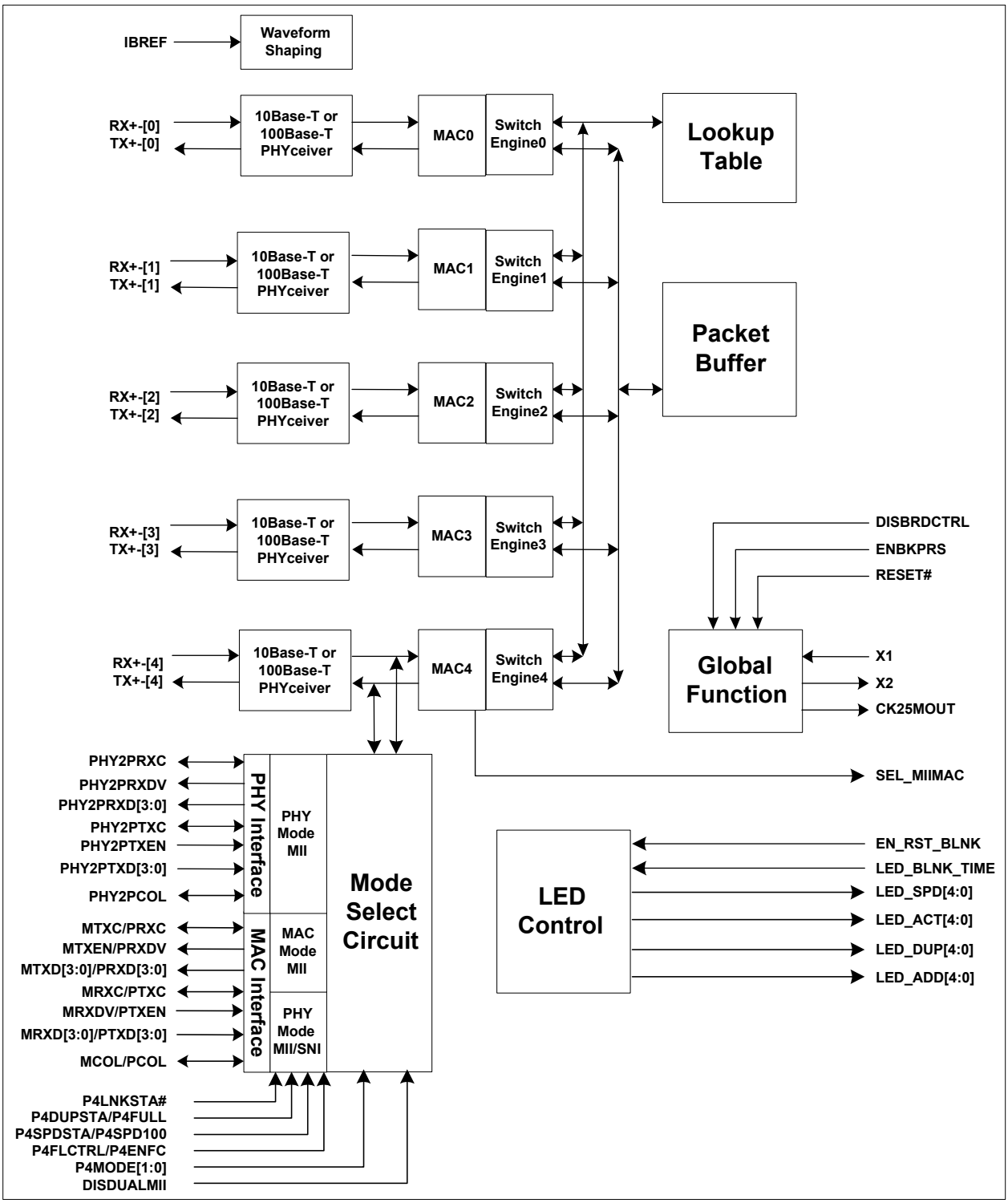


Figure 1. Block Diagram

4. Pin Assignments

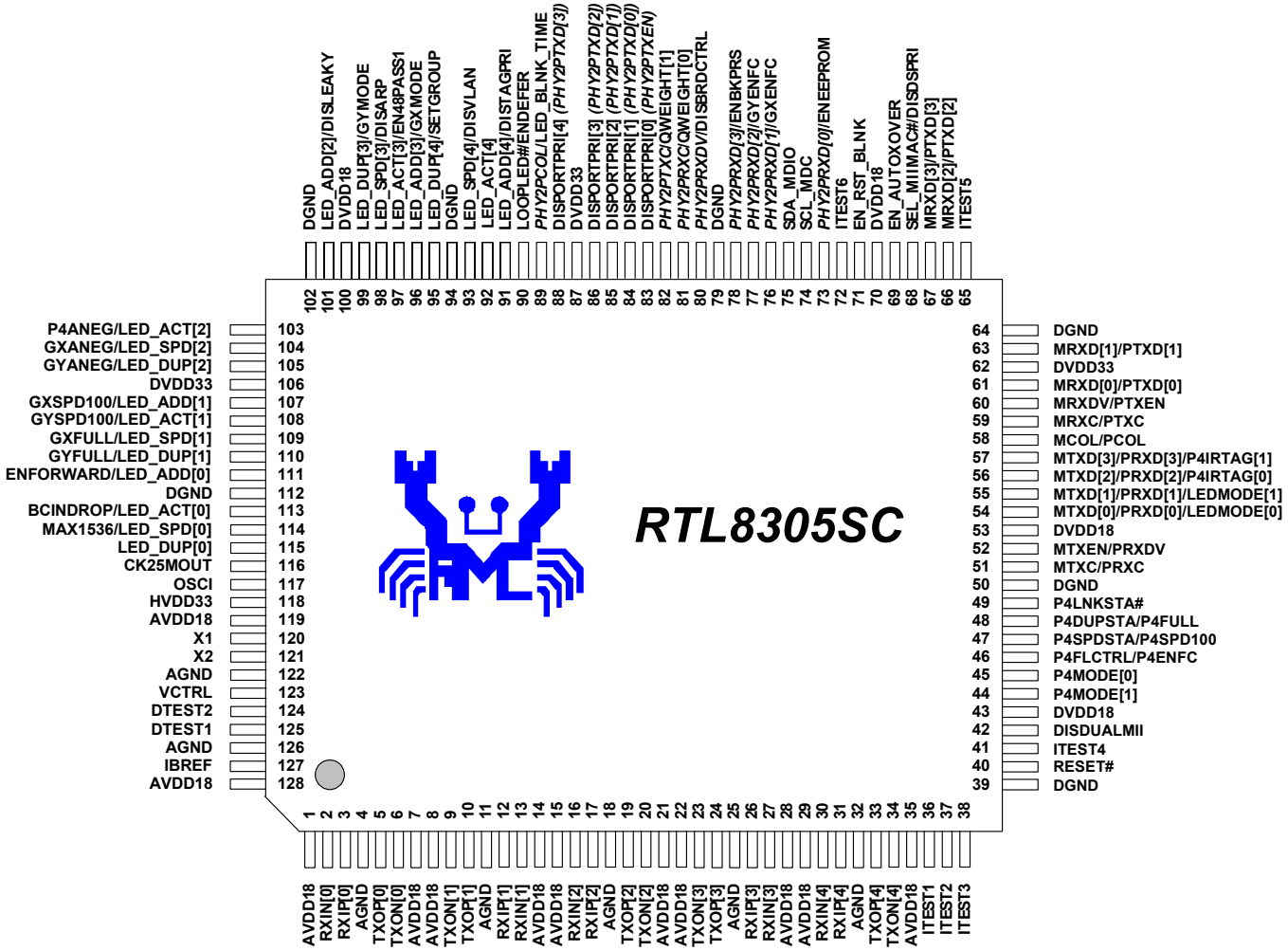


Figure 2. Pin Assignments

Note: When DISDUALMII=1, the function of pins 83~86 and pin 88 follows the names before the parenthesis '( )'.
When DISDUALMII=0, pin names in parenthesis '( )' will become functional and original pin functions will not apply.

'Type' codes used in the following tables: A=Analog; D=Digital, I=Input; O=Output, PU=Internal pull-up, PD=Internal pull-down.

Table 1. Pin Assignments

Name	Pin No.	Type	Name	Pin No.	Type
AVDD18	1	AVDD	ITEST5	65	
RXIN[0]	2	AI	MRXD[2]/PTXD[2]	66	I_{PU}
RXIP[0]	3	AI	MRXD[3]/PTXD[3]	67	I_{PU}
AGND	4	AGND	SEL_MIIMAC#/DISDSPRI	68	I/O_{PU}
TXOP[0]	5	AO	EN_AUTOXOVER	69	I_{PU}
TXON[0]	6	AO	DVDD18	70	DVDD
AVDD18	7	AVDD	EN_RST_BLNK	71	I_{PU}
AVDD18	8	AVDD	ITEST6	72	
TXON[1]	9	AO	PHY2PRXD[0]/ENEEPROM	73	I_{PU}
TXOP[1]	10	AO	SCL_MDC	74	I/O_{PU}
AGND	11	AGND	SDA_MDIO	75	I/O_{PU}
RXIP[1]	12	AI	PHY2PRXD[1]/GXENFC	76	I_{PU}
RXIN[1]	13	AI	PHY2PRXD[2]/GYENFC	77	I_{PU}
AVDD18	14	AVDD	PHY2PRXD[3]/ENBKPRS	78	I_{PU}
AVDD18	15	AVDD	DGND	79	DGND
RXIN[2]	16	AI	PHY2PRXDV/DISBRDCTRL	80	I_{PU}
RXIP[2]	17	AI	PHY2PRXC/QWEIGHT[0]	81	I_{PU}
AGND	18	AGND	PHY2PTXC/QWEIGHT[1]	82	I_{PU}
TXOP[2]	19	AO	DISPORTPRI[0] (***PHY2PTXEN***)	83	I_{PU}
TXON[2]	20	AO	DISPORTPRI[1] (***PHY2PTXD[0]***)	84	I_{PU}
AVDD18	21	AVDD	DISPORTPRI[2] (***PHY2PTXD[1]***)	85	I_{PU}
AVDD18	22	AVDD	DISPORTPRI[3] (***PHY2PTXD[2]***)	86	I_{PU}
TXON[3]	23	AO	DVDD33	87	DVDD
TXOP[3]	24	AO	DISPORTPRI[4] (***PHY2PTXD[3]***)	88	I_{PU}
AGND	25	AGND	PHY2PCOL/LED_BLNK_TIME	89	I_{PU}
RXIP[3]	26	AI	LOOPLED#/ENDEFER	90	I/O_{PU}
RXIN[3]	27	AI	LED_ADD[4]/DISTAGPRI	91	I/O_{PU}
AVDD18	28	AVDD	LED_ACT[4]	92	I/O_{PU}
AVDD18	29	AVDD	LED_SPD[4]/DISVLAN	93	I/O_{PU}
RXIN[4]	30	AI	DGND	94	DGND
RXIP[4]	31	AI	LED_DUP[4]/SETGROUP	95	I/O_{PU}
AGND	32	AGND	LED_ADD[3]/GXMODE	96	I/O_{PU}
TXOP[4]	33	AO	LED_ACT[3]/EN48PASS1	97	I/O_{PU}
TXON[4]	34	AO	LED_SPD[3]/DISARP	98	I/O_{PU}
AVDD18	35	AVDD	LED_DUP[3]/GYMODE	99	I/O_{PU}
ITEST1	36		DVDD18	100	DVDD
ITEST2	37		LED_ADD[2]/DISLEAKY	101	I/O_{PU}
ITEST3	38		DGND	102	DGND
DGND	39	DGND	LED_ACT[2]/P4ANEG	103	I/O_{PU}
RESET#	40	I	LED_SPD[2]/GXANEG	104	I/O_{PU}
ITEST4	41		LED_DUP[2]/GYANEG	105	I/O_{PU}
DISDUALMII	42	I_{PU}	DVDD33	106	DVDD
DVDD18	43	DVDD	LED_ADD[1]/GXSPD100	107	I/O_{PU}
P4MODE[1]	44	I_{PU}	LED_ACT[1]/GYSPD100	108	I/O_{PU}
P4MODE[0]	45	I_{PU}	LED_SPD[1]/GXFULL	109	I/O_{PU}
P4FLCTRL/P4ENFC	46	I_{PU}	LED_DUP[1]/GYFULL	110	I/O_{PU}
P4SPDSTA/P4SPD100	47	I_{PU}	LED_ADD[0]/ENFORWARD	111	I/O_{PU}
P4DUPSTA/P4FULL	48	I_{PU}	DGND	112	DGND
P4LNKSTA#	49	I_{PU}	LED_ACT[0]/BCINDROP	113	I/O_{PU}
DGND	50	DGND	LED_SPD[0]/MAX1536	114	I/O_{PU}
MTXC/PRXC	51	I/O_{PU}	LED_DUP[0]	115	I/O_{PU}
MTXEN/PRXDV/Internal	52	I/O_{PU}	CK25MOUT	116	O
DVDD18	53	DVDD	OSCI	117	I
MTXD[0]/PRXD[0]/LEDMODE[0]	54	I/O_{PU}	HVDD33	118	AVDD
MTXD[1]/PRXD[1]/LEDMODE[1]	55	I/O_{PU}	AVDD18	119	AVDD
MTXD[2]/PRXD[2]/P4IRTAG[0]	56	I/O_{PU}	X1	120	I
MTXD[3]/PRXD[3]/P4IRTAG[1]	57	I/O_{PU}	X2	121	O
MCOL/PCOL	58	I/O_{PD}	AGND	122	AGND
MRXC/PTXC	59	I/O_{PU}	VCTRL	123	O
MRXDV/PTXEN	60	I_{PD}	DTEST2	124	
MRXD[0]/PTXD[0]	61	I_{PU}	DTEST1	125	
DVDD33	62	DVDD	AGND	126	AGND
MRXD[1]/PTXD[1]	63	I_{PU}	IBREF	127	A
DGND	64	DGND	AVDD18	128	AVDD

5. Pin Descriptions

'Type' codes used in the following tables: A=Analog; D=Digital, I=Input; O=Output, PU=Internal pull-up, PD=Internal pull-down.

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

5.1. Media Connection Pins

Table 2. Media Connection Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
RXIP[4:0] RXIN[4:0]	2, 3, 12, 13, 16, 17, 26, 27, 30, 31	I		Differential Receive Data Input Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].
TXOP[4:0] TXON[4:0]	5, 6, 9, 10, 19, 20, 23, 24, 33, 34	O		Differential Transmit Data Output Shared by 100Base-TX, 10Base-T, and 100Base-FX. UTP or FX depends on pin GxMode/GyMode/P4Mode[1:0].

5.2. Port 4 Configuration Pins

Table 3. Port 4 Configuration Pin Definitions

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
DISDUALMII	42	I_{PU}		Disable Dual MII Interface Function This pin disables or enables the Dual MII interface function of port 4. 1: Disable 0: Enable When enabled, the MAC circuit of port 4 can be set as MAC mode MII, PHY mode MII, or PHY mode SNI. The PHY circuit of port 4 is set as PHY mode MII. The PHY circuit of port 4 can optionally be set as UTP or fiber mode according to the P4MOD[1:0] configuration.

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
P4MODE[1:0]	44, 45	I_{PU}		When DISDUALMII=1: Select Port 4 MAC Circuit Operating Mode: 11: UTP/MAC mode MII 10: 100Base-FX mode 01: PHY mode MII 00: PHY mode SNI When DISDUALMII=0, I. Select Port 4 MAC Circuit Operating Mode: 1x: MAC mode MII 01: PHY mode MII 00: PHY mode SNI 11: Port 4 PHY Circuit Operating Mode: *Note: Provides PHY mode MII only when DISDUALMII=0.*
P4LNKSTA#	49	I_{PU}		Port 4 Link Status for MAC This pin determines the link status of the Port 4 MAC in real-time when the Port 4 MAC is in MAC mode MII/PHY mode MII/PHY mode SNI regardless of whether the Port 4 PHY circuit interface is disabled or enabled in PHY mode MII. This pin is low active. Pulling this pin down sets the link status of the PHY 5 MII register to 1.2. 1: No Link 0: Link P4MODE[1:0]=11 and DISDUALMII=1 (UTP/MAC mode MII) This pin determines the link status of MAC mode MII only in real time. The link status of UTP mode is provided by the internal PHY in real time. If both the UTP and MII ports are linked OK, UTP has higher priority. P4MODE[1:0]=11 and DISDUALMII=0 (MAC mode MII) This pin determines the link status of MAC mode MII only in real time. P4MODE[1:0]=10 (100Base-FX mode) This pin does nothing. The internal PHY will provide the link status to the MAC in real time. P4MODE[1:0]=01 (PHY mode MII) This pin determines the link status of Port 4 in real time. P4MODE[1:0]=00 (PHY mode SNI) This pin determines the link status of Port 4 in real time. When DISDUALMII=1, this pin should be left floating in UTP or FX mode, and pulled down in MAC mode MII/PHY mode MII/PHY mode SNI. Regardless of whether DISDUALMII=1 or=0, this pin provides the link status to the Port 4 MAC part in PHY 5 MII register 1.2 when the Port 4 MAC part is configured in MAC mode MII/PHY mode MII/PHY mode SNI.

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
P4DUPSTA	48	I_{PU}		Port 4 Duplex Status Port 4 initial configuration pin for duplex upon reset for PHY in UTP or FX mode, and strap duplex status for MAC of other modes upon reset. 1: Full duplex 0: Half duplex P4MODE[1:0]=11 (UTP/MAC mode MII) This pin provides the initial duplex configuration of the PHY part upon reset when Port 4 operates in UTP mode. If Port 4 operates in MAC mode MII, this pin straps the initial duplex status for the MAC part upon reset. P4MODE[1:0]=10 (100Base-FX mode) This pin provides the initial duplex register configuration of the PHY part upon reset (FX). The duplex status of the MAC part is provided by the internal PHY in real time after reset. P4MODE[1:0]=01 (PHY mode MII) This pin straps the initial duplex status of Port 4 upon reset. P4MODE[1:0]=00 (PHY mode SNI) This pin straps the initial duplex status of Port 4 upon reset. In MAC mode MII/PHY mode MII/PHY mode SNI, the configuration of this pin will set the duplex status of the internal register upon reset.

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
P4SPDSTA	47	I_{PU}		Port 4 Speed Status Port 4 initial configuration pin for speed status upon reset for PHY of UTP mode only, and strap speed status for MAC of other modes upon reset. 1: 100Mbps 0: 10Mbps P4MODE[1:0]=11 (UTP/MAC mode MII) This pin provides the initial speed configuration of the PHY part upon reset when Port 4 operates in UTP mode. If Port 4 operates in MAC mode MII, this pin straps the initial speed status for the MAC part upon reset. P4MODE[1:0]=10 (100Base-FX mode) The speed is dedicated to 100M and this pin should be left floating as it is irrelevant. P4MODE[1:0]=01 (PHY mode MII) This pin straps the initial speed status of Port 4 upon reset. P4MODE[1:0]=00 (PHY mode SNI) The speed is dedicated to 10MHz. This pin should be pulled down. In order to provide 100M as the default value for PHY, this pin is set as high active.

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
P4FLCTRL/ P4EnFC	46	I_{PU}		Port 4 Flow Control Port 4 initial configuration pin for flow control upon reset for PHY of UTP and FX mode, and strap flow control status for MAC of other modes upon reset. 1: Enable Flow Control ability 0: Disable Flow Control ability P4MODE[1:0]=11 (UTP/MAC mode MII) This pin provides the initial flow control configuration of the PHY part upon reset when Port 4 operates in UTP mode. If Port 4 operates in MAC mode MII, this pin straps the initial flow control status for the MAC part upon reset. P4MODE[1:0]=10 (100Base-FX mode) This pin provides the initial configuration of flow control for the PHY part upon reset (FX). P4MODE[1:0]=01 (PHY mode MII) This pin straps the initial flow control status of Port 4 upon reset. P4MODE[1:0]=00 (PHY mode SNI) Flow control should be disabled. This pin must be pulled down. In order to enable flow control ability for the PHY, this pin is set as high active.

Pin Name	Pin No.	Type	Drive (mA)	Description
Port 4 Configuration Pin Definitions				
SEL_MIIMAC#/ DisDSPri /(P4PHY_ MODE)	68	I/O_{PU}	4	Output After Reset = SEL_MIIMAC# used for LED When P4MODE[1:0]=11 and DISDUALMII=1, this pin indicates whether the UTP path or the MII MAC path is selected. Otherwise, this pin has no use. The LED statuses are represented as active-low or high depending on input strapping If Input=1: Output 0=MII MAC port is selected. 1=UTP is selected. If Input=0: Output 1=MII MAC port is selected. 0=UTP is selected. When P4MODE[1:0]=11 and DISDUALMII=1, the RTL8305SC supports UTP/MII MAC auto-detection function via the link status of Port 4 UTP and the P4LNKSTA# pin setting. UTP has higher priority than MAC mode MII. Input Upon Reset when DISDUALMII=1, DisDSPri. Disable Differentiated Service Priority. 1: Disable DS priority 0: Enable DS priority Input Upon Reset when DISDUALMII=0, P4PHY_MODE. Select the operating mode of Port 4 differential pair. 1: UTP mode 0: FX mode

5.3. Port 4 MAC Circuit Interface Pins

The external device must be 3.3V compatible since the digital output of the RTL8305SC is 3.3V.

Table 4. Port 4 MAC Circuit Interface Pin Definitions

Pin Name	Pin No.	Type	Drive (mA)	Description
MRXD[3:0]/ PTXD[3:0]	61, 63, 66, 67	I_{PU}		For MAC mode MII, these pins are MRXD[3:0], MII receive data nibble. For PHY mode MII, these pins are PTXD[3:0], MII transmit data nibble. For PHY mode SNI, PTXD[0] is serial transmit data.
MRXDV/PTXEN	60	I_{PD}		For MAC mode MII, this pin represents MRXDV, MII receive data valid. For PHY mode MII, this pin represents PTXEN, MII transmit enable. For PHY mode SNI, this pin represents PTXEN, transmit enable.
MRXC/PTXC	59	I/O_{PU}	8	For MAC mode MII, this is a receive clock (MRXC acts as input). For PHY mode MII/PHY mode SNI, it is a transmit clock (PTXC acts as output).

Pin Name	Pin No.	Type	Drive (mA)	Description
MCOL/PCOL	58	I/O_{PD}	4	For MAC mode MII, this pin represents MCOL collision (acts as input). For PHY mode MII/PHY mode SNI, this pin represents PCOL collision (acts as output).
MTXD[3]/PRXD[3] /P4IRTag[1] MTXD[2]/PRXD[2] /P4IRTag[0]	57 56	I/O_{PU}	4	Output After Reset. For MAC mode MII (P4MODE[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC. For PHY mode MII (P4MODE[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY. For PHY mode SNI (P4MODE[1:0]=00), PRXD[0] is SNI serial receive data. Input Upon Reset: P4IRTag[1:0] Insert/Remove VLAN tags of Port 4. 11=Do not insert/remove VLAN tags to/from packets. 10=Insert VLAN tags to non-tagged packets. 01=Remove tag from tagged packet. 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets. These pins are used for Port 4 only. Use serial EEPROM for other ports.
MTXD[1]/PRXD[1] /LEDMODE[1] MTXD[0]/PRXD[0] /LEDMODE[0]	55 54	I/O_{PU}	4	Output After Reset. For MAC mode MII (P4MODE[1:0]=11), these pins are MTXD[3:0], MII transmit data of MAC. For PHY mode MII (P4MODE[1:0]=01), these pins are PRXD[3:0], MII receive data of PHY. For PHY mode SNI (P4MODE[1:0]=00), PRXD[0] is SNI serial receive data. Input Upon Reset: LEDMODE[1:0] Each port has four LED indicator pins. Each pin has different indicator meanings set by pins, LEDMODE[1:0]. LEDMODE[1:0]=11: Speed + Link/Act + Duplex/Col + Link/Act/Spd. LEDMODE[1:0]=10: Speed + Act + Duplex/Col+Bi-color Link/Active. LEDMODE[1:0]=01: Speed + RxAct + TxAct + Link. LEDMODE[1:0]=00: Reserved. All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status. Link/Act/Spd: Link, Activity, and Speed Indicator. ON for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps.

Pin Name	Pin No.	Type	Drive (mA)	Description
MTXEN/PRXDV /Internal	52	I/O_{PD}	4	Output After Reset. For MAC mode MII, this pin represents MTXEN, MII transmit enable. For PHY mode MII, this pin represents PRXDV, MII received data valid. For PHY mode SNI, this pin represents PRXDV, received data valid. Input Upon Reset. Internal Use
MTXC/PRXC	51	I/O_{PU}	8	For MAC mode MII, it is a transmit clock (MTXC acts as input). For PHY mode MII/PHY mode SNI, it is a receive clock (PRXC acts as output).

5.4. Port 4 PHY Circuit Interface Pins

The external device must be 3.3V compatible as the digital output of the RTL8305SC is 3.3V.

Table 5. Port 4 PHY Circuit Interface Pin Definitions

Pin Name	Pin No.	Type	Drive (mA)	Description
DISPORTPRI[4] (PHY2PTXD[3])	88	I_{PU}	-	DISDUALMII=1, Enable Port based priority QoS function of port 4. DisPortPri[4]: 1=Disable port 4 priority. 0=Enable port 4 priority. DISDUALMII=0, PHY mode MII Transmit Data Nibble. For PHY mode MII, this pin is PHY2PTXD[3]. DISPORTPRI[4] power on strapping is not supported when DISDUALMII=0. This configuration can be set from the MII register.
DISPORTPRI[3] (PHY2PTXD[2])	86	I_{PU}	-	DISDUALMII=1, Enable Port based priority QoS function of port 3. DisPortPri[3]: 1=Disable port 3 priority. 0=Enable port 3 priority. DISDUALMII=0, PHY mode MII Transmit Data Nibble. For PHY mode MII, this pin is PHY2PTXD[2]. DISPORTPRI[3] power on strapping is not supported when DISDUALMII=0. This configuration can be set from the MII register.
DISPORTPRI[2] (PHY2PTXD[1])	85	I_{PU}	-	DISDUALMII=1, Enable Port based priority QoS function of port 2. DisPortPri[2]: 1=Disable port 2 priority. 0=Enable port 2 priority. DISDUALMII=0, PHY mode MII Transmit Data Nibble. For PHY mode MII, this pin is PHY2PTXD[1]. DISPORTPRI[2] power on strapping is not supported when DISDUALMII=0. This configuration can be set from the MII register.

Pin Name	Pin No.	Type	Drive (mA)	Description
DISPORTPRI[1] (PHY2PTXD[0])	84	I_{PU}	-	DISDUALMII=1, Enable Port based priority QoS function of port 1. DisPortPri[1]: 1=Disable port 1 priority. 0=Enable port 1 priority. DISDUALMII=0, PHY mode MII Transmit Data Nibble. For PHY mode MII, this pin is PHY2PTXD[0]. DISPORTPRI[1] power on strapping is not supported when DISDUALMII=0. This configuration can be set from the MII register.
DISPORTPRI[0] (PHY2PTXEN)	83	I_{PU}	-	DISDUALMII=1, Enable Port based priority QoS function of port 0. DisPortPri[0]: 1=Disable port 0 priority. 0: Enable port 0 priority. DISDUALMII=0, PHY mode MII Transmit Data Enable. For PHY mode MII, this pin is PHY2PTXEN. DISPORTPRI[0] power on strapping is not supported when DISDUALMII=0. This configuration can be set from the MII register. For Dual MII application, this pin should be pulled low (about 1k ohm) in the external circuit.
PHY2PCOL /LED_BLNK_ TIME	89	I/O_{PU}	4	Output After Reset: DISDUALMII=0, PHY mode MII PCOL. For PHY mode MII, this pin represents PCOL collision (acts as output). Input Upon Reset: LED Blink Time. This pin selects the blinking speed of the activity and collision LEDs. 1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms Power on strapping is independent of DISDUALMII configuration.
PHY2PTXC /QWEIGHT[1] PHY2PRXC /QWEIGHT[0]	82 81	I/O_{PU}	8	Output After Reset: DISDUALMII=0, PHY mode MII Transmit/ Receive Data Clock. For PHY mode MII, this is transmit/receive data clock, PTXC/PRXC (acts as output). Input Upon Reset: Weighted round robin ratio of priority queue. The frame service rate of High-priority queue: Low-priority queue QWEIGHT[1:0]=11: 16:1 QWEIGHT[1:0]=10: Always high priority queue first QWEIGHT[1:0]=01: 8:1 QWEIGHT[1:0]=00: 4:1 Power on strapping is independent of DISDUALMII configuration.

Pin Name	Pin No.	Type	Drive (mA)	Description
PHY2PRXD[3] /ENBKPRS	78	I/O_{PU}	4	Output After Reset: DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output). For PHY mode MII, this pin is PHY2PRXD[3]. Input Upon Reset: Enable Back Pressure. This pin sets back pressure in half duplex mode on all UTP ports. 1: Enable 0: Disable Power on strapping is independent of DISDUALMII configuration.
PHY2PRXD[2] /GYENFC	77	I/O_{PU}	4	Output After Reset: DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output). For PHY mode MII, this pin is PHY2PRXD[2]. Input Upon Reset: GroupY Enable Flow Control ability. 1: Enable Reg4.10 (NWAY Full duplex only), or 'Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)', or 'Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)' 0: Disable Reg4.10 (NWAY Full duplex only), or 'Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)', or 'Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)' Strap after reset for initial value of Group Y 'UTP NWAY Full', or 'UTP Force Full or Half mode', or 'FX Full or Half mode'. Power on strapping is independent of DISDUALMII configuration.
PHY2PRXD[1] /GXENFC	76	I/O_{PU}	4	Output After Reset: DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output). For PHY mode MII, this pin is PHY2PRXD[1]. Input Upon Reset: GroupX Enable Flow Control ability: 1: Enable Reg4.10 (NWAY Full duplex only), or 'Enable Force Full pause ability of Force mode (UTP Force mode or FX mode)', or 'Enable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)' 0: Disable Reg4.10 (NWAY Full duplex only), or 'Disable Force Full pause ability of Force mode (UTP Force mode or FX mode)', or 'Disable Force Half Back Pressure ability of Force mode (UTP Force mode or FX mode)' Strap after reset for initial value of Group X 'UTP NWAY Full', or 'UTP Force Full or Half mode', or 'FX Full or Half mode'. Power on strapping is independent of DISDUALMII configuration.

Pin Name	Pin No.	Type	Drive (mA)	Description
PHY2PRXD[0] /ENEEPROM	73	I/O_{PU}	4	DISDUALMII=0, PHY mode MII Receive Data Nibble (acts as output). For PHY mode MII, this pin is PHY2PRXD[0]. Enable EEPROM: This pin sets the RTL8305SC to enable loading of the serial EEPROM upon reset. 1: Enable 0: Disable These pins have internal 75k ohm pull-high resistors. Power on strapping is independent of DISDUALMII configuration.
PHY2PRXDV /DISBRDCTRL	80	I/O_{PU}	4	DISDUALMII=0, PHY mode MII Receive Data Valid. For PHY mode MII, this pin represents PRXDV. Disable Broadcast Storm Control. 1: Disable 0: Enable The RTL8305SC will disable this function when pin DISBRDCTRL is left floating. This pin has an internal 75k ohm pull-high resistor. Power on strapping is independent of DISDUALMII configuration.

5.5. Miscellaneous Pins

Table 6. Miscellaneous Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
X1	120	I		A 25MHz crystal input The clock tolerance is +-50ppm. When using an oscillator, this pin should be tied to ground.
X2	121	O		For crystal input When using an oscillator, this pin should be left floating.
OSCI	117	I		A 25MHz clock from oscillator is fed to this pin The X1 should be tied to ground and X2 should be left floating in this application. If a 25MHz clock is from crystal via X1 and X2, this pin should be left floating.
CK25MOUT	116	O	8	A 25MHz clock output This pin is used to support an extra 25M clock for an external device (for example: HomePNA PHY). If this clock output is not used, this pin should be left floating.
RESET#	40	I		Active low reset signal To complete the reset function, this pin must be asserted for at least 1ms. After reset, about 30ms is needed for the RTL8305SC to complete internal test functions and initialization. This pin is a Schmitt input.

Pin Name	Pin No.	Type	Drive (mA)	Description
IBREF	127	A		Control transmit output waveform Vpp This pin should be grounded through a 1.96KΩ resistor.
VCTRL	123	O	4	Voltage control to external regulator This signal controls a power PNP transistor to generate the 1.8V power supply.
ITEST1	36			Reserved pin for internal use. Should be left floating
ITEST2	37			Reserved pin for internal use. Should be left floating
ITEST3	38			Reserved pin for internal use. Should be left floating
ITEST4	41			Reserved pin for internal use. Should be left floating
ITEST5	65			Reserved pin for internal use. Should be left floating
ITEST6	72			Reserved pin for internal use. Should be left floating
DTEST2	124			Reserved pin for internal use. Should be left floating
DTEST1	125			Reserved pin for internal use. Should be left floating

5.6. Port LED Pins

Each port has four LED indicator pins. Each pin may have different indicator meanings as set by pins LEDMODE[1:0].

All LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status.

Those pins that are dual function pins are output for LED or input for strapping. Below are LED descriptions only.

Table 7. Port LED Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_SPD[4:0]/…	93, 98, 104, 109, 114	I/O_{PU}	4	Output After Reset = Used for 1st LED. LEDMode[1:0]=11 -> Speed (On=100, Off=10) LEDMode[1:0]=10 -> Speed (On=100, Off=10) LEDMode[1:0]=01 -> Speed (On=100, Off=10) LEDMode[1:0]=00 -> Reserved Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LED_ACT[4:0]/…	92, 97, 103, 108, 113	I/O_{PU}	4	Output After Reset = Used for 2nd LED. LEDMode[1:0]=11 -> Link/Act: (On=Link, Off=No Link, Flash=Tx or Rx activity) LEDMode[1:0]=10 -> Act: (Off=No activity, On=Tx or Rx activity) LEDMode[1:0]=01 -> RxAct: (Off=No activity, On=Rx activity) LEDMode[1:0]=00 -> Reserved Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.

Pin Name	Pin No.	Type	Drive (mA)	Description
LED_DUP[4:0]/…	95, 99, 105, 110, 115	I/O_{PU}	4	Output After Reset = Used for 3rd LED. LEDMode[1:0]=11 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=10 -> Duplex/Col: (On=Full, Off=Half with no collision, Flash=Collision) LEDMode[1:0]=01 -> TxAct: (Off=No activity, On=Tx activity) LEDMode[1:0]=00 -> Reserved Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LED_ADD[4:0]/..	91, 96, 101, 107, 111	I/O_{PU}	4	Output After Reset = Used for 4th LED. LEDMode[1:0]=11 -> Link/Act/Spd: On for link established. Blinking every 43ms when the corresponding port is transmitting or receiving at 100Mbps. Blinking every 120ms when the port is transmitting or receiving at 10Mbps. LEDMode[1:0]=10 -> Bi-color Link/Active: polarity depends on Spd status. LEDMode[1:0]=01 -> Link: (On=Link, Off=No Link) LEDMode[1:0]=00 -> Reserved Input Upon Reset = Refer to Table 9, on page 22, and Table 10, on page 24.
LoopLED# /EnDefer	90	I/O_{PU}	4	Output After Reset = LoopLED# used for LED. If the Loop detection function is enabled, this pin indicates whether a Network loop is detected or not. Otherwise, this pin is of no use. The LED statuses are represented as active-low or high depending on input strapping. => If Input=1: Output 0=Network loop is detected. 1=No loop. => If Input=0: Output 1=Network loop is detected. 0=No loop. Input Upon Reset = Enable defer 1: Enable Carrier Sense Deferring function for half duplex back pressure. 0: Disable Carrier Sense Deferring function for half duplex back pressure.

5.7. Serial EEPROM and SMI Pins

As the output of the RTL8305SC is 3.3V, the serial EEPROM and external device must be 3.3V compatible.

Table 8. Serial EEPROM and SMI Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SCL_MDC	74	I/O_{PU}	4	SCL or MDC This pin is tri state when pin RESET#=0. When pin EnEEPROM=1, this pin becomes SCL (output) to load the serial EEPROM upon reset. Then this pin changes to MDC (input) after reset. When pin EnEEPROM=0, this pin is MDC (input): 0 to 25MHz clock, sourced by an external device to sample MDIO.
SDA_MDIO	75	I/O_{PU}	4	SDA or MDIO This pin is tri state when RESET#=0. When pin EnEEPROM=1, this pin becomes SDA (input/output) to load the serial EEPROM upon reset. Then this pin changes to MDIO (input/output) after reset. It should be pulled-high by an external resistor. When pin EnEEPROM=0, this pin is MDIO (input/output). It should be pulled-high by an external resistor.

5.8. Strapping Pins

Pins that are dual function pins are outputs for LED or inputs for strapping. Below are strapping descriptions only.

Table 9. Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
EN_AUTOXOVER	69	I_{PU}		Enable Auto crossover function 1: Enable auto crossover detection 0: Disable auto crossover detection. MDI only
EN_RST_BLNK	71	I_{PU}		Enable Reset Blink This enables blinking of the LEDs upon reset for diagnostic purposes. 1: Enable reset LED blinking 0: Disable reset LED blinking
DisTagPri /LED_ADD[4]	91	I/O_{PU}	4	Input Upon Reset = Disable 802.1p VLAN Tag priority based QoS function. 1: Disable 0: Enable Output After Reset = Used for LED.

Pin Name	Pin No.	Type	Drive (mA)	Description
DISVLAN /LED_SPD[4]	93	I/O_{PU}	4	Input Upon Reset = Disable VLAN function 1: Disable VLAN 0: Enable VLAN. The default VLAN membership configuration by internal register is port 4 overlapped with all the other ports, to form 4 individual VLANs. This default membership configuration may be modified by setup internal registers via the SMI interface or EEPROM Output After Reset = Used for LED.
En48pass1 /LED_ACT[3]	97	I/O_{PU}	4	Input Upon Reset = Enable 48 pass 1 1: 48 pass 1, continuously collides 48 input packets then passes 1 packet to retain system resource and avoid the partition in repeater when the packet buffer in 8305SC is full 0: Continuously collides to avoid packet loss when the packet buffer in 8305SC is full Output After Reset = Used for LED.
DisARP /LED_SPD[3]	98	I/O_{PU}	4	Input Upon Reset = Disable ARP broadcast to all VLANs 1: Disables ability to broadcast ARP broadcast packets to all VLANs 0: Enables ability to broadcast ARP broadcast packets to all VLANs ARP broadcast frame: DID is all F. Output After Reset = Used for LED.
DisLeaky /LED_ADD[2]	101	I/O_{PU}	4	Input Upon Reset = Disable Leaky VLAN 1: Disable forwarding of unicast frames to other VLANs 0: Enable forwarding of unicast frames to other VLANs Broadcast and multicast frames adhere to the VLAN configuration. Output After Reset = Used for LED.
EnForward /LED_ADD[0]	111	I/O_{PU}	4	Input Upon Reset = Enable to forward 802.1D specified reserved multicast addresses frame 1: Forward reserved control frames, with DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F 0: Filter reserved control packets, with DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F Output After Reset = Used for LED.
BCInDrop /LED_ACT[0]	113	I/O_{PU}	4	Input Upon Reset = Broadcast Input Drop 1: Use Broadcast Input drop mechanism 0: Use Broadcast Output drop mechanism Output After Reset = Used for LED.
Max1536 /LED_SPD[0]	114	I/O_{PU}	4	Input Upon Reset = Maximum Frame Length 1: 1536 Bytes 0: 1552 Bytes Output After Reset = Used for LED.

5.9. Port Status Strapping Pins

Pins that are dual function pins are outputs for LEDs or inputs for strapping. Below are strapping descriptions only.

Table 10. Port Status Strapping Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
SetGroup /LED_DUP[4]	95	I/O_{PU}	4	Input Upon Reset = Set group of port 1 1: Port 0 is group X. Port 1, 2, and 3 are group Y 0: Port 0, and 1 are group X. Port 2, and 3 are group Y Output After Reset = Used for LED.
GxMode /LED_ADD[3]	96	I/O_{PU}	4	Input Upon Reset = Group X operating mode 1: UTP mode 0: FX mode Output After Reset = Used for LED.
GyMode /LED_DUP[3]	99	I/O_{PU}	4	Input Upon Reset = Group Y operating mode 1: UTP mode 0: FX mode Output After Reset = Used for LED.
P4ANEG /LED_ACT[2]	103	I/O_{PU}	4	Input Upon Reset = Port 4 Auto-Negotiation ability 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Port 4. Strap after reset for initial value of Port 4 UTP mode only. This pin is not used for Port 4 FX, MAC mode MII, PHY mode MII, and PHY mode SNI. Output After Reset = Used for LED.
GxANEG /LED_SPD[2]	104	I/O_{PU}	4	Input Upon Reset = GroupX Auto-Negotiation ability 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group X. Strap after reset for initial value of UTP mode only. This pin is not used for FX. Output After Reset = Used for LED.
GyANEG /LED_DUP[2]	105	I/O_{PU}	4	Input Upon Reset = GroupY Auto-Negotiation ability 1: Enable auto-negotiation (NWAY mode) 0: Disable auto-negotiation (Force mode) Upon reset, this pin sets Reg.0.12 of Group Y. Strap after reset for initial value of UTP mode only. This pin is not used for FX. Output After Reset = Used for LED.

Pin Name	Pin No.	Type	Drive (mA)	Description
GxSpd100 /LED_ADD[1]	107	I/O_{PU}	4	Input Upon Reset = GroupX 10Base-T/100Base-TX ability GxSpd100=1, GxFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GxSpd100=1, GxFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GxSpd100=0, GxFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GxSpd100=0, GxFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GxFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group X UTP mode only. This pin is not used for FX. Output After Reset = Used for LED.
GySpd100 /LED_ACT[1]	108	I/O_{PU}	4	Input Upon Reset = GroupY 10Base-T/100Base-TX ability GySpd100=1, GyFull=1 => MII Reg0.13=1, 0.8=1, 4.8=1, 4.7=1, 4.6=1, 4.5=1 GySpd100=1, GyFull=0 => MII Reg0.13=1, 0.8=0, 4.8=0, 4.7=1, 4.6=1, 4.5=1 GySpd100=0, GyFull=1; => MII Reg0.13=0, 0.8=1, 4.8=0, 4.7=0, 4.6=1, 4.5=1 GySpd100=0, GyFull=0; => MII Reg0.13=0, 0.8=0, 4.8=0, 4.7=0, 4.6=0, 4.5=1 Upon reset, this pin sets Reg.0.13. In addition, upon reset, this pin and GyFull also sets Reg.4.8/4.7/4.6/4.5. Strap after reset for initial value of Group Y UTP mode only. This pin is not used for FX. Output After Reset = Used for LED.
GxFull /LED_SPD[1]	109	I/O_{PU}	4	Input Upon Reset = GroupX Full Duplex ability Upon reset, this pin sets the default value of Reg.0.8. In addition, on reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group X UTP or FX mode. FX can be Force 100 Full or Force 100 Half. Output After Reset = Used for LED.
GyFull /LED_DUP[1]	110	I/O_{PU}	4	Input Upon Reset = GroupY Full Duplex ability Upon reset, this pin sets the default value of Reg.0.8. On reset, this pin also sets NWay full-duplex ability on Reg.4.8 and Reg.4.6. Strap after reset for initial value of Group Y UTP or FX mode. FX can be Force 100 Full or Force 100 Half. Output After Reset = Used for LED.

5.10. Power Pins

Table 11. Power Pins

Pin Name	Pin No.	Type	Drive (mA)	Description
AVDD18	1, 7, 8, 14, 15, 21, 22, 28, 29, 35, 119, 128	P		1.8V Analog Power
HVDD33	118	P		3.3V Analog Power
AGND	4, 11, 18, 25, 32, 122, 126	P		Analog Ground
DVDD18	43, 53, 70, 100	P		1.8V Digital Power
DVDD33	62, 87, 106	P		3.3V Digital Power
DGND	39, 50, 64, 79, 94, 102, 112	P		Digital Ground

6. EEPROM Description

6.1. Port 0 Registers

6.1.1. Global Control Register0

Table 12. Global Control Register0

Name	Byte.bit	Description	Default
EEPROM Existence	0.7	1: EEPROM does not exist (pin EnEEPROM=0 or pin EnEEPROM=1 but EEPROM does not exist) 0: EEPROM exists (pin EnEEPROM=1 and EEPROM exists)	0
Reserved	0.6		1
Internal Use	0.5		1
Internal Use	0.4		1
Internal Use	0.3		1
Enable Loop Detection Function	0.2	1: Enable loop detection function 0: Disable loop detection function	0
Reserved	0.1		1
Internal Use	0.0		0

6.1.2. Global Control Register1

Table 13. Global Control Register1

Name	Byte.bit	Description	Default
Page selection	1.7	1: Select the registers in page 1 0: Select the registers in page 0	0
Reserved	1.6		0
Lookup table accessible enable	1.5	1: Lookup table is accessible via indirect access registers 0: Lookup table is not accessible	0
Internal Use	1.4		0
Reserved	1.3		0
Disable 802.1Q tag aware VLAN	1.2	1: Disable 802.1Q tagged-VID Aware function. The RTL8305SC will not check the tagged VID on received frames to perform tagged-VID VLAN mapping. Under this configuration, the RTL8305SC only uses the per port VLAN index register to perform Port-Based VLAN mapping 0: Enable the Member Set Filtering function of VLAN Ingress Rule. The RTL8305SC checks the tagged VID on received frames with the VIDA[11:0]~VIDH[11:0] to index to a member set, then performs VLAN mapping. The RTL8305SC uses tagged-VID VLAN mapping for tagged frames but still uses Port-Based VLAN mapping for priority-tagged and untagged frames	1

Name	Byte.bit	Description	Default
Disable VLAN member set ingress filtering	1.1	1: The switch will not drop the received frame if the ingress port of this packet is not included in the matched VLAN member set. It will still forward the packet to the VLAN members specified in the matched member set. This setting works on both port-based and tag-based VLAN configurations 0: The switch will drop the received frame if the ingress port of this packet is not included in the matched VLAN member set	1
Disable VLAN tag admit control	1.0	1: The switch accepts all frames it receives whether tagged or untagged. 0: The switch will only accept tagged frames and will drop untagged frames.	1

6.1.3. Global Control Register2

Table 14. Global Control Register2

Name	Byte.bit	Description	Default
Internal Use	2.7		0
Internal Use	2.6		0
Internal Use	2.5~2.0		11 1111

6.1.4. Global Control Register3

Table 15. Global Control Register3

Name	Byte.bit	Description	Default
Internal Use	3.7		0
Internal Use	3.6		0
Internal Use	3.5~3.0		11 1111

6.1.5. Global Control Register4

Table 16. Global Control Register4

Name	Byte.bit	Description	Default
Reserved	4.7		1
Enable defer	4.6	1: Enable carrier sense deferring for half duplex back pressure 0: Disable carrier sense deferring for half duplex back pressure	1
LED blink time	4.5	1: On 43ms, then Off 43ms 0: On 120ms, then Off 120ms	1
Queue weight	4.4~4.3	The frame service ratio between the high priority queue and low priority queue is: 11=16:1 10=Always high priority queue first 01=8:1 00=4:1	11
Disable broadcast storm control	4.2	1: Disable Broadcast Storm Control 0: Enable Broadcast Storm Control	1

Name	Byte.bit	Description	Default
Enable power-on blinking	4.1	1: Enable power-on LED blinking for diagnosis 0: Disable power-on LED blinking for diagnosis	1
Reserved	4.0		1

6.1.6. Global Control Register5

Table 17. Global Control Register5

Name	Byte.bit	Description	Default
Reserved	5.7		1
Maximum Frame Length	5.6	1: 1536 Byte 0: 1552 Byte	1
Enable broadcast drop	5.5	1: Use Broadcast Input drop mechanism 0: Use Broadcast Output drop mechanism	1
Forward 802.1D reserved MAC addresses frame.	5.4	1: Forward reserved control frames, which DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F packets 0: Filter reserved control packets, which DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F	1
Disable leaky VLAN	5.3	1: Disable forwarding of unicast frames to other VLANs 0: Enable forwarding of unicast frames to other VLANs Broadcast and multicast frames adhere to the VLAN configuration.	1
Disable ARP VLAN	5.2	1: Disable to broadcast the ARP broadcast packet to all VLANs 0: Enable to broadcast the ARP broadcast packet to all VLANs ARP broadcast frame: DID is all F.	1
Enable 48 pass 1	5.1	1: 48 pass 1, continuously collides 48 input packets then passes 1 packet to retain system resource and avoid partition in the repeater when the packet buffer is full 0: Continuously collides to avoid packet loss when the packet buffer is full	1
Disable VLAN	5.0	1: Disable VLAN 0: Enable VLAN. The default VLAN membership configuration by internal register is port 4 overlapped with all the other ports, to form 4 individual VLANs. This default membership configuration may be modified by setup internal registers via the SMI interface or EEPROM	1

6.1.7. Global Control Register6

Table 18. Global Control Register6

Name	Byte.bit	Description	Default
Reserved	6.7~6.0		1111 1111

6.1.8. Global Control Register7

Table 19. Global Control Register 7

Name	Byte.bit	Description	Default
Reserved	7.7~7.6		11
LED Mode[1:0]	7.5~7.4	11=Mode 3: Speed, Link+Act, Duplex+Col, Link/Act/Speed 10=Mode 2: Speed, Act, Duplex/Col, Bi-color Link/Activity 01=Mode 1: Speed, RxAct, TxAct, Link 00=Mode 0: Reserved	11
Internal Use	7.3		1
Disable dual MII interface of port 4	7.2	1: Disable dual MII interface of port 4. Only provides MII interface for the MAC circuit of port 4 0: Enable dual MII interface of port 4. Not only provides MII interface for the MAC circuit of port 4 but provides MII interface for the PHY circuit of port 4	1
Reserved	7.1~7.0		11

6.1.9. Port 0 Control 0

Table 20. Port 0 Control 0

Name	Byte.bit	Description	Default
Reserved	8.7		0
Internal Use	8.6		1
Internal Use	8.5~8.4		11
Internal Use	8.3		1
Internal Use	8.2		1
VLAN tag insert and remove	8.1~8.0	For port 0 egress packets 11=Do not insert or remove VLAN tags to/from packet 10=Insert VLAN tags to non-tagged packets 01=Remove tag from tagged packets 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets	11

6.1.10. Port 0 Control 1

Table 21. Port 0 Control 1

Name	Byte.bit	Description	Default
Reserved	9.7		1
Internal Use	9.6		0
Local loopback	9.5	1: Perform 'local loopback', i.e. loopback MAC's RX back to TX 0: Normal operation	0
Internal Use	9.4		0
Discard Non PVID packets	9.3	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID 0: No packets will be dropped	0
Disable 802.1p priority	9.2	1: Disable 802.1p priority classification for ingress packets on port 0 0: Enable 802.1p priority classification on port 0	1
Disable Diffserv priority	9.1	1: Disable Diffserv priority classification for ingress packets on port 0 0: Enable Diffserv priority classification	1
Disable port-based priority on port 0	9.0	1: Disable port based priority QoS function on port 0 0: Enable port based priority QoS function on port 0. Ingress packets on port 0 will be classed as high priority	1

6.1.11. Port 0 Control 2

Table 22. Port 0 Control 2

Name	Byte.bit	Description	Default
Reserved	10.7~10.0		0000 0000

6.1.12. Port 0 Control 3

Table 23. Port 0 Control 3

Name	Byte.bit	Description	Default
Reserved	11.7~11.0		0000 0000

6.1.13. Port 0 Control 4 & VLAN Entry [A]

Table 24. Port 0 Control 4 & VLAN Entry [A]

Name	Byte.bit	Description	Default
VLAN Entry [A]			
Internal Use	12.7		1
Internal Use	12.6		1
Reserved	12.5		0
VLAN ID [A] membership Bit [4:0]	12.4~12.0	This 5-bit field specifies which ports are the members of VLAN A. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN A 10010 means port 4 and 1 are the members of VLAN A 11111 means all 5 ports are the members of VLAN A	1 0001
Port 0 Control 4			
Port 0 VLAN index [3:0]	13.7~13.5	In a port-based VLAN configuration, this register indexes port 0's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [P] Membership". Port 0 can only communicate within the membership. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID.	0000
Internal Use	13.3		1
Internal Use	13.2		1
Internal Use	13.1		1
Reserved	13.0		0
VLAN Entry [A]			
VLAN ID [A] [7:0]	14.7~14.0	This register along with byte 15.3~15.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A	0000 0000
Port 0 Control 4 & VLAN Entry [A]			
Internal Use	15.7		1
Internal Use	15.6		1
Internal Use	15.5		1
Internal Use	15.4		1
VLAN ID [A] [11:8]	15.3~15.0	This register along with byte 14.7~14.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A	0000

6.2. Port 1 Registers

6.2.1. Internal Use Register

Table 25. Internal Use Register

Name	Byte.bit	Description	Default
Internal Use	16.7~16.0	Internal Use	0xFF
Internal Use	17.7~17.0	Internal Use	0xFF
Internal Use	18.7~18.0	Internal Use	0xFF
Internal Use	19.7~19.0	Internal Use	0xFF
Internal Use	20.7~20.0	Internal Use	0xFF
Internal Use	21.7~21.0	Internal Use	0xFF
Internal Use	22.7~22.0	Internal Use	0xFF
Internal Use	23.7~23.0	Internal Use	0xFF

6.2.2. Port 1 Control 0

Table 26. Port 1 Control 0

Name	Byte.bit	Description	Default
Reserved	24.7		0
Internal Use	24.6		1
Internal Use	24.5~24.4		11
Internal Use	24.3		1
Internal Use	24.2		1
VLAN tag insert and remove	24.1~24.0	For port 1 egress packets 11=Do not insert or remove VLAN tags to/from packet 10=Insert VLAN tags to non-tagged packets 01=Remove tag from tagged packets 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets	11

6.2.3. Port 1 Control 1

Table 27. Port 1 Control 1

Name	Byte.bit	Description	Default
Reserved	25.7		1
Internal Use	25.6		0
Local loopback	25.5	1: Perform local loopback, i.e. loopback MAC's RX back to TX 0: Normal operation	0
Internal Use	25.4		0
Discard Non PVID packets	25.3	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID 0: No packets will be dropped	0
Disable 802.1p priority	25.2	1: Disable 802.1p priority classification for ingress packets on port 1 0: Enable 802.1p priority classification on port 1	1
Disable Diffserv priority	25.1	1: Disable Diffserv priority classification for ingress packets on port 1 0: Enable Diffserv priority classification	1
Disable port-based priority on port 1	25.0	1: Disable port based priority QoS function on port 1 0: Enable port-based priority QoS function on port 1. Ingress packets on port 1 will be classed as high priority	1

6.2.4. Port 1 Control 2

Table 28. Port 1 Control 2

Name	Byte.bit	Description	Default
Internal Use	26.7		0
Reserved	26.6~ 26.5		10
Internal Use	26.4		1
Reserved	26.3~ 26.0		1111

6.2.5. Port 1 Control 3

Table 29. Port 1 Control 2

Name	Byte.bit	Description	Default
Reserved	27.7		1
Internal Use	27.6		0
Reserved	27.5~ 27.0		00 1111

6.2.6. Port 1 Control 4 & VLAN Entry [B]

Table 30. Port 1 Control 4 & VLAN Entry [B]

Name	Byte.bit	Description	Default
VLAN Entry [B]			
Internal Use	28.7		1
Internal Use	28.6		1
Reserved	28.5		0
VLAN ID [B] Membership Bit [4:0]	28.4~ 28.0	This 5-bit field specifies which ports are the members of VLAN B. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN B 10010 means port 4 and 1 are the members of VLAN B 11111 means all 5 ports are members of VLAN B.	1 0010
Port 1 Control 4			
Port 1 VLAN index [3:0]	29.7~ 29.5	In a port-based VLAN configuration, this register indexes to port 1's 'Port VLAN Membership', which may be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 1 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0001, which indexes to the VLAN entry [B] that is composed of VLAN ID [B] Membership Bit [4:0] in PHY1 Reg.24.[4:0] and VLAN ID [B] in PHY1 Reg.25.[11:0].	0001
Internal Use	29.3		1
Internal Use	29.2		1
Internal Use	29.1		1
Reserved	29.0		0
VLAN Entry [B]			
VLAN ID [B] [7:0]	30.7~ 30.0	This register, along with byte 31.3~31.0, defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B.	0000 0001
Port 1 Control 4 & VLAN Entry [B]			
Internal Use	31.7		1
Internal Use	31.6		1
Internal Use	31.5		1
Internal Use	31.4		1
VLAN ID [B] [11:8]	31.3~ 31.0	This register, along with byte 30.7~30.0, defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B.	0000

6.3. Port 2 Registers

6.3.1. Internal Use Register

Table 31. Internal Use Register

Name	Byte.bit	Description	Default
Internal Use Register			
Internal Use	32.7~32.0		0xFF
Internal Use	33.7~33.0		0xFF
Internal Use	34.7~34.0		0xFF
Internal Use	35.7~35.0		0xFF
Internal Use	36.7~36.0		0xFF
Internal Use	37.7~37.0		0xFF
Internal Use	38.7~38.0		0xFF
Internal Use	39.7~39.0		0xFF

6.3.2. Port 2 Control 0

Table 32. Port 2 Control 0

Name	Byte.bit	Description	Default
Reserved	40.7		0
Internal Use	40.6		1
Internal Use	40.5~40.4		11
Internal Use	40.3		1
Internal Use	40.2		1
VLAN tag insert and remove	40.1~40.0	For port 2 egress packets 11=Do not insert or remove VLAN tags to/from packet 10=Insert VLAN tags to non-tagged packets 01=Remove tag from tagged packets 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets	11

6.3.3. Port 2 Control 1

Table 33. Port 2 Control 1

Name	Byte.bit	Description	Default
Reserved	41.7		1
Internal Use	41.6		0
Local loopback	41.5	1: Perform 'local loopback', i.e. loopback MAC's RX back to TX 0: Normal operation	0
Internal Use	41.4		0
Discard Non PVID packets	41.3	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID 0: No packets will be dropped	0
Disable 802.1p priority	41.2	1: Disable 802.1p priority classification for ingress packets on port 2 0: Enable 802.1p priority classification on port 2	1
Disable Diffserv priority	41.1	1: Disable Diffserv priority classification for ingress packets on port 2 0: Enable Diffserv priority classification	1
Disable port-based priority on port 2	41.0	1: Disable port based priority QoS function on port 2 0: Enable port based priority QoS function on port 2. Ingress packets on port 2 will be classed as high priority	1

6.3.4. Reserved

Table 34. Reserved

Name	Byte.bit	Description	Default
Reserved	42.7~42.0		0x20
Reserved	43.7~43.0		0x00

6.3.5. Port 2 Control 2 & VLAN Entry [C]

Table 35. Port 2 Control 2 & VLAN Entry [C]

Name	Byte.bit	Description	Default
VLAN Entry [C]			
Internal Use	44.7		1
Internal Use	44.6		1
Reserved	44.5		0
VLAN ID [C] Membership Bit [4:0]	44.4~44.0	This 5-bit field specifies which ports are the members of VLAN C. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g. 10001 means port 4 and 0 are the members of VLAN C 10010 means port 4 and 1 are the members of VLAN C 11111 means all 5 ports are the members of VLAN C	1 0100
Port 2 Control 2			
Port 2 VLAN index [3:0]	45.7~45.5	In a port-based VLAN configuration, this register indexes to port 2's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 2 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0010, which indexes to the VLAN entry [C] that is composed of VLAN ID [C] Membership Bit [4:0] in PHY2 Reg.24.[4:0] and VLAN ID [C] in PHY2 Reg.25.[11:0].	0010
Internal Use	45.3		1
Internal Use	45.2		1
Internal Use	45.1		1
Reserved	45.0		0
VLAN Entry [C]			
VLAN ID [C] [7:0]	46.7~46.0	This register along with byte 47.3~47.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C	0000 0010
Port 2 Control 2 & VLAN Entry [C]			
Internal Use	47.7		1
Internal Use	47.6		1
Internal Use	47.5		1
Internal Use	47.4		1
VLAN ID [C] [11:8]	47.3~47.0	This register along with byte 46.7~46.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C	0000

6.4. Port 3 Registers

6.4.1. Switch MAC Address

The Switch MAC address is used as the source address in MAC pause control frames.

Table 36. Switch MAC Address

Name	Byte.bit	Description	Default
Switch MAC Address [47:40]	48.7~48.0	Switch MAC Address Byte 5	0x52
Switch MAC Address [39:32]	49.7~49.0	Switch MAC Address Byte 4	0x54
Switch MAC Address [31:24]	50.7~50.0	Switch MAC Address Byte 3	0x4C
Switch MAC Address [23:16]	51.7~51.0	Switch MAC Address Byte 2	0x83
Switch MAC Address [15:8]	52.7~52.0	Switch MAC Address Byte 1	0x05
Switch MAC Address [7:0]	53.7~53.0	Switch MAC Address Byte 0	0xC0

6.4.2. Port 3 Control 0

Table 37. Port 3 Control 0

Name	Byte.bit	Description	Default
Reserved	54.7		0
Internal Use	54.6		1
Internal Use	54.5~54.4		11
Internal Use	54.3		1
Internal Use	54.2		1
VLAN tag insert and remove	54.1~54.0	For port 3 egress packets 11=Do not insert or remove VLAN tags to/from packet 10=Insert VLAN tags to non-tagged packets 01=Remove tag from tagged packets 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets	11

6.4.3. Port 3 Control 1

Table 38. Port 3 Control 1

Name	Byte.bit	Description	Default
Reserved	55.7		1
Internal Use	55.6		0
Local loopback	55.5	1: Perform 'local loopback', i.e. loopback MAC's RX back to TX 0: Normal operation	0
Internal Use	55.4		0
Discard Non PVID packets	55.3	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port's PVID 0: No packets will be dropped	0
Disable 802.1p priority	55.2	1: Disable 802.1p priority classification for ingress packets on port 3 0: Enable 802.1p priority classification on port 3	1
Disable Diffserv priority	55.1	1: Disable Diffserv priority classification for ingress packets on port 3 0: Enable Diffserv priority classification	1
Disable port-based priority on port 3	55.0	1: Disable port-based priority QoS function on port 3 0: Enable port-based priority QoS function on port 3. Ingress packets on port 3 will be classed as high priority	1

6.4.4. Reserved

Table 39. Reserved

Name	Byte.bit	Description	Default
Reserved	56.7~56.0		0x00
Reserved	57.7~57.0		0x00

6.4.5. Port 3 Control 2 & VLAN Entry [D]

Table 40. Port 3 Control 2 & VLAN Entry [D]

Name	Byte.bit	Description	Default
VLAN Entry [D]			
Internal Use	58.7		1
Internal Use	58.6		1
Reserved	58.5		0
VLAN ID [D] Membership Bit [4:0]	58.4~58.0	This 5-bit field specifies which ports are the members of VLAN D. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN D 10010 means port 4 and 1 are the members of VLAN D 11111 means all 5 ports are the members of VLAN D	1 1000

Port 3 Control 2			
Port 3 VLAN index [3:0]	59.7~59.5	In a port-based VLAN configuration, this register indexes to port 3's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 3 can only communicate with the members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0011, which indexes to the VLAN entry [D] that is composed of VLAN ID [D] Membership Bit [4:0] in PHY3 Reg.24.[4:0] and VLAN ID [D] in PHY3 Reg.25.[11:0].	0011
Internal Use	59.3		1
Internal Use	59.2		1
Internal Use	59.1		1
Reserved	59.0		0
VLAN Entry [D]			
VLAN ID [D] [7:0]	60.7~60.0	This register along with byte 61.3~61.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D	0000 0011
Port 3 Control 2 & VLAN Entry [D]			
Internal Use	61.7		1
Internal Use	61.6		1
Internal Use	61.5		1
Internal Use	61.4		1
VLAN ID [D] [11:8]	61.3~61.0	This register along with byte 60.7~60.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D	0000

6.4.6. Internal Use Register

Table 41. Internal Use Register

Name	Byte.bit	Description	Default
Internal Use	62.7~62.0		0x00
Internal Use	63.7~63.0		0x00
Internal Use	64.7~64.0		0x00
Internal Use	65.7~65.0		0x00
Internal Use	66.7~66.0		0x00
Internal Use	67.7~67.0		0x00

6.5. Port 4 Registers

6.5.1. Port 4 Control 0

Table 42. Port 4 Control 0

Name	Byte.bit	Description	Default
Reserved	68.7		0
Internal Use	68.6		1
Internal Use	68.5~68.4		11
Internal Use	68.3		1
Internal Use	68.2		1
VLAN tag insert and remove	68.1~68.0	For port 4 egress packets 11=Do not insert or remove VLAN tags to/from packet 10=Insert VLAN tags to non-tagged packets 01=Remove tag from tagged packets 00=Replace the VLAN tags for tagged packets and insert a VLAN tag to non-tagged packets	11

6.5.2. Port 4 Control 1

Table 43. Port 4 Control 1

Name	Byte.bit	Description	Default
Reserved	69.7		1
Internal Use	69.6		0
Local loopback	69.5	1: Perform ‘local loopback’, i.e. loopback MAC’s RX back to TX 0: Normal operation	0
Internal Use	69.4		0
Discard Non PVID packets	69.3	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port’s PVID 0: No packets will be dropped	0
Disable 802.1p priority	69.2	1: Disable 802.1p priority classification for ingress packets on port 4 0: Enable 802.1p priority classification on port 4	1
Disable Diffserv priority	69.1	1: Disable Diffserv priority classification for ingress packets on port 4 0: Enable Diffserv priority classification	1
Disable port-based priority on port 4	69.0	1: Disable port based priority QoS function on port 4 0: Enable port based priority QoS function on port 4. Ingress packet on port 4 will be classified as high priority	1

6.5.3. Reserved

Table 44. Reserved

Name	Byte.bit	Description	Default
Reserved	70.7~70.0		0x00
Reserved	71.7~71.0		0x00

6.5.4. Port 4 Control 2 & VLAN Entry [E]

Table 45. Port 4 Control 2 & VLAN Entry [E]

Name	Byte.bit	Description	Default
VLAN Entry [E]			
Internal Use	72.7		1
Internal Use	72.6		1
Reserved	72.5		0
VLAN ID [E] Membership Bit [4:0]	72.4~72.0	This 5-bit field specifies which ports are the members of VLAN E. If a destination address look up fails, a packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN E 10010 means port 4 and 1 are the members of VLAN E 11111 means all 5 ports are the members of VLAN E	1 1111
Port 4 Control 2			
Port 4 VLAN index [3:0]	73.7~73.5	In a port-based VLAN configuration, this register indexes to port 4's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 4 can only communicate with the members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0100, which indexes to the VLAN entry [E] that is composed of VLAN ID [E] Membership Bit [4:0] in PHY4 Reg.24.[4:0] and VLAN ID [E] in PHY4 Reg.25.[11:0].	0100
Internal Use	73.3		1
Internal Use	73.2		1
Internal Use	73.1		1
Reserved	73.0		0
VLAN Entry [E]			
VLAN ID [E] [7:0]	74.7~74.0	This register, along with byte 75.3~75.0, defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E	0000 0100
Port 4 Control 2 & VLAN Entry [E]			
Internal Use	75.7		1
Internal Use	75.6		1
Internal Use	75.5		1
Internal Use	75.4		1
VLAN ID [E] [11:8]	75.3~75.0	This register, along with byte 74.7~74.0, defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E	0000

6.5.5. Internal Use Register

Table 46. Internal Use Register

Name	Byte.bit	Description	Default
Reserved	76.7		0
Internal Use	76.6~76.4		100
Reserved	76.3		0
Internal Use	76.2~76.0		000

6.5.6. 802.1p Base Priority

Table 47. 802.1p Base Priority

Name	Byte.bit	Description	Default
802.1p base priority	77.7~77.5	Classifies priority for incoming 802.1Q packets, if 802.1p priority classification is enabled. “User priority” compared against this value. >=: Classify as high priority <: Classify as low priority	100
Reserved	77.4~77.0		0 0000

6.6. VLAN Entries

6.6.1. VLAN Entry [F]

Table 48. VLAN Entry [F]

Name	Byte.bit	Description	Default
VLAN Entry [F]			
Reserved	78.7~78.5		000
VLAN ID [F] Membership Bit [4:0]	78.4~78.0	This 5-bit field specifies which ports are the members of VLAN F. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN F 10010 means port 4 and 1 are the members of VLAN F 11111 means all 5 ports are the members of VLAN F	1 0001
Reserved	79.7~79.0		0101 0000
VLAN ID [F] [7:0]	80.7~80.0	This register along with byte 81.3~81.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F	0000 0101
Reserved	81.7~81.4		1111
VLAN ID [F] [11:8]	81.3~81.0	This register along with byte 80.7~80.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F	0000

6.6.2. VLAN Entry [G]

Table 49. VLAN Entry [G]

Name	Byte.bit	Description	Default
VLAN Entry [G]			
Reserved	82.7~82.5		000
VLAN ID [G] membership Bit [4:0]	82.4~82.0	This 5-bit field specifies which ports are the members of VLAN G. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN G 10010 means port 4 and 1 are the members of VLAN G 11111 means all 5 ports are the members of VLAN G	1 0010
Reserved	83.7~83.0		0110 0000
VLAN ID [G] [7:0]	84.7~84.0	This register along with byte 85.3~85.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN G	0000 0110
Reserved	85.7~85.4		1111
VLAN ID [G] [11:8]	85.3~85.0	This register along with byte 84.7~84.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN G	0000

6.6.3. VLAN Entry [H]

Table 50. VLAN Entry [H]

Name	Byte.bit	Description	Default
VLAN Entry [H]			
Reserved	86.7~86.5		000
VLAN ID [H] membership Bit [4:0]	86.4~86.0	This 5-bit field specifies which ports are the members of VLAN H. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN H 10010 means port 4 and 1 are the members of VLAN H 11111 means all 5 ports are members of VLAN H	1 0100
Reserved	87.7~87.0		0111 0000
VLAN ID [H] [7:0]	88.7~88.0	This register along with byte 89.3~89.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H	0000 0111
Reserved	89.7~89.4		1111
VLAN ID [H] [11:8]	89.3~89.0	This register along with byte 88.7~88.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H	0000

6.6.4. VLAN Entry [I]

Table 51. VLAN Entry [I]

Name	Byte.bit	Description	Default
VLAN Entry [I]			
Reserved	90.7~90.5		000
VLAN ID [I] membership Bit [4:0]	90.4~90.0	This 5-bit field specifies which ports are the members of VLAN I. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN I 10010 means port 4 and 1 are the members of VLAN I 11111 means all 5 ports are the members of VLAN I	1 1000
Reserved	91.7~91.0		1000 0000
VLAN ID [I] [7:0]	92.7~92.0	This register along with byte 93.3~93.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I	0000 1000
Reserved	93.7~93.4		1111
VLAN ID [I] [11:8]	93.3~93.0	This register along with byte 92.7~92.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I	0000

6.6.5. VLAN Entry [J]

Table 52. VLAN Entry [J]

Name	Byte.bit	Description	Default
VLAN Entry [I]			
Reserved	94.7~94.5		000
VLAN ID [J] membership Bit [4:0]	94.4~94.0	This 5-bit field specifies which ports are the members of VLAN J. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN J 10010 means port 4 and 1 are the members of VLAN J 11111 means all 5 ports are members of VLAN J	1 1111
Reserved	95.7~95.0		1001 0000
VLAN ID [J] [7:0]	96.7~96.0	This register along with byte 97.3~97.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN J	0000 1001
Reserved	97.7~97.4		1111
VLAN ID [J] [11:8]	97.3~97.0	This register along with byte 96.7~96.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN J	0000

6.6.6. VLAN Entry [K]

Table 53. VLAN Entry [K]

Name	Byte.bit	Description	Default
Reserved	98.7~98.5		000
VLAN ID [K] Membership Bit [4:0]	98.4~98.0	This 5-bit field specifies which ports are the members of VLAN K. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN K 10010 means port 4 and 1 are the members of VLAN K 11111 means all 5 ports are the members of VLAN K	1 0001
Reserved	99.7~99.0		1010 0000
VLAN ID [K] [7:0]	100.7~100.0	This register along with byte 101.3~101.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN K	0000 1010
Reserved	101.7~101.4		1111
VLAN ID [K] [11:8]	101.3~101.0	This register along with byte 100.7~100.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN K	0000

6.6.7. VLAN Entry [L]

Table 54. VLAN Entry [L]

Name	Byte.bit	Description	Default
VLAN Entry [L]			
Reserved	102.7~102.5		000
VLAN ID [L] membership Bit [4:0]	102.4~102.0	This 5-bit field specifies which ports are the members of VLAN L. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN L 10010 means port 4 and 1 are the members of VLAN L 11111 means all 5 ports are members of VLAN L	1 0010
Reserved	103.7~103.0		1011 0000
VLAN ID [L] [7:0]	104.7~104.0	This register along with byte 105.3~105.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN L	0000 1011
Reserved	105.7~105.4		1111
VLAN ID [L] [11:8]	105.3~105.0	This register along with byte 104.7~104.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN L	0000

6.6.8. VLAN Entry [M]

Table 55. VLAN Entry [M]

Name	Byte.bit	Description	Default
VLAN Entry [M]			
Reserved	106.7~106.5		000
VLAN ID [M] membership Bit [4:0]	106.4~106.0	This 5-bit field specifies which ports are the members of VLAN M. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN M 10010 means port 4 and 1 are the members of VLAN M 11111 means all 5 ports are members of VLAN M	1 0100
Reserved	107.7~107.0		1100 0000
VLAN ID [M] [7:0]	108.7~108.0	This register along with byte 109.3~109.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN M	0000 1100
Reserved	109.7~109.4		1111
VLAN ID [M] [11:8]	109.3~109.0	This register along with byte 108.7~108.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN M	0000

6.6.9. VLAN Entry [N]

Table 56. VLAN Entry [N]

Name	Byte.bit	Description	Default
VLAN Entry [N]			
Reserved	110.7~110.5		000
VLAN ID [N] membership Bit [4:0]	110.4~110.0	This 5-bit field specifies which ports are the members of VLAN N. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN N 10010 means port 4 and 1 are the members of VLAN N 11111 means all 5 ports are the members of VLAN N	1 1000
Reserved	111.7~111.0		1101 0000
VLAN ID [N] [7:0]	112.7~112.0	This register along with byte 113.3~113.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN N	0000 1101
Reserved	113.7~113.4		1111
VLAN ID [N] [11:8]	113.3~113.0	This register along with byte 112.7~112.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN M	0000

6.6.10. VLAN Entry [O]

Table 57. VLAN Entry [O]

Name	Byte.bit	Description	Default
VLAN Entry [O]			
Reserved	114.7~114.5		000
VLAN ID [O] membership Bit [4:0]	114.4~114.0	This 5-bit field specifies which ports are the members of VLAN O. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN O 10010 means port 4 and 1 are the members of VLAN O 11111 means all 5 ports are members of VLAN O	1 1111
Reserved	115.7~115.0		1110 0000
VLAN ID [O] [7:0]	116.7~116.0	This register along with byte 117.3~117.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN O	0000 1110
Reserved	117.7~117.4		1111
VLAN ID [O] [11:8]	117.3~117.0	This register along with byte 116.7~116.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN O	0000

6.6.11. VLAN Entry [P]

Table 58. VLAN Entry [P]

Name	Byte.bit	Description	Default
VLAN Entry [P]			
Reserved	118.7~118.5		000
VLAN ID [P] Membership Bit [4:0]	118.4~118.0	This 5-bit field specifies which ports are the members of VLAN P. If a destination address look up fails, packets associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN P 10010 means port 4 and 1 are the members of VLAN P 11111 means all 5 ports are members of VLAN P	1 0001
Reserved	119.7~119.0		1111 0000
VLAN ID [P] [7:0]	120.7~120.0	This register along with byte 27.3~27.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN P	0000 1111
Reserved	121.7~121.4		1111
VLAN ID [P] [11:8]	121.3~121.0	This register along with byte 26.7~26.0 defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN P	0000

7. Register Descriptions

Hardware Reset: pin RESET#=0 to 1. Reset all then load EEPROM and Pin registers with serial EEPROM and Pin strapping.

Soft Reset: Write bit12 of Reg16 of PHY0 as 1. Reset all except loading EEPROM and Pin Registers with serial EEPROM and Pins. After updating the EEPROM or Pin registers via SMI, the external device must do a soft reset in order to allow the configuration change to take affect.

Note: In this section the following abbreviations are used:

RO: Read Only
RW: Read/Write
LL: Latch Low until clear
LH: Latch High until clear
SC: Self Clearing

Table 59. Register Descriptions

Name	PHY	Page	Register	Register Description
Port 0 PHY Register	0	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Register
			16~19	Global Control Register
			22	Port 0 Control Register 0
			24	Port 0 Control Register 1 & VLAN ID [A] Membership
			25	Port 0 Control Register 2 & VLAN ID [A]
		0	26	Reserved
		1	26	VLAN ID [F] Membership
		0	27	Reserved
		1	27	VLAN ID [F]
		0	28	Reserved
		1	28	VLAN ID [K] Membership
		0	29	Reserved
		1	29	VLAN ID [K]
		0	30	Reserved
		1	30	VLAN ID [P] Membership
		0	31	Reserved
		1	31	VLAN ID [P]
Port 1 PHY Register	1	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2

Name	PHY	Page	Register	Register Description
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Register
			16~17	Internal Use Register
			18~19	Internal Use Register
			22	Port 1 Control Register 0
			23	Global Option Register 0
			24	Port 1 Control Register 1 & VLAN ID[B] Membership
			25	Port 1 Control Register 2 & VLAN ID[B]
		0	26	Reserved
		1	26	VLAN ID [G] Membership
		0	27	Reserved
		1	27	VLAN ID [G]
		0	28	Reserved
		1	28	VLAN ID [L] Membership
		0	29	Reserved
		1	29	VLAN ID [L]
Port 2 PHY Register	2	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Register
			16~17	Internal Use Register
			18~19	Internal Use Register
			22	Port 2 Control Register 0
			24	Port 2 Control Register 1 & VLAN ID[C] Membership
			25	Port 2 Control Register 2 & VLAN ID [C]
		0	26	Reserved
		1	26	VLAN ID [H] Membership
		0	27	Reserved
		1	27	VLAN ID [H]
		0	28	Reserved
		1	28	VLAN ID [M] Membership
		0	29	Reserved
		1	29	VLAN ID [M]
Port 3 PHY Register	3	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Register

Name	PHY	Page	Register	Register Description
			16~18	Switch MAC Address
			19~21	Internal Use Register
			22	Port 3 Control Register 0
			24	Port 3 Control Register 1 & VLAN ID[D] Membership
			25	Port 3 Control Register 2 & VLAN ID [D]
		0	26	Reserved
		1	26	VLAN ID [I] Membership
		0	27	Reserved
		1	27	VLAN ID [I]
		0	28	Reserved
		1	28	VLAN ID [N] Membership
		0	29	Reserved
		1	29	VLAN ID [N]
Port 4 PHY Register	4	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2
			4	Auto-Negotiation Advertisement Register
			5	Auto-Negotiation Link Partner Ability Register
			6	Auto-Negotiation Expansion Register
			16	Indirect Access Control
			17~20	Indirect Access Data
			21	Internal Use Register
			22	Port 4 Control Register 0
			24	Port 4 Control Register 1 & VLAN ID[E] Membership
			25	Port 4 Control Register 2 & VLAN ID [E]
		0	26	Reserved
		1	26	VLAN ID [J] Membership
		0	27	Reserved
		1	27	VLAN ID [J]
		0	28	Reserved
		1	28	VLAN ID [O] Membership
		0	29	Reserved
		1	29	VLAN ID [O]
PHY Register for Port 4 MAC	5	0	0	Control Register
			1	Status Register
			2	PHY Identifier 1
			3	PHY Identifier 2
			4	Auto-Negotiation Advertisement Register

7.1. PHY 0 Registers

7.1.1. PHY 0 Register 0 for Port 0: Control

Table 60. PHY 0 Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset. This bit is self-clearing	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex or 100Base-TX full duplex.	0
0.13	Speed Select	RW	1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI. (Read/Write). When 100FX mode is enabled, this bit=1 (Read only).	From pin
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write). When 100FX mode is enabled, this bit=0 (Read only). 100FX must be in Force Mode. In order to avoid errors, the RTL8305SC will ignore the action of this bit when writing Reg0.12 as 1 in 100FX mode.	From pin
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from MII. PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled (Reg0.12=1), this bit reflects the result of auto-negotiation (Read only). When NWay is disabled (Reg0.12=0, force mode of UTP or 100FX), this bit can be set through SMI (Read/Write). 100FX must be in Force Mode. In order to avoid errors, the RTL8305SC will ignore the action to this bit when writing Reg0.12 as 1 in 100FX mode.	From pin
0.[7:0]	Reserved			0000 0000

7.1.2. PHY 0 Register 1 for Port 0: Status

Table 61. PHY 0 Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base_T4	RO	0: No 100Base-T4 capability	0
1.14	100Base_TX_FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base_TX_HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base_T_FD	RO	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base_T_HD	RO	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
1.[10:7]	Reserved	RO		0000
1.6	MF Preamble Suppression	RO	The RTL8305SC will accept management frames with preamble suppressed. (The RTL8305SC accepts management frames without preamble. Minimum preamble of 32 bits is required for the first SMI read/write transaction after reset. One idle bit is required between any two management transactions as defined in IEEE 802.3u).	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. MII Reg.4 and 5 are valid if this bit is set 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault condition detected 0: No remote fault When in 100FX mode, this bit means in-band signal Far-End-Fault is detected	0
1.3	Auto-Negotiation Ability	RO	1: NWay auto-negotiation capable (permanently=1)	1
1.2	Link Status	RO/LL	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link has failed	0
1.1	Jabber Detect	RO/LH	0: No Jabber detected The RTL8305SC does not support this function.	0
1.0	Extended Capability	RO	1: Extended register capable (permanently=1)	1

7.1.3. PHY 0 Register 2 for Port 0: PHY Identifier 1

Table 62. PHY 0 Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively	0x001C

7.1.4. PHY 0 Register 3 for Port 0: PHY Identifier 2

Table 63. PHY 0 Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's model number (05: Indicates RTL8305	000101
3.[3:0]	Revision Number	RO	Manufacturer's revision number (02: Indicates SC	0010

7.1.5. PHY 0 Register 4 for Port 0: Auto-Negotiation Advertisement

Note: Each time the link ability of the RTL8305SC is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 64. PHY 0 Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Next Page enabled 0: Next Page disabled (Permanently=0)	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8305SC has detected a remote fault 0: No remote fault detected	0
4.[12:11]	Reserved	RO		00
4.10	Pause	RW	1: Advertises that the RTL8305SC possesses 802.3x flow control capability 0: No flow control capability	From pin
4.9	100Base-T4	RO	Technology not supported. (Permanently=0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	From pin
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	From pin
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	From pin
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RW	[00001]=IEEE 802.3	00001

7.1.6. PHY 0 Register 5 for Port 0: Auto-Negotiation Link Partner Ability

Table 65. PHY 0 Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.[12:11]	Reserved	RO		00
5.10	Pause	RO	1: Flow control supported by Link Partner 0: Flow control not supported by Link Partner	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner For 100FX mode, this bit will be set if Reg.0.8=1 or Full=1 after link is established When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=1 after link is established.	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner For 100FX mode, this bit is set when Reg.0.8=1 or Full=1 after link established. When auto negotiation is disabled, this bit will be set if Reg0.13=1 and Reg0.8=0 after link is established.	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=1 after link is established.	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner When auto negotiation is disabled, this bit will be set if Reg0.13=0 and Reg0.8=0 after link is established.	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

7.1.7. PHY 0 Register 16: Global Control 0

Table 66. PHY 0 Register 16: Global Control 0

Reg.bit	Name	Mode	Description	Default
16.15	Page selection	RW	1: Select the registers in page 1 0: Select the registers in page 0	0
16.14	Reserved			0

Reg.bit	Name	Mode	Description	Default
16.13	Lookup table accessible enable	RW	1: Lookup table is accessible via indirect access registers 0: Lookup table is not accessible	0
16.12	Software Reset	RW SC	1: Soft reset. This bit is self-clearing If this bit is set to 1, the RTL8305SC will reset all internal registers except PHY registers, and will not load configurations from EEPROM or strapping pins. Software reset is designed to provide a convenient way for users to change the configuration via SMI. After changing register values in the RTL8305SC (except PHY registers) via SMI, the external device must execute a soft reset (by setting this bit to 1) in order to update the configuration.	0
16.11	Reserved			0
16.10	Disable 802.1Q tag aware VLAN	RW	1: Disable 802.1Q tagged-VID Aware function. The RTL8305SC will not check the tagged VID on received frames to perform tagged-VID VLAN mapping. Under this configuration, the RTL8305SC only uses the per-port VLAN index register to perform Port-Based VLAN mapping 0: Enable the Member Set Filtering function of the VLAN Ingress Rules. The RTL8305SC checks the tagged VID on received frames with the VIDA[11:0]~VIDH[11:0] to index to a member set, then performs VLAN mapping. The RTL8305SC uses tagged-VID VLAN mapping for tagged frames but still uses Port-Based VLAN mapping for priority-tagged and untagged frames	1
16.9	Disable VLAN member set ingress filtering	RW	1: The switch will not drop the received frame if the ingress port of this packet is not included in the matched VLAN member set. It will still forward the packet to the VLAN members specified in the matched member set. This setting both works on port-based and tag-based VLAN configurations 0: The switch will drop the received frame if the ingress port of this packet is not included in the matched VLAN member set	1
16.8	Disable VLAN tag admit control	RW	1: The switch accepts all frames it receives whether tagged or untagged 0: The switch will only accept tagged frames and will drop untagged frames	1
16.7	EEPROM existence	RO	1: EEPROM does not exist (pin EnEEPROM=0 or pin EnEEPROM=1 but EEPROM does not exist) 0: EEPROM exists (pin EnEEPROM=1 and EEPROM exists)	1
16.6	Internal Use	RW		1
16.5	Internal Use	RW		1
16.4	Internal Use	RW		1
16.3	Internal Use	RW		1
16.2	Enable loop detection function	RW	1: Enable loop detection function 0: Disable loop detection function	0
16.1	Reserved	RW		1
16.0	Internal Use	RW		0

7.1.8. PHY 0 Register 17: Global Control 1

Table 67. PHY 0 Register 17: Global Control 1

Reg.bit	Name	Mode	Description	Default
17.15	Internal Use	RW		0
17.14	Internal Use	RW		0
17.[13:8]	Internal Use	RW		11 1111
17.7	Internal Use	RW		0
17.6	Internal Use	RW		0
17.[5:0]	Internal Use	RW		11 1111

7.1.9. PHY 0 Register 18: Global Control 2

Table 68. PHY 0 Register 18: Global Control 2

Reg.bit	Name	Mode	Description	Default
18.15	Reserved	RW		Default=1
18.14	Maximum Frame Length	RW	1: 1536Bytes 0: 1552Bytes	Pin Max1536 strap option Default=1
18.13	Enable broadcast drop	RW	1: Use Broadcast Input drop mechanism 0: Use Broadcast Output drop mechanism	Pin BCInDrop strap option Default=1
18.12	Forward 802.1D reserved MAC addresses frame.	RW	1: Forward reserved control frames, whose DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F packets 0: Filter reserved control packets, whose DID=01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F	Pin EnForward strap option Default=1
18.11	Disable leaky VLAN	RW	1: Disable forwarding of unicast frames to other VLANs 0: Enable forwarding of unicast frames to other VLANs Broadcast and multicast frames adhere to the VLAN configuration	Pin DisLeaky strap option Default=1
18.10	Disable ARP VLAN	RW	1: Disable broadcasting of ARP broadcast packets to all VLANs 0: Enable broadcasting of ARP broadcast packets to all VLANs ARP broadcast frame DID is all F	Pin DisARP strap option Default=1
18.9	Enable 48 pass 1	RW	1: 48 pass 1. Continuously collides 48 input packets then passes 1 packet to retain system resources and avoid partition in the repeater when the packet buffer is full 0: Continuously collides to avoid packet loss when the packet buffer is full	Pin En48pass1 strap option Default=1
18.8	Disable VLAN	RW	1: Disable VLAN 0: Enable VLAN. The default VLAN membership configuration by internal register is port 4 overlapped with all the other ports, to form 4 individual VLANs. This default membership configuration may be modified by setting up internal registers via the SMI interface or EEPROM	Pin DISVLAN strap option Default=1
18.7	Reserved	RW		Default=1

Reg.bit	Name	Mode	Description	Default
18.6	Enable defer	RW	1: Enable carrier sense deferring for half duplex back pressure 0: Disable carrier sense deferring for half duplex back pressure	Pin EnDefer strap option Default=1
18.5	LED blink time	RW	1: On for 43ms, then Off for 43ms 0: On for 120ms, then Off for 120ms	Pin LED_BLNK_TIME strap option Default=1
18.[4:3]	Queue weight	RW	The frame service ratio between the high priority queue and low priority queue is: 11=16:1 10=Always high priority queue first 01=8:1 00=4:1	Pin QWeight[1:0] strap option Default=11
18.2	Disable broadcast storm control	RW	1: Disable Broadcast Storm Control 0: Enable Broadcast Storm Control	Pin DisBrdCtrl strap option Default=1
18.1	Enable power-on blinking	RW	1: Enable power-on LED blinking for diagnosis 0: Disable power-on LED blinking for diagnosis	Pin En_Rst_Blnk strap option Default=1
18.0	Reserved			1

7.1.10. PHY 0 Register 19: Global Control 3

Table 69. PHY 0 Register 19: Global Control 3

Reg.bit	Name	Mode	Description	Default
19.[15:14]	Reserved			11
19.[13:12]	LED Mode[1:0]	RW	11=Mode 3: Speed, Link+Act, Duplex+Col, Link/Act/Speed 10=Mode 2: Speed, Act, Duplex/Col, Bi-color Link/Activity 01=Mode 1: Speed, RxAct, TxAct, Link 00=Mode 0: Reserved	Pin LEDMode[1:0] strap option Default=11
19.11	Internal Use	RW		Default=1
19.10	Disable dual MII interface of Port 4	RW	1: Disable dual MII interface of port 4. Only provides MII interface for the MAC circuit of port 4 0: Enable dual MII interface of port 4. Provides MII interface for the MAC circuit of port 4, and also provides MII interface for the PHY circuit of port 4	Pin DISDUALMII strap option Default=1
19.[9:0]	Reserved			11 1111 1111

7.1.11. PHY 0 Register 22: Port 0 Control Register 0

Table 70. PHY 0 Register 22: Port 0 Control Register 0

Reg.bit	Name	Mode	Description	Default
22.15	Reserved			1
22.14	Internal Use	RW		0
22.13	Port 0 Local loopback	RW	1: Perform 'local loopback', i.e. loop MAC's RX back to TX. 0: Normal operation	0
22.12	Internal Use	RW		0
22.11	Port 0 Non PVID packets Discard	RW	1: If the received packets are tagged, the switch will discard packets whose VID does not match the ingress port default VID, which is indexed by port 0's 'Port based VLAN index' 0: No packets will be discarded	0
22.10	Port 0 802.1p priority Disable	RW	1: Disable 802.1p priority classification for ingress packets on port 0 0: Enable 802.1p priority classification	Pin DisTagPri strap option Default=1
22.9	Port 0 Diffserv priority Disable	RW	1: Disable Diffserv priority classification for ingress packets on port 0 0: Enable Diffserv priority classification	Pin DisDSPri strap option Default=1
22.8	Port 0 port-based priority Disable	RW	1: Disable port-based priority QoS function on port 0 0: Enable port-based priority QoS function on port 0. Ingress packet on port 0 will be classified as high priority	Pin DisPortPri[0] strap option Default=1
22.7	Reserved			0
22.6	Internal Use	RW		1
22.[5:4]	Internal Use	RW		1
22.3	Internal Use	RW		1
22.2	Internal Use	RW		1
22.[1:0]	Port 0 VLAN tag insert and remove	RW	11=Do not insert or remove VLAN tags to/from packets that are output on this port 10=The switch will add VLAN tags to packets, if they are not tagged when these packets are output on this port. The switch will not add tags to packets already tagged. The inserted tag is the ingress port's 'Default tag', which is indexed by port 0's 'Port based VLAN index' 01=The switch will remove VLAN tags from packets if they are tagged when these packets are output on port 0. The switch will not modify packets received without tags 00=The switch will remove VLAN tags from packets then add new tags to them. The inserted tag is the ingress port's 'Default tag', which is indexed by port 0's 'Port based VLAN index'. This is a replacement processing for tagged packets and an insertion for untagged packets	11

7.1.12. PHY 0 Register 24: Port 0 Control Register 1 & VLAN ID [A] Membership

Table 71. PHY 0 Register 24: Port 0 Control Register 1 & VLAN ID [A] Membership

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Port 0 VLAN index [3:0]	RW	In a port-based VLAN configuration, this register indexes to port 0's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 0 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0000, which indexes to the VLAN entry [A] that is composed of VLAN ID[A] Membership Bit [4:0] in PHY0 Reg.24.[4:0], and VLAN ID [A] in PHY0 Reg.25.[11:0].	0000
24.11	Internal Use	RW		1
24.10	Internal Use	RW		1
24.9	Internal Use	RW		1
24.8	Internal Use	RO		0
24.7	Internal Use	RW		1
24.6	Internal Use	RW		1
24.5	Reserved			0
24.[4:0]	VLAN ID [A] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN A. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4.E.g.: 10001 means port 4 and 0 are the members of VLAN A 10010 means port 4 and 1 are the members of VLAN A 11111 means all 5 ports are the members of VLAN A	1 0001

7.1.13. PHY 0 Register 25: Port 0 Control Register 2 & VLAN ID [A]

Table 72. PHY 0 Register 25: Port 0 Register Control 2 & VLAN ID [A]

Reg.bit	Name	Mode	Description	Default
25.15	Internal Use	RW		1
25.14	Internal Use	RW		1
25.13	Internal Use	RW		1
25.12	Internal Use	RW		1
25.[11:0]	VLAN ID [A]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN A	0x000

7.1.14. PHY 0 Register 26: Reserved or VLAN ID [F] Membership

7.1.14.1 PHY 0 Register 26: Reserved Register (Page=0)

Table 73. PHY 0 Register 26: Reserved Register

Reg.bit	Name	Mode	Description	Default
26.[15:0]	Reserved			0x5105

7.1.14.2 PHY 0 Register 26: VLAN ID [F] Membership (Page=1)

Table 74. PHY 0 Register 26: VLAN ID [F] Membership

Reg.bit	Name	Mode	Description	Default
26.[15:5]	Reserved			1111 1111 111
26.[4:0]	VLAN ID [F] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN F. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN F 10010 means port 4 and 1 are the members of VLAN F 11111 means all 5 ports are the members of VLAN F	1 0001

7.1.15. PHY 0 Register 27: Reserved or VLAN ID [F]

7.1.15.1 PHY 0 Register 27: Reserved Register (Page=0)

Table 75. PHY 0 Register 27: Reserved Register

Reg.bit	Name	Mode	Description	Default
27.[15:0]	Reserved			0x0000

7.1.15.2 PHY 0 Register 27: VLAN ID [F] (Page=1)

Table 76. PHY 0 Register 27: VLAN ID [F]

Reg.bit	Name	Mode	Description	Default
27.[15:12]	Reserved			1111
27.[11:0]	VLAN ID [F]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN F	0000 0000 0101

7.1.16. PHY 0 Register 28: Reserved or VLAN ID [K] Membership

7.1.16.1 PHY 0 Reg.28: Reserved Register (Page=0)

Table 77. PHY 0 Register 28: Reserved Register

Reg.bit	Name	Mode	Description	Default
28.[15:0]	Reserved			0x0020

7.1.16.2 PHY 0 Register 28: VLAN ID [K] Membership (Page=1)

Table 78. PHY 0 Register 28: VLAN ID [K] Membership

Reg.bit	Name	Mode	Description	Default
28.[15:5]	Reserved			1111 1111 111
28.[4:0]	VLAN ID [K] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN K. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN K 10010 means port 4 and 1 are the members of VLAN K 11111 means all 5 ports are the members of VLAN K	1 0001

7.1.17. PHY 0 Register 29: Reserved or VLAN ID [K]

7.1.17.1 PHY 0 Register 29: Reserved Register (Page=0)

Table 79. PHY 0 Register 29: Reserved Register

Reg.bit	Name	Mode	Description	Default
29.[15:0]	Reserved			

7.1.17.2 PHY 0 Register 29: VLAN ID [K] (Page=1)

Table 80. PHY 0 Register 29: VLAN ID [K]

Reg.bit	Name	Mode	Description	Default
29.[15:12]	Reserved			1111
29.[11:0]	VLAN ID [K]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN K	0000 0000 1010

7.1.18. PHY 0 Register 30: Reserved or VLAN ID [P] Membership

7.1.18.1 PHY 0 Register 30: Reserved Register (Page=0)

Table 81. PHY 0 Register 30: Reserved Register

Reg.bit	Name	Mode	Description	Default
30.[15:0]	Reserved			

7.1.18.2 PHY0 Register 30: VLAN ID [P] Membership (Page=1)

Table 82. PHY 0 Register 30: VLAN ID [P] Membership

Reg.bit	Name	Mode	Description	Default
30.[15:5]	Reserved			1111 1111 111
30.[4:0]	VLAN ID [P] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN P. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN P 10010 means port 4 and 1 are the members of VLAN P 11111 means all 5 ports are the members of VLAN P	1 0001

7.1.19. PHY 0 Register 31: Reserved or VLAN ID [P]

7.1.19.1 PHY 0 Register 31: Reserved Register (Page=0)

Table 83. PHY 0 Register 31: Reserved Register

Reg.bit	Name	Mode	Description	Default
31.[15:0]	Reserved			

7.1.19.2 PHY 0 Register 31: VLAN ID [P] (Page=1)

Table 84. PHY 0 Register 31: VLAN ID [P]

Reg.bit	Name	Mode	Description	Default
31.[15:12]	Reserved			1111
31.[11:0]	VLAN ID [P]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN P	0000 0000 1111

7.2. PHY 1 Registers

7.2.1. PHY 1 Register 0 for Port 1: Control

This register has the same definition as PHY 0 Register 0 for Port 0: Control, page 53.

7.2.2. PHY 1 Register 1 for Port 1: Status

This register has the same definition as PHY 0 Register 1 for Port 0: Status, page 54.

7.2.3. PHY 1 Register 2 for Port 1: PHY Identifier 1

This register has the same definition as PHY 0 Register 2 for Port 0: PHY Identifier 1, page 54.

7.2.4. PHY 1 Register 3 for Port 1: PHY Identifier 2

This register has the same definition as PHY 0 Register 3 for Port 0: PHY Identifier 2, page 55.

7.2.5. PHY 1 Register 4 for Port 1: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 for Port 0: Auto-Negotiation Advertisement, page 55.

7.2.6. PHY 1 Register 5 for Port 1: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 for Port 0: Auto-Negotiation Link Partner Ability, page 56.

7.2.7. PHY 1 Register 16~17: Internal Use Register

Table 85. PHY 1 Register 16~17: Internal Use Register

Reg.bit	Name	Mode	Description	Default
16	Internal Use	RW		0xFFFF
17	Internal Use	RW		0xFFFF

7.2.8. PHY 1 Register 18~19: Internal Use Register

Table 86. PHY 1 Register 18~19: Internal Use Register

Reg.bit	Name	Mode	Description	Default
18	Internal Use	RW		0xFFFF
19	Internal Use	RW		0xFFFF

7.2.9. PHY 1 Register 22: Port 1 Control Register 0

This register has the same definition as PHY 0 Register 22: Port 0 Control Register 0page 60.

Note: Reg 22.8 is pin DisPortPri[1] strap option for port 1. Default value for 22.8 is 1.

7.2.10. PHY 1 Register 23: Global Option Register 0

Table 87. PHY 1 Register 23: Global Option Register 0

Reg.bit	Name	Mode	Description	Default
23.15	Reserved			1
23.14	Internal Use	RW		0
23.[13:8]	Reserved			00 1111
23.7	Internal Use	RW		0
23.[6:5]	Reserved			10
23.4	Internal Use	RW		1
23.[3:0]	Reserved			1111

7.2.11. PHY 1 Register 24: Port 1 Control Register 1 & VLAN ID [B] Membership

Table 88. PHY 1 Register 24: Port 1 Control Register 1 & VLAN ID [B] Membership

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Port 1 VLAN index [3:0]	RW	In a port-based VLAN configuration, this register indexes to port 1's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to "VLAN ID [P] Membership". Port 1can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0001, which indexes to the VLAN entry [B] that is composed of VLAN ID [B] Membership Bit [4:0] in PHY1 Reg.24.[4:0] and VLAN ID [B] in PHY1 Reg.25.[11:0].	0001
24.11	Internal Use	RW		1
24.10	Internal Use	RW		1
24.9	Internal Use	RW		1
24.8	Internal Use	RO		0
24.7	Internal Use	RW		1
24.6	Internal Use	RW		1
24.5	Reserved			0

Reg.bit	Name	Mode	Description	Default
24.[4:0]	VLAN ID [B] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN B. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN B 10010 means port 4 and 1 are the members of VLAN B 11111 means all 5 ports are members of VLAN B	1 0010

7.2.12. PHY 1 Register 25: Port 1 Control Register 2 & VLAN ID [B]

Table 89. PHY 1 Register 25: Port 1 Control Register 2 & VLAN Entry [B]

Reg.bit	Name	Mode	Description	Default
25.15	Internal Use	RW		1
25.14	Internal Use	RW		1
25.13	Internal Use	RW		1
25.12	Internal Use	RW		1
25.[11:0]	VLAN ID [B]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN B	0000 0000 0001

7.2.13. PHY 1 Register 26: Reserved or VLAN ID [G] Membership

7.2.13.1 PHY 1 Register 26: Reserved Register (Page=0)

Table 90. PHY 1 Register 26: Reserved Register

Reg.bit	Name	Mode	Description	Default
26.[15:0]	Reserved			0x031F

7.2.13.2 PHY 1 Register 26: VLAN ID [G] Membership (Page=1)

Table 91. PHY 1 Register 26: VLAN ID [G] Membership

Reg.bit	Name	Mode	Description	Default
26.[15:5]	Reserved			1111 1111 111
26.[4:0]	VLAN ID [G] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN G. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for Port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN G 10010 means port 4 and 1 are the members of VLAN G 11111 means all 5 ports are members of VLAN G	1 0010

7.2.14. PHY 1 Register 27: Reserved or VLAN ID [G]

7.2.14.1 PHY 1 Register 27: Reserved Register (Page=0)

Table 92. PHY 1 Register 27: Reserved Register

Reg.bit	Name	Mode	Description	Default
27.[15:0]	Reserved			0x1F10

7.2.14.2 PHY 1 Register 27: VLAN ID [G] (Page=1)

Table 93. PHY 1 Register 27: VLAN ID [G]

Reg.bit	Name	Mode	Description	Default
27.[15:12]	Reserved			1111
27.[11:0]	VLAN ID [G]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN G	0000 0000 0110

7.2.15. PHY 1 Register 28: Reserved or VLAN ID [L] Membership

7.2.15.1 PHY 1 Register 28: Reserved Register (Page=0)

Table 94. PHY 1 Register 28: Reserved Register

Reg.bit	Name	Mode	Description	Default
28.[15:0]	Reserved			0x0012

7.2.15.2 PHY 1 Register 28: VLAN ID [L] Membership (Page=1)

Table 95. PHY 1 Register 28: VLAN ID [L] Membership

Reg.bit	Name	Mode	Description	Default
28.[15:5]	Reserved			1111 1111 111
28.[4:0]	VLAN ID [L] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN L. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN L 10010 means port 4 and 1 are the members of VLAN L 11111 means all 5 ports are members of VLAN L	1 0010

7.2.16. PHY 1 Register 29: Reserved or VLAN ID [L]

7.2.16.1 PHY 1 Register 29: Reserved (Page=0)

Table 96. PHY 1 Register 29: Reserved Register

Reg.bit	Name	Mode	Description	Default
29.[15:0]	Reserved			0x02C5

7.2.16.2 PHY 1 Register 29: VLAN ID [L] (Page=1)

Table 97. PHY 1 Register 29: VLAN ID [L]

Reg.bit	Name	Mode	Description	Default
29.[15:12]	Reserved			1111
29.[11:0]	VLAN ID [L]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN L	0000 0000 1011

7.3. PHY 2 Registers

7.3.1. PHY 2 Register 0 for Port 2: Control

This register has the same definition as PHY 0 Register 0 for Port 0: Control, page 53.

7.3.2. PHY 2 Register 1 for Port 2: Status

This register has the same definition as PHY 0 Register 1 for Port 0: Status, page 54.

7.3.3. PHY 2 Register 2 for Port 2: PHY Identifier 1

This register has the same definition as PHY 0 Register 2 for Port 0: PHY Identifier 1, page 54.

7.3.4. PHY 2 Register 3 for Port 2: PHY Identifier 2

This register has the same definition as PHY 0 Register 3 for Port 0: PHY Identifier 2, page 55.

7.3.5. PHY 2 Register 4 for Port 2: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 for Port 0: Auto-Negotiation Advertisement, page 55.

7.3.6. PHY 2 Register 5 for Port 2: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 for Port 0: Auto-Negotiation Link Partner Ability, page 56.

7.3.7. PHY 2 Register 16~17: Internal Use Register

Table 98. PHY 2 Register 16~17: Internal Use Register

Reg.bit	Name	Mode	Description	Default
16	Internal Use	RW		0xFFFF
17	Internal Use	RW		0xFFFF

7.3.8. PHY 2 Register 18~19: Internal Use Register

Table 99. PHY 2 Register 18~19: Internal Use Register

Reg.bit	Name	Mode	Description	Default
18	Internal Use	RW		0xFFFF
19	Internal Use	RW		0xFFFF

7.3.9. PHY 2 Register 22: Port 2 Control Register 0

This register has the same definition as PHY 0 Register 22: Port 0 Control Register 0, on page 60.

Note: Reg 22.8 is pin DisPortPri[2] strap option for port 2. Default value for 22.8 is 1.

7.3.10. PHY 2 Register 23: Global Option 1 Register

Table 100. PHY 2 Register 23: Global Option Register 1

Reg.bit	Name	Mode	Description	Default
23.[15:12]	Reserved			0000
23.11	Internal Use	RW		0
23.10	Internal Use	RW		0
23.9	Internal Use	RW		0
23.[8:0]	Reserved			0 0010 0000

7.3.11. PHY 2 Register 24: Port 2 Control Register 2 & VLAN ID [C] Membership

Table 101. PHY 2 Register 24: Port 2 Control Register 2 & VLAN ID [C] Membership

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Port 2 VLAN index [3:0]	RW	In a port-based VLAN configuration, this register indexes to port 2's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 2 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0010, which indexes to the VLAN entry [C] that is composed of VLAN ID [C] Membership Bit [4:0] in PHY2 Reg.24.[4:0], and VLAN ID [C] in PHY2 Reg.25.[11:0].	0010
24.11	Internal Use	RW		1
24.10	Internal Use	RW		1
24.9	Internal Use	RW		1
24.8	Internal Use	RO		0
24.7	Internal Use	RW		1
24.6	Internal Use	RW		1
24.5	Reserved			0

Reg.bit	Name	Mode	Description	Default
24.[8:0]	VLAN ID [C] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN C. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN C 10010 means port 4 and 1 are the members of VLAN C 11111 means all 5 ports are the members of VLAN C	1 0100

7.3.12. PHY 2 Register 25: Port 2 Control Register 3 & VLAN ID [C]

Table 102. PHY 2 Register 25: Port 2 Control Register 3 & VLAN ID [C]

Reg.bit	Name	Mode	Description	Default
25.15	Internal Use	RW		1
25.14	Internal Use	RW		1
25.13	Internal Use	RW		1
25.12	Internal Use	RW		1
25.[11:0]	VLAN ID [C]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN C	0000 0000 0010

7.3.13. PHY 2 Register 26: Reserved or VLAN ID [H] Membership

7.3.13.1 PHY 2 Register 26: Reserved Register (Page=0)

Table 103. PHY 2 Register 26: Reserved Register

Reg.bit	Name	Mode	Description	Default
26.[15:0]	Reserved			0x0052

7.3.13.2 PHY 2 Register 26: VLAN ID [H] Membership (Page=1)

Table 104. PHY 2 Register 26: VLAN ID [H] Membership

Reg.bit	Name	Mode	Description	Default
26.[15:5]	Reserved			1111 1111 111
26.[4:0]	VLAN ID [H] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN H. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN H 10010 means port 4 and 1 are the members of VLAN H 11111 means all 5 ports are the members of VLAN H	1 0100

7.3.14. PHY 2 Register 27: Reserved or VLAN ID [H]

7.3.14.1 PHY 2 Register 27: Reserved Register (Page=0)

Table 105. PHY 2 Register 27: Reserved Register

Reg.bit	Name	Mode	Description	Default
27.[15:0]	Reserved			0xA9CD

7.3.14.2 PHY 2 Register 27: VLAN ID [H] (Page=1)

Table 106. PHY 2 Register 27: VLAN ID [H]

Reg.bit	Name	Mode	Description	Default
27.[15:12]	Reserved			1111
27.[11:0]	VLAN ID [H]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN H	0000 0000 0111

7.3.15. PHY 2 Register 28: Reserved or VLAN ID [M] Membership

7.3.15.1 PHY 2 Register 28: Reserved Register (Page=0)

Table 107. PHY 2 Register 28: Reserved Register

Reg.bit	Name	Mode	Description	Default
28.[15:0]	Resreved			0xB029

7.3.15.2 PHY 2 Register 28: VLAN ID [M] Membership (Page=1)

Table 108. PHY 2 Register 28: VLAN ID [M] Membership

Reg.bit	Name	Mode	Description	Default
28.[15:5]	Reserved			1111 1111 111
28.[4:0]	VLAN ID [M] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN M. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN M 10010 means port 4 and 1 are the members of VLAN M 11111 means all 5 ports are the members of VLAN M	1 0100

7.3.16. PHY 2 Register 29: Reserved or VLAN ID [M]

7.3.16.1 PHY 2 Register 29: Reserved Register (Page=0)

Table 109. PHY 2 Register 29: Reserved Register

Reg.bit	Name	Mode	Description	Default
29.[15:0]	Reserved			0xB01F

7.3.16.2 PHY 2 Register 29: VLAN ID [M] (Page=1)

Table 110. PHY 2 Register 29: VLAN ID [M]

Reg.bit	Name	Mode	Description	Default
29.[15:12]	Reserved			1111
29.[11:0]	VLAN ID [M]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN M.	0000 0000 1100

7.4. PHY 3 Registers

7.4.1. PHY 3 Register 0 for Port 3: Control

This register has the same definition as PHY 0 Register 0 for Port 0: Control, page 53.

7.4.2. PHY 3 Register 1 for Port 3: Status

This register has the same definition as PHY 0 Register 1 for Port 0: Status, page 54.

7.4.3. PHY 3 Register 2 for Port 3: PHY Identifier 1

This register has the same definition as PHY 0 Register 2 for Port 0: PHY Identifier 1, page 54.

7.4.4. PHY 3 Register 3 for Port 3: PHY Identifier 2

This register has the same definition as PHY 0 Register 3 for Port 0: PHY Identifier 2, page 55.

7.4.5. PHY 3 Register 4 for Port 3: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 for Port 0: Auto-Negotiation Advertisement, page 55.

7.4.6. PHY 3 Register 5 for Port 3: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 for Port 0: Auto-Negotiation Link Partner Ability, page 56.

7.4.7. PHY 3 Register 16~18: Switch MAC Address

The Switch MAC address is used as the source address in MAC pause control frames.

Table 111. PHY 3 Register 16~18: Switch MAC Address

Reg.bit	Name	Mode	Description	Default
16	Switch MAC Address [47:32]	RW	16.[15:8] = Switch MAC Address Byte 4 16.[7:0] = Switch MAC Address Byte 5	0x5452
17	Switch MAC Address [31:16]	RW	17.[15:8] = Switch MAC Address Byte 2 17.[7:0] = Switch MAC Address Byte 3	0x834C
18	Switch MAC Address [15:0]	RW	18.[15:8] = Switch MAC Address Byte 0 18.[7:0] = Switch MAC Address Byte 1	0xC005

7.4.8. PHY 3 Register 19~21: Internal Use Register

Table 112. PHY 3 Register 19~21: Internal Use Register

Reg.bit	Name	Mode	Description	Default
19	Internal Use	RW		0x0000
20	Internal Use	RW		0x0000
21	Internal Use	RW		0x0000

7.4.9. PHY 3 Register 22: Port 3 Control Register 0

This register has the same definition as PHY 0 Register 22: Port 0 Control Register 0, on page 60.

Note: Reg 22.8 is pin DisPortPri[3] strap option for port 3. Default value for 22.8 is 1.

7.4.10. PHY 3 Register 24: Port 3 Control Register 1 & VLAN ID [D] Membership

Table 113. PHY 3 Register 24: Port 3 Control Register 1 & VLAN ID [D] Membership

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Port 3 VLAN index [3:0]	RW	In a port-based VLAN configuration, this register indexes to port 3's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 3 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0011, which indexes to the VLAN entry [D] that is composed of VLAN ID [D] Membership Bit [4:0] in PHY3 Reg.24.[4:0], and VLAN ID [D] in PHY3 Reg.25.[11:0].	0011
24.11	Internal Use	RW		1
24.10	Internal Use	RW		1
24.9	Internal Use	RW		1
24.8	Internal Use	RO		0
24.7	Internal Use	RW		From pin Default=1
24.6	Internal Use	RW		1
24.5	Reserved			0

Reg.bit	Name	Mode	Description	Default
24.[4:0]	VLAN ID [D] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN D. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN D 10010 means port 4 and 1 are the members of VLAN D 11111 means all 5 ports are the members of VLAN D	1 1000

7.4.11. PHY 3 Register 25: Port 3 Control Register 2 & VLAN ID [D]

Table 114. PHY 3 Register 25: Port 3 Control Register 2 & VLAN ID [D]

Reg.bit	Name	Mode	Description	Default
25.15	Internal Use	RW		1
25.14	Internal Use	RW		1
25.13	Internal Use	RW		1
25.12	Internal Use	RW		1
25[11:0]	VLAN ID [D]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN D	0000 0000 0011

7.4.12. PHY 3 Register 26: Reserved or VLAN ID [I] Membership

7.4.12.1 PHY 3 Register 26: Reserved Register (Page=0)

Table 115. PHY 3 Register 26: Reserved Register

Reg.bit	Name	Mode	Description	Default
26.[15:0]	Reserved			0x9668

7.4.12.2 PHY 3 Register 26: VLAN ID [I] Membership (Page=1)

Table 116. PHY 3 Register 26: VLAN ID [I] Membership

Reg.bit	Name	Mode	Description	Default
26.[15:5]	Reserved			1111 1111 111
26.[4:0]	VLAN ID [I] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN I. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN I 10010 means port 4 and 1 are the members of VLAN I 11111 means all 5 ports are the members of VLAN I	1 1000

7.4.13. PHY 3 Register 27: Reserved or VLAN ID [I]

7.4.13.1 PHY 3 Register 27: Reserved Register (Page=0)

Table 117. PHY 3 Register 27: Reserved Register

Reg.bit	Name	Mode	Description	Default
27.[15:0]	Reserved			0xA464

7.4.13.2 PHY 3 Register 27: VLAN ID [I] (Page=1)

Table 118. PHY 3 Register 27: VLAN ID [I]

Reg.bit	Name	Mode	Description	Default
27.[15:12]	Reserved			1111
27.[11:0]	VLAN ID [I]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN I	0000 0000 1000

7.4.14. PHY 3 Register 28: Reserved or VLAN ID [N] Membership

7.4.14.1 PHY 3 Register 28: Reserved Register (Page=0)

Table 119. PHY 3 Register 28: Reserved Register

Reg.bit	Name	Mode	Description	Default
28.[15:0]	Reserved			0x9458

7.4.14.2 PHY 3 Register 28: VLAN ID [N] Membership (Page=1)

Table 120. PHY 3 Register 28: VLAN ID [N] Membership

Reg.bit	Name	Mode	Description	Default
28.[15:5]	Reserved			1111 1111 111
28.[4:0]	VLAN ID [N] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN N. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN N 10010 means port 4 and 1 are the members of VLAN N 11111 means all 5 ports are the members of VLAN N	1 1000

7.4.15. PHY 3 Register 29: Reserved or VLAN ID [N]

7.4.15.1 PHY 3 Register 29: Reserved Register (Page=0)

Table 121. PHY 3 Register 29: Reserved Register

Reg.bit	Name	Mode	Description	Default
29.[15:0]	Reserved			0x2154

7.4.15.2 PHY 3 Register 29: VLAN ID [N] (Page=1)

Table 122. PHY 3 Register 29: VLAN ID [N]

Reg.bit	Name	Mode	Description	Default
29.[15:12]	Reserved			1111
29.[11:0]	VLAN ID [N]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN N.	0000 0000 1101

7.5. PHY 4 Registers

7.5.1. PHY 4 Register 0 for Port 4: Control

This register has the same definition as PHY 0 Register 0 for Port 0: Control, page 53.

7.5.2. PHY 4 Register 1 for Port 4: Status

This register has the same definition as PHY 0 Register 1 for Port 0: Status, page 54.

7.5.3. PHY 4 Register 2 for Port 4: PHY Identifier 1

This register has the same definition as PHY 0 Register 2 for Port 0: PHY Identifier 1, page 54.

7.5.4. PHY 4 Register 3 for Port 4: PHY Identifier 2

This register has the same definition as PHY 0 Register 3 for Port 0: PHY Identifier 2, page 55.

7.5.5. PHY 4 Register 4 for Port 4: Auto-Negotiation Advertisement

This register has the same definition as PHY 0 Register 4 for Port 0: Auto-Negotiation Advertisement, page 55.

7.5.6. PHY 4 Register 5 for Port 4: Auto-Negotiation Link Partner Ability

This register has the same definition as PHY 0 Register 5 for Port 0: Auto-Negotiation Link Partner Ability, page 56.

7.5.7. PHY 4 Register 16: Indirect Access Control

PHY 4 register 16 is used for reading or writing data to the MAC address table.

Table 123. PHY 4 Register 16: Indirect Access Control

Reg.bit	Name	Mode	Description	Default
16.[15:2]	Reserved			0000 0000 0000 00
16.1	Command execution	RW	1: Trigger a command to read or write lookup table 0: Indicate this command is done	0
16.0	Read or write operation	RW	1: Read cycle 0: Write cycle	0

7.5.8. PHY 4 Register 17~20: Indirect Access Data

Table 124. PHY 4 Register 17~20: Indirect Access Data

Reg.bit	Name	Mode	Description	Default
17	Indirect Data 0 [15:0]	RW	Indirect Data 0 [6] = If this bit is 1, indicates this entry is static and will never be aged out. If this bit is 0, indicates this entry is dynamically learned, aged, updated, and deleted. Indirect Data [5:4] = 2-bit counter for internal aging. (10->11->01->00) Indirect Data [3:0] = The source port of this Source MAC Address ID learned Indirect Data 0 [15:7] = Reserved.	0x00
18	Indirect Data 1 [15:0]	RW	Indirect Data 1 [15:8] = Source MAC Address [7:0] (Byte 5) Indirect Data 1 [7:0] = Source MAC Address [15:8] (Byte 4) Indirect Data 1 [1:0] and Indirect Data 1 [15:8] of this register also determine the Entry Index [9:0] in the lookup table of this accessed data. Indirect Data 1 [1:0] = Entry Index [9:8] Indirect Data 1 [15:8] = Entry Index [7:0] In the write cycle: Entry Index [9:0] indirectly maps to an entry in the lookup table for writing. The written data must be the Source MAC Address [47:10] and Entry Index [9:0]. In the read cycle: Entry Index [9:0] indirectly maps to an entry in the lookup table for reading. The read back data will be shown in Indirect Data 0, 1, 2, and 3.	0x00
19	Indirect Data 2 [15:0]	RW	Indirect Data 2 [7:0] = Source MAC Address [31:24] (Byte 3) Indirect Data 2 [15:8] = Source MAC Address [23:16] (Byte 2)	0x00
20	Indirect Data 3 [15:0]	RW	Indirect Data 3 [7:0] = Source MAC Address [47:40] (Byte 1) Indirect Data 3 [15:8] = Source MAC Address [39:32] (Byte 0)	0x00

7.5.9. PHY 4 Register 21: 802.1p Base Priority

Table 125. PHY 2 Register 20: 802.1p Base Priority

Reg.bit	Name	Mode	Description	Default
21.[15.13]	802.1p base priority	RW	Classifies priority for incoming IEEE 802.1Q packets, if IEEE 802.1p priority classification is enabled. 'User priority' is compared against this value. >=: Classify as high priority <: Classify as low priority	100
21.[12:7]	Reserved			0 0000 0
21.[6:4]	Internal Use	RW		100
21.3	Reserved			0
21.[2:0]	Internal Use	RW		000

7.5.10. PHY 4 Register 22: Port 4 Control Register 0

This register has the same definition as PHY 0 Register 22: Port 0 Control Register 0, on page 60.

Note: Reg 22.8 is not pin DisPortPri[4] strap option for port 4. Default value for 22.8 is 1.

7.5.11. PHY 4 Register 24: Port 4 Control Register 1 & VLAN ID [E] Membership

Table 126. PHY 4 Register 24: Port 4 Control Register 1 & VLAN ID [E] Membership

Reg.bit	Name	Mode	Description	Default
24.[15:12]	Port 4 VLAN index [3:0]	RW	In a port-based VLAN configuration, this register indexes to port 4's 'Port VLAN Membership', which can be defined in one of the registers 'VLAN ID [A] Membership' to 'VLAN ID [P] Membership'. Port 4 can only communicate with members within this VLAN. This register also indexes to a default Port VID (PVID) for each port. The PVID is used in tag insertion and filtering if the tagged VID is not the same as the PVID. The default value of this register is 0100, which indexes to the VLAN entry [E] that is composed of VLAN ID [E] Membership Bit [4:0] in PHY4 Reg.24.[4:0], and VLAN ID [E] in PHY4 Reg.25.[11:0].	0100
24.11	Internal Use	RW		1
24.10	Internal Use	RW		1
24.9	Internal Use	RW		1
24.8	Internal Use	RO		0
24.7	Internal Use	RW		1
24.6	Internal Use	RW		1
24.5	Reserved			0
24.[4:0]	VLAN ID [E] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN E. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN E 10010 means port 4 and 1 are the members of VLAN E 11111 means all 5 ports are the members of VLAN E	1 1111

7.5.12. PHY 4 Register 25: Port 4 Control Register 2 & VLAN ID [E]

Table 127. PHY 4 Register 25: Port 4 Control Register 2 & VLAN ID [E]

Reg.bit	Name	Mode	Description	Default
25.15	Internal Use	RW		1
25.14	Internal Use	RW		1
25.13	Internal Use	RW		1
25.12	Internal Use	RW		1
25.[11:0]	VLAN ID [E]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN E	0000 0000 0100

7.5.13. PHY 4 Register 26: Reserved or VLAN ID [J] Membership

7.5.13.1 PHY 4 Register 26: Reserved Register (Page=0)

Table 128. PHY 4 Register 26: Reserved Register

Reg.bit	Name	Mode	Description	Default
26.[15:0]	Reserved			0x07D0

7.5.13.2 PHY 4 Register 26: VLAN ID [J] Membership (Page=1)

Table 129. PHY 4 Register 26: VLAN ID [J] Membership

Reg.bit	Name	Mode	Description	Default
26.[15:5]	Reserved			1111 1111 111
26.[4:0]	VLAN ID [J] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN J. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN J 10010 means port 4 and 1 are the members of VLAN J 11111 means all 5 ports are the members of VLAN J	1 1111

7.5.14. PHY 4 Register 27: Reserved or VLAN ID [J]

7.5.14.1 PHY 4 Register 27: Reserved Register (Page=0)

Table 130. PHY 4 Register 27: Reserved Register

Reg.bit	Name	Mode	Description	Default
27.[15:0]	Reserved			

7.5.14.2 PHY 4 Register 27: VLAN ID [J] (Page=1)

Table 131. PHY 4 Register 27: VLAN ID [J]

Reg.bit	Name	Mode	Description	Default
27.[15:12]	Reserved			1111
27.[11:0]	VLAN ID [J]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN J	0000 0000 1001

7.5.15. PHY 4 Register 28: Reserved or VLAN ID [O] Membership

7.5.15.1 PHY 4 Register 28: Reserved Register (Page=0)

Table 132. PHY 4 Register 28: Reserved Register

Reg.bit	Name	Mode	Description	Default
28.[15:0]	Reserved			

7.5.15.2 PHY 4 Register 28: VLAN ID [O] Membership (Page=1)

Table 133. PHY 4 Register 28: VLAN ID [O] Membership

Reg.bit	Name	Mode	Description	Default
28.[15:5]	Reserved			1111 1111 111
28.[4:0]	VLAN ID [O] Membership Bit [4:0]	RW	This 5-bit field specifies which ports are the members of VLAN O. If a destination address look up fails, the packet associated with this VLAN will be broadcast to the ports specified in this field. Bit 0 stands for port 0, bit 4 stands for port 4. E.g.: 10001 means port 4 and 0 are the members of VLAN O 10010 means port 4 and 1 are the members of VLAN O 11111 means all 5 ports are the members of VLAN O	1 1111

7.5.16. PHY 4 Register 29: Reserved or VLAN ID [O]

7.5.16.1 PHY 4 Register 29: Reserved Register (Page=0)

Table 134. PHY 4 Register 29: Reserved Register

Reg.bit	Name	Mode	Description	Default
29.[15:0]	Reserved			

7.5.16.2 PHY 4 Register 29: VLAN ID [O] (Page=1)

Table 135. PHY 4 Register 29: VLAN ID [O]

Reg.bit	Name	Mode	Description	Default
29.[15:12]	Reserved			1111
29.[11:0]	VLAN ID [O]	RW	Defines the IEEE 802.1Q 12-bit VLAN identifier of VLAN O	0000 0000 1110

7.6. PHY 5 Registers

7.6.1. PHY 5 Register 0 for Port 4 MAC: Control

Note: This register only works in MII PHY and SNI PHY mode. In MII MAC mode, these registers have no meaning.

Table 136. PHY 5 Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RO	0: No reset allowed (permanently=0)	0
0.14	Loopback (digital loopback)	RO	0: Normal operation (permanently=0)	0
0.13	Speed Select	RW	1: 100Mbps 0: 10Mbps When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit can be set through SMI (Read/Write).	Pin P4SPDSTA strap option
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	Pin P4ANEG strap option
0.11	Power Down	RO	0: Normal operation (permanently=0)	0
0.10	Isolate	RO	0: Normal operation (permanently=0)	0
0.9	Restart Auto Negotiation	RO	0: Normal operation (permanently=0)	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation When NWay is enabled, this bit reflects the result of auto-negotiation (Read only). When NWay is disabled, this bit may be set through SMI (Read/Write).	Pin P4DUPSTA strap option
0.[7:0]	Reserved			0000 0000

7.6.2. PHY 5 Register 1 for Port 4 MAC: Status

Note: This register only works in MII PHY and SNI PHY mode. In MII MAC mode, these registers have no meaning.

Table 137. PHY 5 Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base_T4	RO	0: No 100Base-T4 capability	0
1.14	100Base_TX_FD	RO	1: 100Base-TX full duplex capable (permanently=1)	1
1.13	100Base_TX_HD	RO	1: 100Base-TX half duplex capable (permanently=1)	1
1.12	10Base_T_FD	RO	1: 10Base-TX full duplex capable (permanently=1)	1
1.11	10Base_T_HD	RO	1: 10Base-TX half duplex capable (permanently=1)	1
1.[10:7]	Reserved	RO		0
1.6	MF Preamble Suppression	RO	The RTL8305SC will accept management frames with preamble suppressed (permanently=1)	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed. MII Reg.4, 5 are valid if this bit is set (permanently=1)	1
1.4	Remote Fault	RO	0: No remote fault (permanently=0)	0
1.3	Auto-Negotiation Ability	RO	1: NWay auto-negotiation capable (permanently=1)	1
1.2	Link Status	RO	1: Link is established 0: Link is failed This bit reflects the status of pin P4LNKSTA# in real time.	Pin P4LNKSTA# strap option
1.1	Jabber Detect	RO	0: No Jabber detected (permanently=0)	0
1.0	Extended Capability	RO	1: Extended register capable (permanently=1)	1

7.6.3. PHY 5 Register 2 for Port 4 MAC: PHY Identifier 1

Table 138. PHY 5 Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively	0x001C

7.6.4. PHY 5 Register 3 for Port 4 MAC: PHY Identifier 2

Table 139. PHY 5 Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI	1100 10
3.[9:4]	Model Number	RO	Manufacturer's model number (05: Indicates RTL8305	00 0101
3.[3:0]	Revision Number	RO	Manufacturer's revision number (02: Indicates SC	0010

7.6.5. PHY 5 Register 4 for Port 4 MAC: Auto-Negotiation Advertisement

Note: This register only works in PHY mode MII and PHY mode SNI. In MAC mode MII, these registers have no meaning.

Table 140. PHY 5 Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Next Page enabled 0: Next Page disabled (Permanently=0)	0
4.14	Acknowledge	RO	Permanently=0.	0
4.13	Remote Fault	RO	1: Advertises that the RTL8305SC has detected a remote fault 0: No remote fault detected	0
4.[12:11]	Reserved	RO		0
4.10	Pause	RW	1: Advertises that the RTL8305SC possesses 802.3x flow control capability 0: No flow control capability	Pin P4FLCTRL strap option
4.9	100Base-T4	RO	Technology not supported (Permanently=0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	Pin P4DUPSTA and P4SPDSTA strap option
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	Pin P4SPDSTA strap option
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	Pin P4DUPSTA or P4SPDSTA strap option
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	0 0001

7.6.6. MII Port NWay Mode

Table 141. MII Port NWay Mode

Event	Description
Upon Reset	Strapping P4SPDSTA=1 and P4DUPSTA=1 → Reg0.13=1, Reg0.8=1 Strapping P4SPDSTA=1 and P4DUPSTA=0 → Reg0.13=1, Reg0.8=0 Strapping P4SPDSTA=0 and P4DUPSTA=1 → Reg0.13=0, Reg0.8=1 Strapping P4SPDSTA=0 and P4DUPSTA=0 → Reg0.13=0, Reg0.8=0 Defau1t value of Reg4.10 is strapped from pin P4FLCTRL Default value of Reg1.2 is strapped from pin P4LNKSTA# P4LNKSTA# pulled down → Reg1.2=1 P4LNKSTA# pulled up → Reg1.2=0
After Reset	If PHY 5 register 4 is configured as Reg4.8=1, Reg4.7=1, Reg4.6=1, Reg4.5=1, the RTL8305SC will reflect this configuration in PHY 8 register 0 as Reg0.13=1 and Reg0.8=1 If PHY 5 register 4 is configured as Reg4.8=0, Reg4.7=1, Reg4.6=1, Reg4.5=1, the RTL8305SC will reflect this configuration in PHY 8 register 0 as Reg0.13=1 and Reg0.8=0 If PHY 5 register 4 is configured as Reg4.8=0, Reg4.7=0, Reg4.6=1, Reg4.5=1, the RTL8305SC will reflect this configuration in PHY 8 register 0 as Reg0.13=0 and Reg0.8=1 If PHY 5 register 4 is configured as Reg4.8=0, Reg4.7=0, Reg4.6=0, Reg4.5=1, the RTL8305SC will reflect this configuration in PHY 8 register 0 as Reg0.13=0 and Reg0.8=0 If the CPU polls register 5, the RTL8305SC replies with the contents in register 4 If the CPU polls register 4, the RTL8305SC replies with the contents in register 4

7.6.7. MII Port Force Mode

Table 142. MII Port Force Mode

Event	Description
Upon Reset	Strapping P4SPDSTA=1 and P4DUPSTA=1 → Reg0.13=1, Reg0.8=1 Strapping P4SPDSTA=1 and P4DUPSTA=0 → Reg0.13=1, Reg0.8=0 Strapping P4SPDSTA=0 and P4DUPSTA=1 → Reg0.13=0, Reg0.8=1 Strapping P4SPDSTA=0 and P4DUPSTA=0 → Reg0.13=0, Reg0.8=0 Defau1t value of Reg4.10 is strapped from pin P4FLCTRL Default value of Reg1.2 is strapped from pin P4LNKSTA# P4LNKSTA# pulled down → Reg1.2=1 P4LNKSTA# pulled up → Reg1.2=0
After Reset	The CPU only writes register 0.13 and 0.8 to propose a link configuration, then reads register 1.2 to determine whether the link partner can accept this link configuration

8. Functional Description

8.1. Switch Core Functional Overview

8.1.1. Applications

The RTL8305SC is a 5-port Fast Ethernet switch controller that integrates memory, five MACs, and five physical layer transceivers for 10Base-T and 100Base-TX operation into a single chip. All ports support 100Base-FX, which shares pins (TX+-/RX+-) with UTP ports and needs no SD+/- pins, a development using Realtek proprietary technology. To compensate for the lack of auto-negotiation in 100Base-FX applications, the RTL8305SC can be forced into 100Base-FX half or full duplex mode, and can enable or disable flow control in fiber mode.

The five ports are separated into three groups (GroupX/GroupY/Port4) for flexible port configuration using strapping pins upon reset. The SetGroup pin is used to select the port numbers for GroupX and GroupY (SetGroup=1: GroupX = Port0; GroupY = Ports 1, 2, and 3. SetGroup=0: GroupX = Ports 0 and 1; GroupY = Ports 2 and 3). The GxMode/GyMode/P4Mode[1:0] pins are used to select the operation mode (UTP/FX for GroupX and GroupY, UTP/FX/PHY mode MII/PHY mode SNI/MAC mode MII for Port 4). Upon reset, in addition to using strapping pins, the RTL8305SC can be configured with an EEPROM or read/write operation by a CPU via the MDC/MDIO interface.

For more detailed system application circuits, refer to Application Information, page 141.

Note:
Upon Reset: Defined as a short time after the end of a hardware reset.
After Reset: Defined as the time after the specified 'Upon Reset' time.

8.1.2. Port 4

Operating Mode of Port 4

Each port has two parts: MAC and PHY. In UTP and FX mode, Port 4 uses both the MAC and internal PHY parts like the other ports. In other modes, Port 4 uses only the MAC part, which provides an external interface to connect to the external MAC or PHY. Two pins are used for these operation mode configurations: P4MODE[1:0].

Port 4 supports an external MAC interface which can be set to PHY mode MII, PHY mode SNI, or MAC mode MII to work with the external MAC of a routing engine, PHY of a HomePNA, or other physical layer transceiver.

If the MAC part of Port 4 connects with an external MAC, such as the processor of a router application, it will act as a PHY. This is PHY mode MII, or PHY mode SNI. In PHY mode MII or PHY mode SNI, Port 4 uses the MAC part only, and provides an external MAC interface to connect MACs of external devices. In order to connect both MACs, the MII of the switch MAC should be reversed into PHY mode.

If the MAC part of Port 4 connects with an external PHY, such as the PHY of a HomePNA application, Port 4 will act as a MAC. This is MAC mode MII. In MAC mode MII, Port 4 uses its MAC to connect to an external PHY and ignores the internal PHY part.

External MAC Interface

In order to act as a PHY when Port 4 is in PHY mode, some pins of the external MAC interface must be changed. For example, TXC are input pins for MAC, but output pins for PHY. The MTXC/PRXC pin is input for MAC mode and output for PHY mode. Refer to Figure 3, page 93 to check the relationship between the RTL8305SC and the external device.

Tip: Connect the input of the RTL8305SC to the output of the external device. The RTL8305SC has no RXER, TXER, and CRS pins for MII signaling. Because the RTL8305SC does not support pin CRS, it is necessary to connect the MTXEN/PRXDV (output) of PHY mode to both CRS and RXDV (input) of the external device.

Port 4 Status Pins

When P4MODE[1:0]=11, Port 4 can be either UTP or MAC mode MII. Port 4 will automatically detect the link status of UTP from the internal PHY, and the link status of MAC mode MII from both the TXC of the external PHY and from P4LNKSTA#. If both UTP and MII port are linked OK, UTP has higher priority and the RTL8305SC will ignore the signal of the MII port.

In UTP and FX mode, the internal PHY will provide the port status (Link/Speed/Duplex/Full Flow Control ability) in real time. In order to provide the initial configuration of Port 4's PHY (UTP or FX mode), four pins (P4ANEG, P4Full, P4Spd100, P4EnFC) are used to strap upon reset. However, three of these pins are also used for Port 4's MAC (the other three modes) in real time after reset (P4Spd100 -> P4SpdSta, P4Full -> P4DupSta, P4EnFC -> P4FLCTRL).

In the other three modes, four pins (P4LNKSTA#, P4SpdSta, P4DupSta, P4FLCTRL) are necessary in order to provide the port status to Port 4's MAC. That means that the external MAC or PHY should be forced to the same port status as Port 4's MAC.

Related Pins

When Port 4 is in UTP or FX mode, the LEDs of Port 4 are used to display PHY status. When Port 4 is in other modes, the LEDs of Port 4 are used to display MAC status.

Four parallel LEDs corresponding to port 4 can be tri-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM to 0. In UTP applications, this bit should be 1.

The SEL_MIIMAC# pin can be used to indicate MII MAC port active after reset for the purposes of UTP/MII auto-detection.

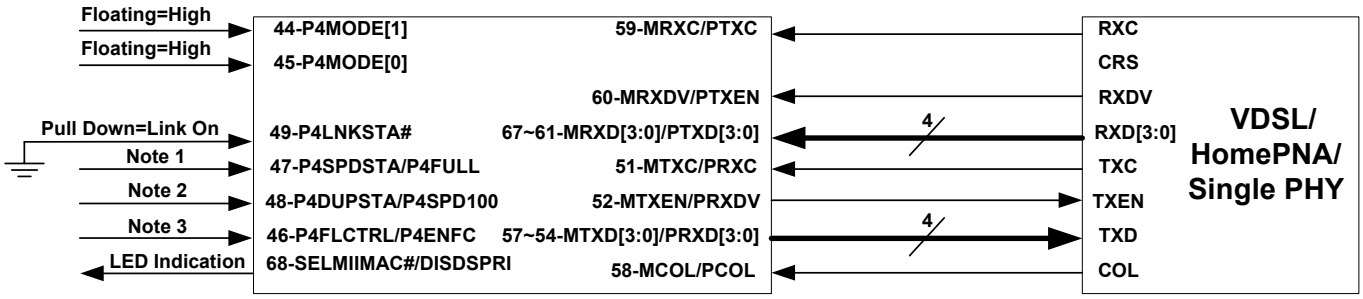
One 25MHz clock output (pin CK25MOUT) can be used as a clock source for the underlying HomePNA/other PHY physical devices.

PHY Mode MII/PHY Mode SNI

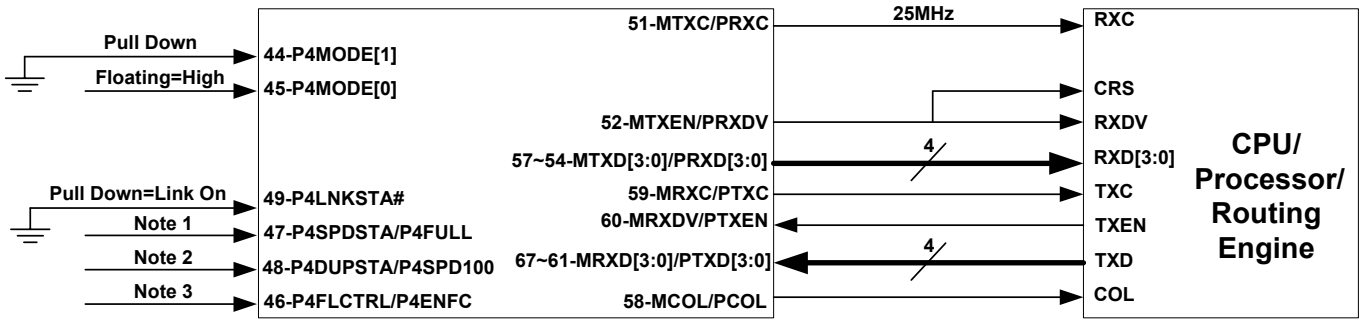
In routing applications, the RTL8305SC cooperates with a routing engine to communicate with the WAN (Wide Area Network) through MII/SNI. In such applications, P4LNKSTA# =0 and P4MODE[1] is pulled low upon reset. P4MODE[0] determines whether MII or SNI mode is selected.

In MII (nibble) mode (P4MODE[0]=1), P4SPDSTA=1 results in MII operating at 100Mbps with MTXC, and MRXC runs at 25MHz; however, P4SPDSTA=0 leads to MII operating at 10Mbps with MTXC, and MRXC runs at 2.5MHz.

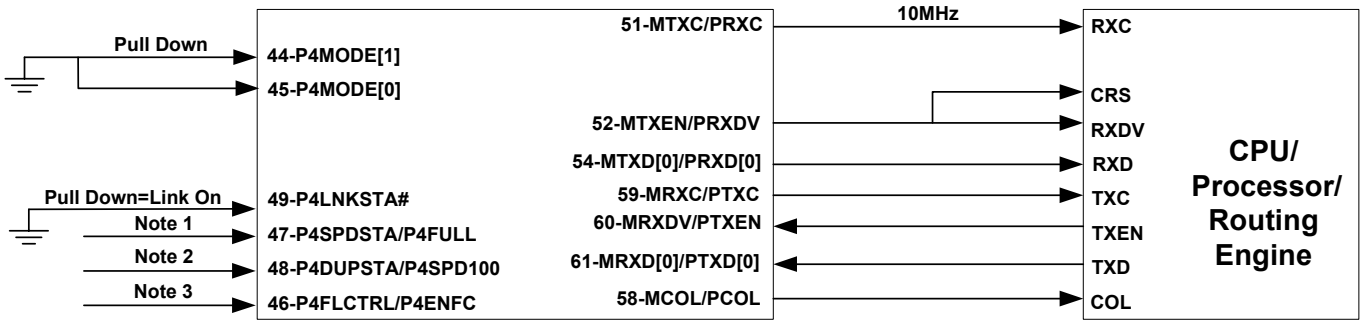
In SNI (serial) mode (P4MODE[0]=0), P4SPDSTA has no effect and should be pulled-down. SNI mode operates at 10Mbps only, with MTXC and MRXC running at 10MHz. In SNI mode the RTL8305SC does not loopback an RXDV signal as a response to TXEN, and does not support the heartbeat function (asserting COL signal for each complete TXEN signal).



MAC Mode MII



PHY Mode MII



PHY Mode SNI

Figure 3. Port 4 Operating Mode Overview

Note 1: Pulled high or floating to set speed to 100Mbps, and pulled low to set speed to 10Mbps.

Note 2: Pulled high or floating to set to full duplex, and pulled low to set to half duplex.

Note 3: Pulled high or floating to enable flow control in full duplex, and pulled low to disable.

MAC Mode MII

In HomePNA or other PHY applications, the RTL8305SC provides the MII interface to the underlying HomePNA or other physical device in order to communicate with other types of LAN media. In such applications, the P4MODE[1:0] pins are floating upon reset and the RTL8305SC supports the UTP/MII auto-detection function. When both UTP and MII are active (link on), the UTP port has higher priority than the MII port.

In HomePNA applications P4SPDSTA must be pulled down, as HomePNA is half-duplex only. P4DUPSTA should also be pulled down. P4LNKSTA# must be pulled down instead of being wired to the LINK LED pin of the HomePNA because of the unstable link state of HomePNA, a characteristic of the HomePNA 1.0 standard.

Because the HomePNA PHY physical layer is half duplex and can only detect a collision event during the AID header interval (the time when transmitting the Ethernet preamble), the back pressure flow control algorithm is not suitable for the HomePNA network and the P4FLCTRL pin should be pulled down.

For other PHY applications, P4SPDSTA, P4DUPSTA, and P4FLCTRL depend on the application.

8.1.3. Port Status Configuration

The RTL8305SC supports flexible port status configuration for PHY by pin (GxANeg/GyANeg/P4ANeg, GxSpd100/ GySpd100/P4Spd100, and GxFull/GyFull/P4Full) on a group basis upon reset, or by internal registers (Reg0.12, Reg0.13, Reg0.8, and Reg4.5/4.6/4.7/4.8) via SMI on a per-port basis after reset. Those pins are used to assign the initial value of MII register 0 and 4 (PHY registers) upon reset. The registers can be updated via SMI on a per-port basis after reset. For example, the initial value of register 0.12 of Port 4 will be 0 when pin P4Aneg is 1 upon reset.

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+- pins (Realtek patent). 100Base-FX can be forced into half or full duplex mode with optional flow control ability. In order to operate correctly, both sides of the connection should be set to the same settings. In 100Base-FX, duplex and flow control ability can be set via strapped pins upon reset, or via SMI after reset.

Note: In compliance with IEEE 802.3u, 100Base-FX does not support Auto-Negotiation.

Pins GxANeg/GyANeg/P4Aneg as well as GxSpd100/GySpd100/P4Spd100 are not used for 100Base-FX mode and can be left floating while in 100Base-FX mode. For example, Port 4 will be forced into full duplex 100Base-FX with flow control ability when P4Mode[1:0]=10, P4Full=1, P4EnFC=1 upon reset (regardless of P4Spd100 and P4ANeg).

When Auto-Negotiation ability is enabled in UTP mode, the RTL8305SC supports Auto-Negotiation and parallel detection of 10Base-T/100Base-TX to automatically determine line speed, duplex, and flow control. The parallel detection process is used when connecting a device that does not support auto-negotiation.

For example: port0 is UTP with all abilities (default for normal switch applications: GxMode=1, GxANeg=1, GxSpd100=1, GxFull=1, GxEnFC=1. The content of MII registers will be Reg0.12=1, Reg4.5=1, Reg4.6=1, Reg4.7=1, Reg4.8=1, and Reg4.10=1). If the connecting device supports auto-negotiation, 10Full with 802.3x flow control ability, port0 will enter the auto-negotiation process. The result will be 10Full with 802.3x flow control ability for both devices. If the other device is 10M without auto-negotiation, port0 will enter the parallel detection process. The result will be 10Half without 802.3x flow control ability for port0.

Note: Each port can operate at 10Mbps or 100Mbps in full-duplex or half-duplex mode independently of others when auto-negotiation is on.

The port status for the PHY on a group basis can easily be set by pin configuration. For example, when group X is 100FX (GxMode=0), group X can be set as force mode half duplex by setting pin GxFull to 0. Group Y can also be set as UTP mode NWAY mode 10Full by setting GyMode=1, GyANeg=1, GySpd100=0, GyFull=1. Refer to section 5 Pin Descriptions for details.

8.1.4. Flow Control

The RTL8305SC supports IEEE 802.3x full duplex flow control, Force mode Full duplex Flow Control, and optional half duplex back pressure.

IEEE 802.3x Full Duplex Flow Control

For UTP with auto-negotiation ability (GxANeg/GyANeg/P4Aneg set to 1), the pause ability (Reg.4.10) of full duplex flow control is enabled by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or internal registers via SMI on a per-port basis after reset. For UTP with auto-negotiation ability, IEEE 802.3x flow control's ability is auto-negotiated between the remote device and the RTL8305SC. If the auto-negotiation result of the 802.3x pause ability is 'Enabled' (Reg.4.10=1 and Reg.5.10=1), the full duplex 802.3x flow control function is enabled. Otherwise, the full duplex 802.3x flow control function is disabled.

Force Mode Full Duplex Flow Control

For UTP without auto-negotiation ability (GxANeg/GyANeg/P4Aneg is 0) and 100Base-FX, IEEE 802.3x flow control's ability can be forced to 'Enabled' by pins GxEnFC/GyEnFC/P4EnFC on a group basis upon reset, or internal registers (Reg.5.10) via SMI on a per-port basis after reset. For

example, port 4 will be forced to 10Full UTP with forced mode full duplex flow control ability, regardless of the connected device, when P4Mode[1:0]=10, P4Aneg=0, P4Spd100=0, P4Full=1, P4EnFC=1. Port 0 will be forced to 100Full FX with forced mode full duplex flow control ability, regardless of the connected device, when SetGroup=1, GxMode=0, GxFull=1, GxEnFC=1.

Regardless of IEEE 802.3x full duplex flow control or Force mode Full duplex Flow Control, when full duplex flow control is enabled, the RTL8305SC will only recognize the 802.3x flow control PAUSE ON/OFF frames with DA=0180C2000001, type = 8808, OP-code=01, PAUSE Time = maximum to zero, and with a good CRC.

If a PAUSE frame is received from any PAUSE flow control enabled port set to DA=0180C2000001, the corresponding port of the RTL8305SC will stop its packet transmission until the PAUSE timer times out or another PAUSE frame with zero PAUSE time is received. The RTL8305SC will not forward any 802.3x PAUSE frames received from any port.

Half Duplex Back Pressure

If pin EnDefer is 1, the RTL8305SC will send a preamble to defer the other station's transmission when there is no packet to send. Otherwise, if pin EnDefer is 0, the RTL8305SC will force a collision with the other station's transmission when the buffer is full.

If pin 48pass1 is 0, the RTL8305SC will always collide with JAM (Continuous collision). Otherwise, if pin 48pass1 is 1, the RTL8305SC will try to forward one packet successfully after 48 forced collisions (48pass1), to avoid the connected repeater being partitioned due to excessive collisions.

NWay Mode

For UTP with auto-negotiation ability, pins GxEnFC/GyEnFC/P4EnFC are effective only in full duplex mode. Therefore, for UTP in half duplex mode, half duplex back pressure flow control is controlled by the ENBKPRS pin strap upon hardware reset.

Force Mode

For UTP without auto-negotiation ability, or in 100Base-FX mode, the operation mode can be forced to half duplex. Half duplex back pressure flow control can be forced to 'enabled' on the RTL8305SC side by pin GxEnFC/GyEnFC/P4EnFC on a group basis upon reset.

8.1.5. Address Search, Learning, and Aging

When a packet is received, the RTL8305SC will use the least 10 bits of the destination MAC address to index the 1024-entry lookup table, and at the same time will compare the destination MAC address with the contents of the 16-entry CAM. If the indexed entry is valid, or the CAM comparison is matched, the received packet will be forwarded to the corresponding destination port. Otherwise, the RTL8305SC will broadcast the packet. This is the 'Address Search'.

The RTL8305SC then extracts the least 10 bits of the source MAC address to index the 1024-entry lookup table. If the entry is not already in the table it will record the source MAC address and add switching information. If this is an occupied entry, it will update the entry with new information. This is called 'Learning'. If the indexed location has been occupied by a different MAC address (hash collision), the new source MAC address will be recorded into the 16-entry CAM. The 16-entry CAM reduces address hash collisions and improves switching performance.

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The lookup engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8305SC is between 200 and 300 seconds.

8.1.6. Address Direct Mapping Mode

The RTL8305SC uses the least 10 bits of the MAC address to index the 1024-entry lookup table. For example: the index of MAC address '12 34 56 78 90 ab' will be 0xab.

8.1.7. Half Duplex Operation

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. A controlled randomization process called 'truncated binary exponential backoff' determines the scheduling of the retransmissions. At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slotTime (512 bit times). The number of slot times to delay before the n^{th} retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). IEEE 802.3 defines the backoffLimit as 10.

8.1.8. InterFrame Gap

The InterFrame Gap is 9.6μs for 10Mbps Ethernet and 960ns for 100Mbps Fast Ethernet.

8.1.9. Illegal Frame

Illegal frames such as CRC error packets, runt packets (length < 64 bytes), and oversize packets (length > maximum length), will be discarded.

8.1.10. Dual MII Interface

Home Gateways, broadband access routers, and SOHO routers generally contain a powerful Network Processor, with many I/O interfaces, including MII and SNI interfaces. Traditionally, this system connects one of the MII interfaces to a single PHY as the WAN port, and another interface connects to a multi-port switch as the LAN ports. In order to meet application demands, Realtek offers an advanced dual MII interface for this application. This eliminates the need for a single PHY.

Figure 4 shows the traditional design of a SOHO router. In this case, the router needs an extra single PHY as the WAN port. A traditional 5-port switch has five MAC and five PHY circuits on a single chip. When port 4 is configured as MII-MAC/MII-PHY/SNI-PHY, we only use the MAC part of port 4.

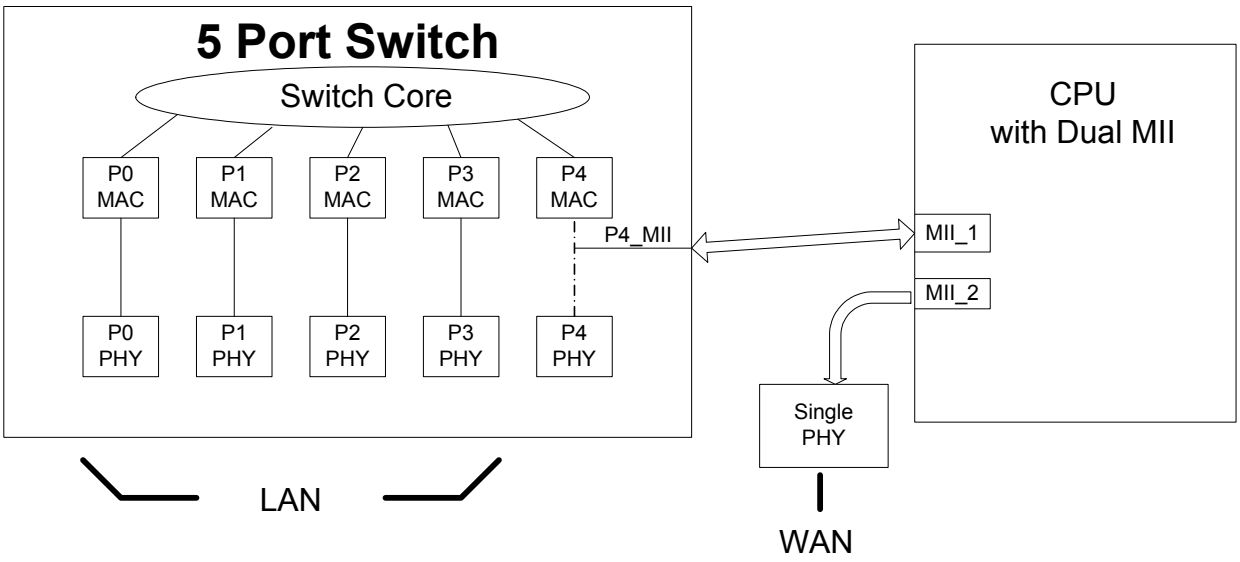


Figure 4. Traditional Application

The RTL8305SC has pin 42, DISDUALMII, to support both port 4 PHY and MAC circuits. When the Dual MII feature is enabled, the port 4 PHY may be used as the WAN interface as shown in Figure 5.

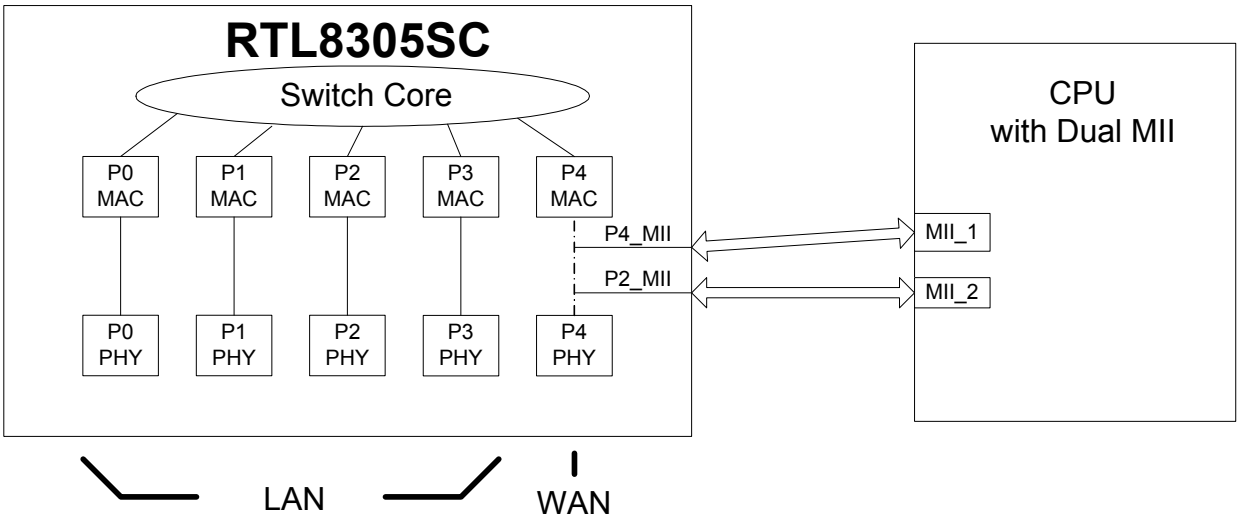


Figure 5. Dual MII Application Diagram

Dual MII Interfaces Configuration

Port 4 of the RTL8305SC is able to separate the MAC and PHY circuits via the DISDUALMII configuration. When DISDUALMII is configured as 0, the port 4 MAC circuit supports MAC mode MII, PHY mode MII, or PHY mode SNI interface. The port 4 PHY circuit supports an MII on the MAC side, and a UTP or fiber interface in the PHY transceiver. Four pins define the mode of the dual MII interface, DISDUALMII (pin-42), P4MODE[0] (pin-45), P4MODE[1] (pin-44), and P4PHY_MODE (pin-68).

- DISDUALMII: Enable dual MII interface feature, pull high = disable, and pull low = enable.
- P4MODE[1:0]: When DISDUALMII is enabled:
  11b/10b = P4MAC is MAC mode MII
  01b = P4MAC is PHY mode MII
  00b = P4MAC is PHY mode SNI
- P4PHY_MODE: When DISDUALMII is enabled:
  1b = P4PHY is UTP mode
  0b = P4PHY is Fiber mode

The following figures show the four types of configuration for the RTL8305SC with a CPU application.

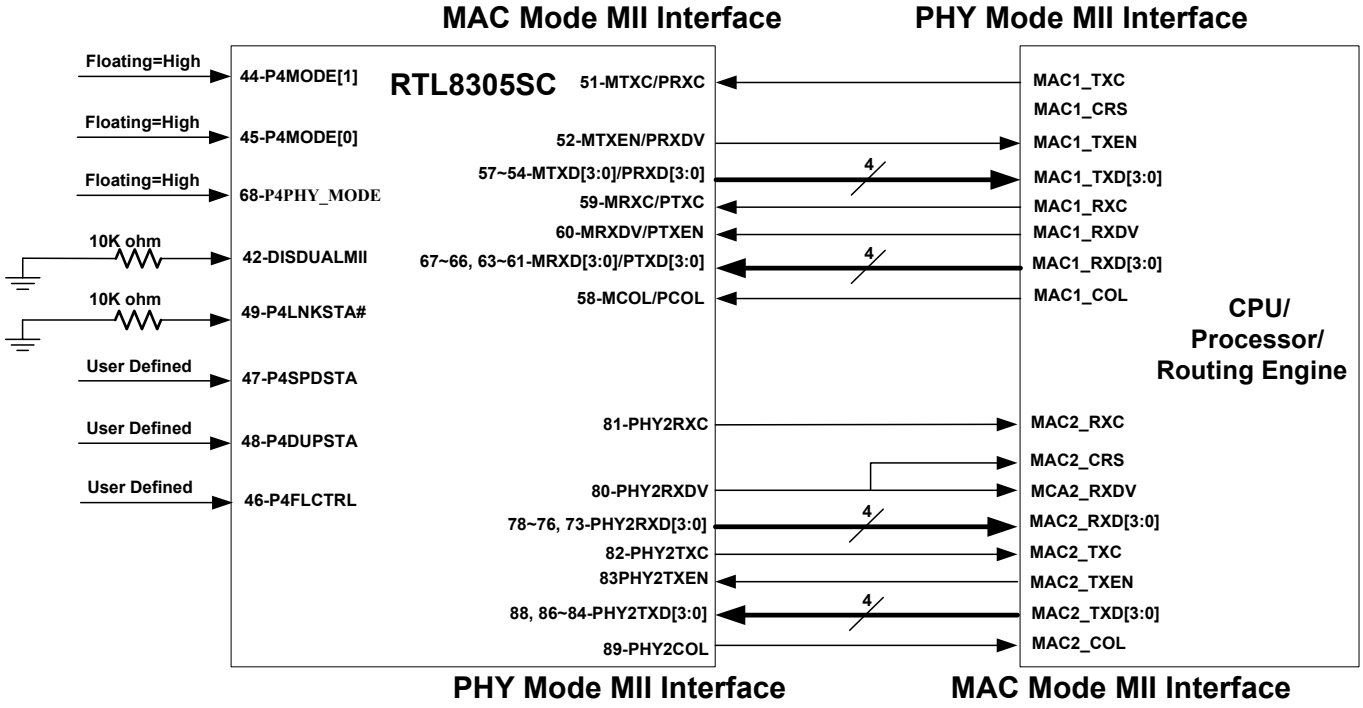


Figure 6. Dual MII Mode with 1 MII-MAC + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

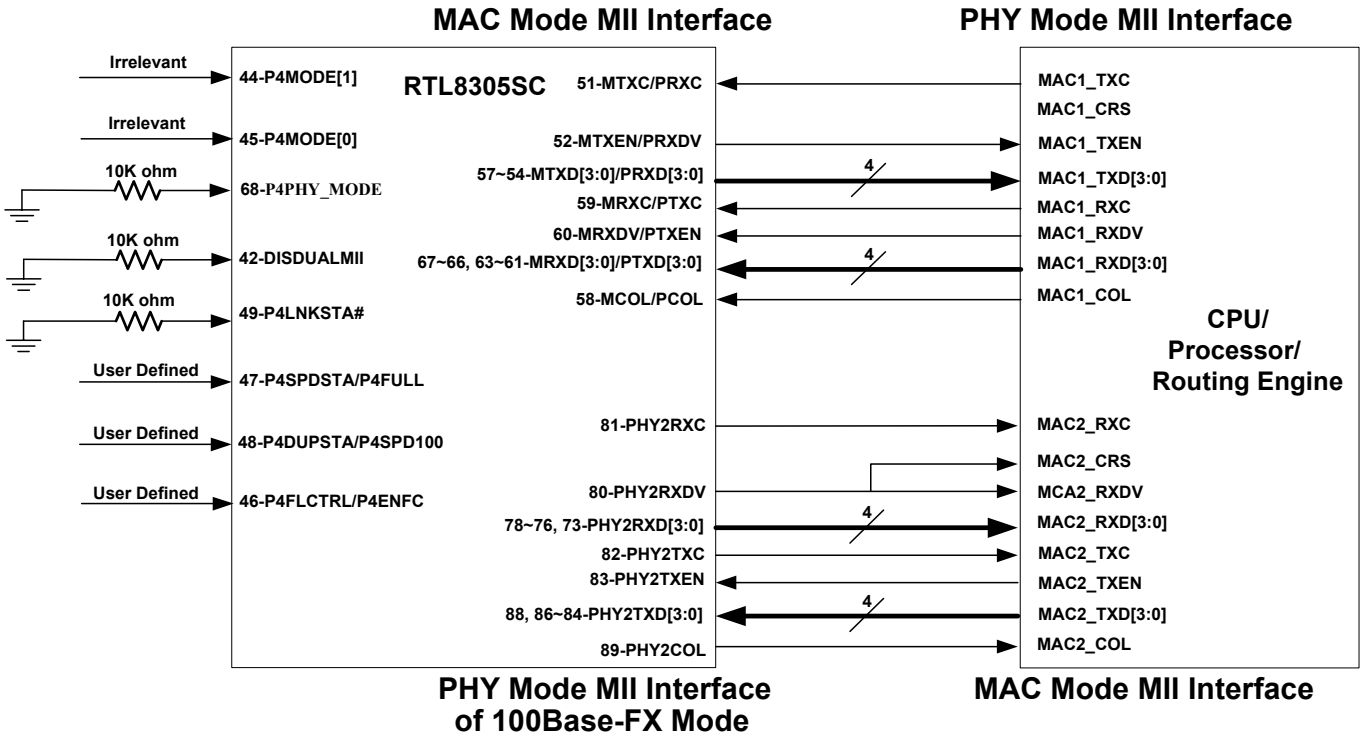


Figure 7. Dual MII Mode with 1 MII-MAC + 1 MII-PHY (100Base-FX Mode) Interfaces Application Circuit

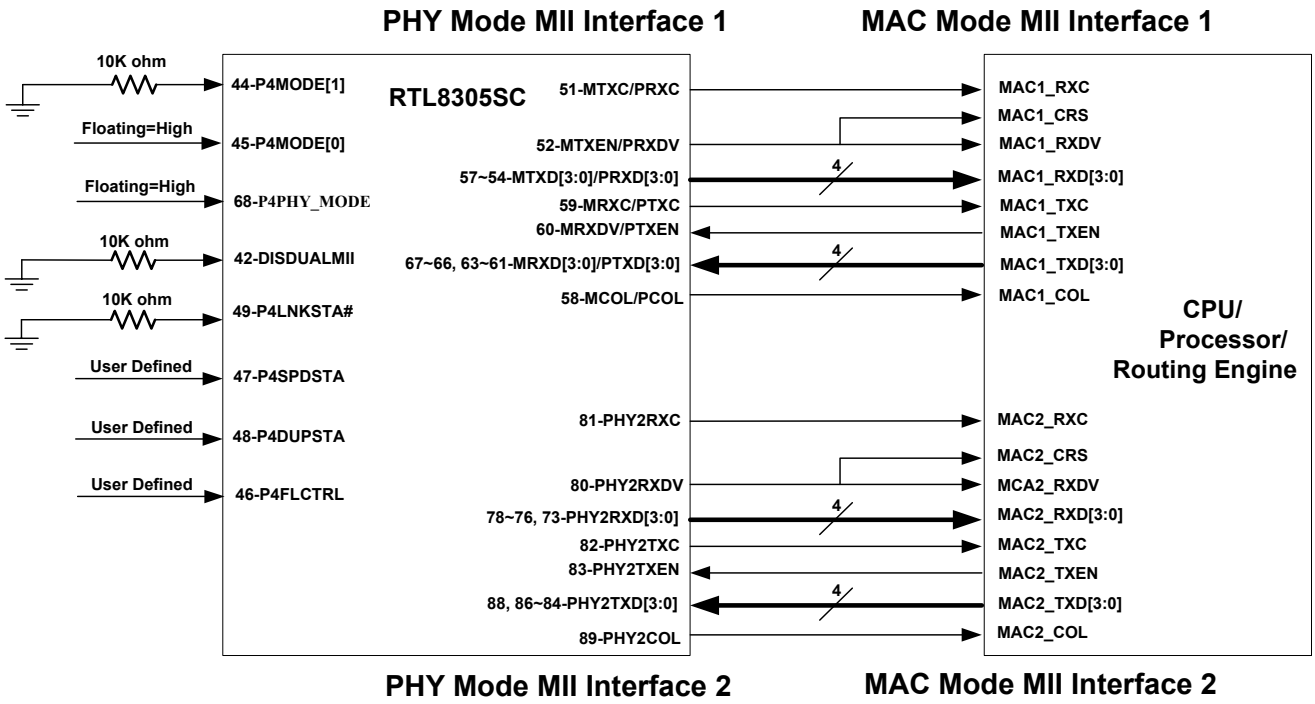


Figure 8. Dual MII Mode with 1 MII-PHY + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

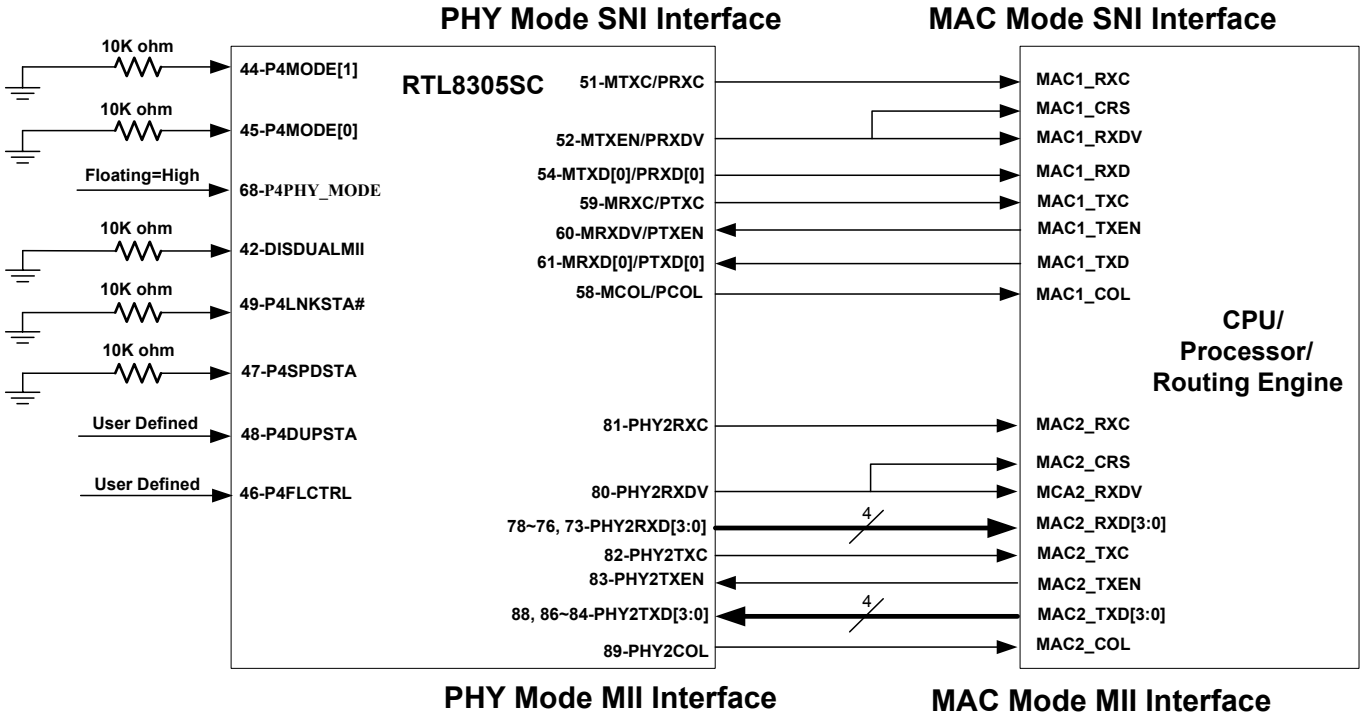


Figure 9. Dual MII Mode with 1 SNI-PHY + 1 MII-PHY (100Base-T UTP) Interfaces Application Circuit

Dual MII Registers Definition

For RTL8305SC single MII interface applications (DISDUALMII=1), PHY 5 MII registers represent the Port 4 MAC part.

For RTL8305SC dual MII interface applications (DISDUALMII=0), PHY4 registers represent the Port 4 PHY part (Read/Write), and PHY5 registers represent the Port 4 MAC part (Reg.013, 0.12, 0.8, 4.10, 4.8~4.5 are Read/Write; others are Read-Only). The 100Base-FX mode of the PHY circuit (P4MODE[1:0]=10) only supports 100Mbps and full duplex. The PHY circuit of UTP mode only supports full ability NWay (Flow control enabled, both 10/100Mbps, both Full/Half duplex).

The RTL8305SC support four status pins to provide the link status or initial configuration for the MAC circuit. A brief description of the function follows:

- P4LNKSTA#: Determines the link status of Port 4 MAC in real-time
- P4SPDSTA: Provides initial configuration pin for speed ability upon reset
- P4DUPSTA: Provides initial configuration pin for duplex ability upon reset
- P4FLCTRL: Provides initial configuration pin for flow control ability upon reset

Table 143 shows the MII PHY registers of PHY4 and PHY5 definitions when P4MODE[1:0] and DISDUALMII are configured in various combinations.

Table 143. MII Register Definition for PHY 4 and PHY 5

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th colspan="2">Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>1</td><td>11</td><td>P4LNKSTA#=1 or P4LNKSTA#=0 but UTP link on:</td><td>UTP</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=Signal detection and latch low
Reg. 4.10=P4FLCTRL
Reg. 4.8~4.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
Reg. 5.10=NWay result
Reg. 5.8~5.5=NWay result

After Reset:
All RW pins should be fully configurable and act as standard.</td><td>N/A</td><td>UTP</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th colspan="2">Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td></td><td></td><td>P4LNKSTA#=0 and UTP link off:</td><td>MAC: MAC mode MII
PHY: N/A
UTP: N/A</td><td>N/A</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5=Keep the contents identical to Reg. 4.10 and 4.8~4.5.</td><td>Port 4 MAC</td></tr>
<tr><td>1</td><td>10</td><td colspan="2">MAC: N/A
PHY: N/A
UTP: 100Base-FX (Fiber)</td><td>Upon Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=0 (NWay=Disable)
Reg. 0.8=P4DUPSTA
Reg. 1.2=Signal detection
Reg. 4.10=P4FLCTRL
Reg. 4.8~4.5=1111
Reg. 5.10=Reg. 4.10
Reg. 5.8~5.5= Reg. 4.8~4.5

After Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=0 (NWay=Disable)
Reg. 0.8=Configurable
Reg. 1.2=Signal detection
Reg. 4.10=Configurable
Reg. 4.8~4.5=1111
Reg. 5.10=Reg. 4.10
Reg. 5.8~5.5=Reg. 4.8~4.5</td><td>N/A</td><td>Fiber</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>1</td><td>01</td><td>MAC: PHY mode MII
PHY: N/A
UTP: N/A</td><td>N/A</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5= Keep the contents identical to Reg. 4.10 and 4.8~4.5.</td><td>Port 4 MAC</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>1</td><td>00</td><td>MAC: PHY mode SNI
PHY: N/A
UTP: N/A</td><td>N/A</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5= Keep the contents identical to Reg. 4.10 and 4.8~4.5.</td><td>Port 4 MAC</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>0</td><td>11</td><td>P4PHY_MODE (pin 68)=1
MAC: MAC mode MII
PHY: PHY mode MII
UTP: 100Base-TX</td><td>Upon Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=1 (NWay=Enable)
Reg. 0.8=1 (Duplex=Full)
Reg. 1.2=Signal detection and latch low
Reg. 4.10=1 (Enable Fctrl)
Reg. 4.8~4.5=1111
Reg. 5.10=Depends on NWay result
Reg. 5.8~5.5=Depends on NWay result

After Reset:
All RW pins should be fully configurable and act as standard.</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5=Keep the contents identical to Reg. 4.10 and 4.8~4.5</td><td>Port 4 PHY</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>0</td><td>10</td><td>P4PHY_MODE (pin 68)=0
MAC: MAC mode MII
PHY: PHY mode MII
UTP: 100Base-FX (Fiber)</td><td>Upon Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=0 (NWay=Disable)
Reg. 0.8=1 (Duplex=Full)
Reg. 1.2=Signal detection and latch low
Reg. 4.10=1 (Enable Fctrl)
Reg. 4.8~4.5=1111
Reg. 5.10=1
Reg. 5.8~5.5=1111

After Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=0 (NWay=Disable)
Reg. 0.8=Configurable
Reg. 1.2=Signal detection
Reg. 4.10=Configurable
Reg. 4.8~4.5=1111
Reg. 5.10=Reg. 4.10
Reg. 5.8~5.5=1111</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5=Keep the contents identical to Reg. 4.10 and 4.8~4.5</td><td>Fiber</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>0</td><td>01</td><td>MAC: PHY mode MII
PHY: PHY mode MII
UTP: 100Base-TX</td><td>Upon Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=1 (NWay=Enable)
Reg. 0.8=1 (Duplex=Full)
Reg. 1.2=Signal detection and latch low
Reg. 4.10=1 (Enable Fctrl)
Reg. 4.8~4.5=1111
Reg. 5.10=Depends on NWay result
Reg. 5.8~5.5=Depends on NWay result

After Reset:
All RW pins should be fully configurable and act as standard.</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
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<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5=Configurable
Reg. 5.10 and 5.8~5.5=Keep the contents identical to Reg. 4.10 and 4.8~4.5</td><td>Port 4 PHY</td></tr>
</table>

<table>
<tr><th>Dis DualMII</th><th>P4MODE [1:0]</th><th>Port 4 Mode</th><th>PHY4 (Single Mode MII) (Reg0, 1, 2, 3, 4, 5)</th><th>PHY5 (Reg0, 1, 2, 3, 4, 5)</th><th>Port 4 LED</th></tr>
<tr><td>0</td><td>00</td><td>MAC: PHY mode SNI
PHY: PHY mode MII
UTP: 100Base-TX</td><td>Upon Reset:
Reg. 0.13=1 (Speed=100M)
Reg. 0.12=1 (NWay=Enable)
Reg. 0.8=1 (Duplex=Full)
Reg. 1.2=Signal detection and latch low
Reg. 4.10=1 (Enable Fctrl)
Reg. 4.8~4.5=1111
Reg. 5.10=Depends on NWay result
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After Reset:
All RW pins should be fully configurable and act as standard.</td><td>Upon Reset:
Reg. 0.13=P4SPDSTA
Reg. 0.12=P4ANEG
Reg. 0.8=P4DUPSTA
Reg. 1.2=P4LNKSTA#
Reg. 4.10=P4FLCTRL
Reg. 5.10=P4FLCTRL
Reg. 4.8~4.5=Reg. 5.8~5.5=
<table>
<tr><th>Reg. 4.8~4.5</th><th>P4 SPDSTA</th><th>P4 DUPSTA</th></tr>
<tr><td>1111</td><td>1</td><td>1</td></tr>
<tr><td>0111</td><td>1</td><td>0</td></tr>
<tr><td>0011</td><td>0</td><td>1</td></tr>
<tr><td>0001</td><td>0</td><td>0</td></tr>
</table>
After Reset:
Reg. 0.13=Configurable
Reg. 0.12=Configurable
Reg. 0.8=Configurable
Reg. 1.2=P4LNKSTA#
Reg. 4.10 and 4.8~4.5= Configurable
Reg. 5.10 and 5.8~5.5=Keep the contents identical to Reg. 4.10 and 4.8~4.5</td><td>Port 4 PHY</td></tr>
</table>

8.2. Physical Layer Functional Overview

8.2.1. Auto-Negotiation for UTP

The RTL8305SC obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3u specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8305SC advertises full capabilities (100Full, 100Half, 10Full, 10Half) together with flow control ability.

8.2.2. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven into the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

8.2.3. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

8.2.4. Link Monitor

The 10Base-T link pulse detection circuit continually monitors the RXIP/RXIN pins for the presence of valid link pulses. Auto-polarity is implemented to correct the detected reverse polarity of RXIP/RXIN signal pairs.

8.2.5. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven into the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

8.2.6. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A De-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

8.2.7. 100Base-FX

All ports support 100Base-FX, which shares pins with UTP (TX+-/RX+-) and needs no SD+- pins. 100Base-FX can be forced to half or full duplex with optional flow control ability.

Note: In compliance with IEEE 802.3u, 100Base-FX does not support Auto-Negotiation. In order to operate correctly, both sides of the connection should be set to the same duplex and flow control ability.

A scrambler is not needed in 100Base-FX. Compared to common 100Base-FX applications, the RTL8305SC removes a pair of differential SD (Signal Detect) signals that provide a link monitoring function, which reduces the pin count (Realtek patent).

8.2.8. 100Base-FX Transmit Function

In 100Base-FX transmission, di-bits of TXD are processed as 100Base-TX except without being scrambled before the NRZI stage. Instead of converting to MLT-3 signals as in 100Base-TX, the serial data stream is driven out as NRZI PECL (Positive Emitter Coupled Logic) signals, which enter the fiber transceiver in differential-pairs form. The fiber transceiver may be 3.3V or 5V capable. Refer to 100Base-FX Application, on page 143 for an example application.

Table 144. PECL DC Characteristics

Parameter	Symbol	Min	Max	Unit
PECL Input High Voltage	Vih	Vdd-1.16	Vdd-0.88	V
PECL Input Low Voltage	Vil	Vdd-1.81	Vdd-1.47	V
PECL Output High Voltage	Voh	Vdd-1.02		V
PECL Output Low Voltage	Vol		Vdd-1.62	V

8.2.9. 100Base-FX Receive Function

Signals are received through Positive Emitter Coupled Logic (PECL) receiver inputs from a fiber transceiver and directly passed to a clock recovery circuit for data/clock recovery. Scrambling/de-scrambling is bypassed in 100Base-FX.

8.2.10. 100Base-FX FEFI

When 100FX is enabled, PHY Reg.1.4 (Remote Fault) is the Far-End-Fault-Indicator (FEFI) bit for ports, and indicates that a FEFI has been detected. The FEFI is an alternative in-band signaling that is composed of 84 consecutive 1's followed by one 0. When the RTL8305SC has detected this pattern three times, Reg.1.4 will be set, which means the transmit path (Remote side's receive path) has problems. On the other hand, to send an FEFI stream pattern, the following condition needs to be satisfied; the incoming signal causes link failure, which in turn causes the remote side to detect a Far-End-Fault. This means that the receive path has a problem from the view of the RTL8305SC. The FEFI mechanism is used only in 100Base-FX.

During detection of the FEFI, PHY Reg.1.4 should be set to 1. It should remain 1, even after it is read, as long as FEFI is continuously detected by the RTL8305SC. PHY Reg.1.4 should not be cleared until the FEFI has disappeared.

If there is no FEFI, then PHY Reg.1.4 should be 0. In normal conditions where there is no optical or electrical input signal; OPT-PHY should not detect Far-End-Fault signals since there is no such signal at the optical input.

When Optical Receiving Fiber is disconnected from RTL8305SC, the FEFI cannot be detected by the RTL8305SC and also cannot be reflected on PHY Reg.1.4 since there is no FEFI. If there is a FEFI before Optical Receiving Fiber is disconnected, Reg.1.4 should be kept on 1. This bit should be cleared to 0 after it is read (read and clear).

The OPT-PHY of RTL8305SC will not reflect the FEFI (Reg.1.4=1) when Optical Fiber is disconnected at power up, in spite of No-Far-End-Fault signals. After power on, the default value of PHY Reg1.4 will appear as '0'.

8.2.11. Reduced Fiber Interface

The RTL8305SC ignores the underlying SD signal of the fiber transceiver to complete link detection and connection. This is achieved by monitoring RD signals from the fiber transceiver and checking whether any link integrity events are met. This significantly reduces pin-count, especially for high-port PHY devices. This is a Realtek patent-pending technology and available only with Realtek product solutions.

8.2.12. Power Saving Mode

The RTL8305SC implements power saving mode on a per-port basis. A port automatically enters power saving mode 10 seconds after the cable is disconnected from it. Once a port enters power saving mode, it transmits normal link pulses only on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be the 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects any incoming signals, it wakes up from power saving mode and operates in normal mode according to the result of the connection.

8.2.13. Reg0.11 Power-Down Mode

The RTL8305SC implements power-down mode on a per-port basis. Setting MII Reg.0.11 forces the corresponding port of the RTL8305SC to enter power-down mode. This disables all transmit/receive functions, except SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface).

8.2.14. Crossover Detection and Auto Correction

During the link setup phase, the RTL8305SC checks whether it receives active signals on every port in order to determine if a connection can be established. In cases where the receiver data pin pair is connected to the transmitter data pin pair of the peer device and vice versa, the RTL8305SC automatically changes its configuration and swaps receiver/transmitter data pins as required. If a port is connected to a PC or NIC with MDI-X interface with a crossover cable, the RTL8305SC will reconfigure the port to ensure proper connection. This replaces the DIP switch commonly used for reconfiguring a port on a hub or switch.

By pulling-up EN_AUTOXOVER, the RTL8305SC identifies the type of connected cable and sets the port to MDI or MDIX. When switching to MDI mode, the RTL8305SC uses TXOP/N as transmit pairs; when switching to MDIX mode, the RTL8305SC uses RXIP/N as transmit pairs. This function is port-based. Pulling-down EN_AUTOXOVER disables this function, the RTL8305SC operates in MDI mode, in which TXOP/N represents transmit pairs, and RXIP/N represents receive pairs.

IEEE 802.3 compliant forced mode 100M ports with Autoxover have link issues with NWay (Auto-Negotiation) ports. It is recommended to *not* use Autoxover for forced 100M.

8.2.15. Polarity Detection and Correction

For better noise immunity and lower interference to ambient devices, the Ethernet electrical signal on a twisted pair cable is transmitted in differential form. That is, the signal is transmitted on two wires in each direction with inverse polarities (+/-). If wiring on the connector is faulty or a faulty transformer is used, the two inputs to a transceiver may carry signals with opposite but incorrect polarities. As a direct consequence, the transceiver will not work properly.

When the RTL8305SC operates in 10Base-T mode, it automatically reverses the polarity of its two receiver input pins if it detects that the polarities of the incoming signals on the pins is incorrect. However, this feature is unnecessary when the RTL8305SC is operating in 100Base-TX mode.

8.3. Advanced Functional Overview

8.3.1. Reset

The whole or just part of the RTL8305SC is initialized depending on the reset type. There are several ways to reset the RTL8305SC: hardware reset for the whole chip by pin RESET#, soft reset for all except PHY by register SoftReset, and PHY software reset for each PHY by register reset.

Hardware Reset: Pin RESET#=0 set to RESET#=1 (for at least 1ms). The RTL8305SC resets the whole chip and then gets initial values from pins and serial EEPROM.

Soft Reset: Write bit12 of Reg16 of PHY0 as 1. The RTL8305SC resets all except PHY and does not load EEPROM and Pin Registers with serial EEPROM and Pins. The SoftReset, EEPROM, and Pin registers are designed to provide a convenient way for users who want to use SMI to change the configuration. After changing the EEPROM or Pin registers via SMI (Serial Management Interface), the external device has to perform a soft reset in order to update the configuration.

PHY Software Reset: Write bit15 of Reg0 of a PHY as 1. The RTL8305SC will then reset this PHY.

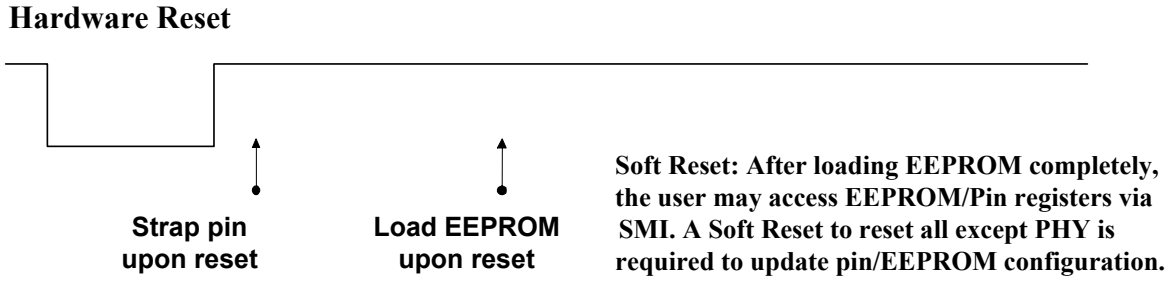


Figure 10. Reset

Some setting values for operation modes are latched from those corresponding mode pins upon hardware reset. ‘Upon reset’ is defined as a short time after the end of a hardware reset. Other advanced configuration parameters may be latched from serial EEPROM if pin EnEEPROM=1.

8.3.2. Setup and Configuration

The RTL8305SC can be configured easily and flexibly by hardware pins upon reset, optional serial EEPROM upon reset, and internal registers (including PHY registers for each port and MAC register for global) via SMI (Serial Management Interface: MDC/MDIO, also known as MII Management Interface). There are three methods of configuration:

1. Only hardware pins for normal switch applications
2. Hardware pins and serial EEPROM for advanced switch applications
3. Hardware pins and internal registers via SMI for applications with processor

Three types of pins, each with internal pull-high resistors, are used for configuration:

1. Input pins used for strapping upon reset (unused after reset)
2. Input/Output pins (MTXD[3:2]/PRXD[3:2]/P4IRTag[1:0], MTXD[1:0]/PRXD[1:0]/LEDMode[1:0]) used for strapping upon reset and used as output pins after reset
3. Input/Output pins (all LEDs) used for strapping upon reset and used as LED indicator pins after reset. The LED statuses are represented as active-low or high depending on input strapping, except Bi-color Link/Act in Bi-color LED mode, whose polarity depends on Spd status

Pins with default value=1 are internal pull-high and use I/O pads. They can be left floating to set input value as high, but should not be connected to GND without a pull-down resistor.

The serial EEPROM shares two pins, SCL_MDC and SDA_MDIO, with SMI, and is optional for advanced configuration. SCL_MDC and SDA_MDIO are tri-state during hardware reset (pin RESET#=0). The RTL8305SC will try to automatically find the serial EEPROM upon reset only if pin EnEEPROM=1. If the first byte of the serial EEPROM is not 0xFF (NoEEPROM bit of the first byte=0), the RTL8305SC will load all contents of the serial EEPROM into internal registers. Otherwise, the RTL8305SC will use the default internal values.

Internal registers can still be accessed after reset via SMI (pin SCL_MDC and SDA_MDIO). Serial EEPROM signals and SMI signals must not exist at the same time. In order to use the SMI to flexibly change configuration, internal registers include the contents of some pins and all serial EEPROM. These registers do not work in real time and a Soft Reset is necessary after changing the EEPROM or pin registers.

8.3.3. Serial EEPROM Example: 24LC02

The 24LC02 interface is a 2-wire serial EEPROM interface providing 2K bits of storage space. The 24LC02 must be 3.3V compatible.

8.3.3.1 24LC02 Device Operation

Clock and Data transitions: The SDA pin is normally pulled high with an external resistor. Data on the SDA pin may change only during SCL low time periods. Data changes during SCL high periods will indicate a start or stop condition as defined below.

Start Condition: A high-to-low transition of SDA with SCL high is the start condition and must precede any other command.

Stop Condition: A low-to-high transition of SDA with SCL high is a stop condition.

Acknowledge: All addresses and data are transmitted serially to and from the EEPROM in 8-bit words. The 24LC02 sends a zero to acknowledge that it has received each word. This happens during the ninth clock cycle.

Random Read: A random read requires a 'dummy' byte write sequence to load in the data word address.

Sequential Read: For the RTL8305SC, the sequential reads are initiated by a random address read. After the 24LC02 receives a data word, it responds with an acknowledgement. As long as the 24LC02 receives an acknowledgement, it will continue to increment the data word address and clock out sequential data words in series.

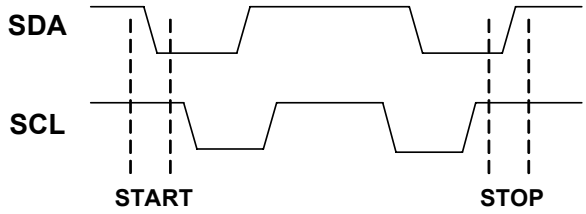


Figure 11. Start and Stop Definition

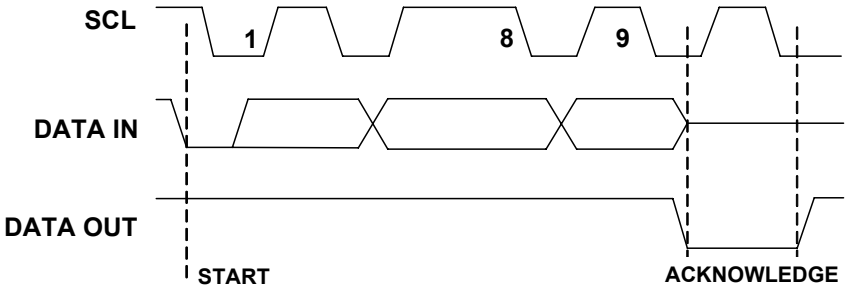


Figure 12. Output Acknowledge

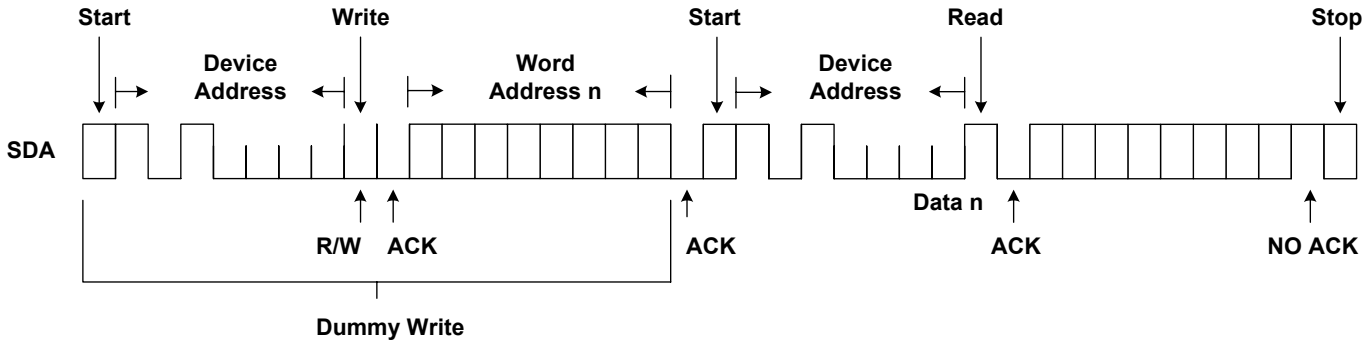


Figure 13. Random Read

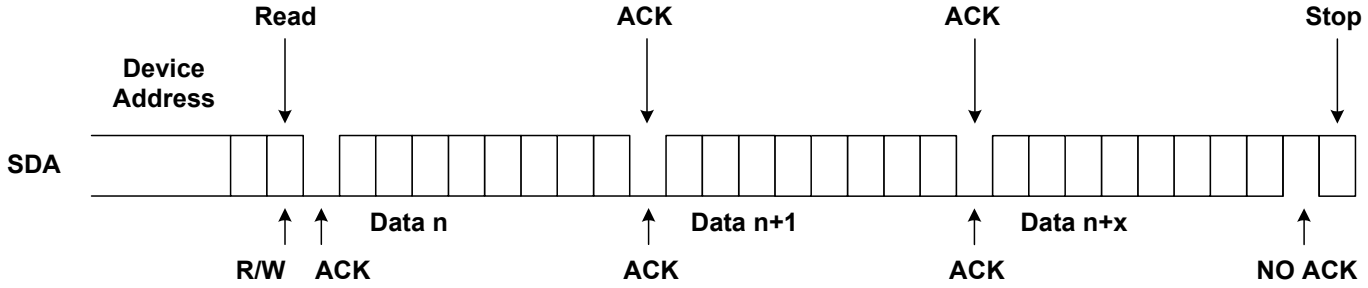


Figure 14. Sequential Read

8.3.4. SMI

The SMI (Serial Management Interface) is also known as the MII Management Interface, and consists of two signals (MDIO and MDC). It allows external devices with SMI master mode (MDC is output) to control the state of the PHY and internal registers (SMI slave mode: MDC is input). MDC is an input clock for the RTL8305SC to latch MDIO on its rising edge. The clock can run from DC to 25MHz. MDIO is a bi-directional connection used to write data to, or read data from the RTL8305SC. The PHY address is from 0 to 4.

Table 145. SMI Read/Write Cycles

	Preamble (32 bits)	Start (2 bits)	OP Code (2 bits)	PHYAD (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}…….D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}…….D_0	Z*

Note: Z: high-impedance. During idle time MDIO state is determined by an external 1.5KΩ pull-up resistor.*

The RTL8305SC supports Preamble Suppression, which allows the MAC to issue Read/Write Cycles without preamble bits. However, for the first cycle of MII management after power-on reset, a 32-bit preamble is needed.

To guarantee the first successful SMI transaction after power-on reset, the external device should delay at least 1second before issuing the first SMI Read/Write Cycle relative to the rising edge of reset.

8.3.5. Head-Of-Line Blocking

The RTL8305SC incorporates an advanced mechanism to prevent Head-Of-Line blocking problems when flow control is disabled. When the flow control function is disabled, the RTL8305SC first checks the destination address of the incoming packet. If the destination port is congested, the RTL8305SC will discard this packet to avoid blocking the next packet, which is going to a non-congested port.

8.3.6. Port-Based VLAN

If the VLAN function is enabled by pulling down the strapping pin DisVLAN, the default VLAN membership configuration by internal register is port 4 overlapped with all the other ports to form four individual VLANs. This default configuration of the input port could be modified via an attached serial EEPROM or SMI interface. The 16 VLAN membership registers designed into the RTL8305SC provide full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members. The RTL8305SC supports five VLAN indexes for each port to individually index this port to one of the 16 VLAN membership registers. These 16 VLAN membership registers, *VLAN ID [A] membership bit [4:0] ~ VLAN ID [P] membership bit [4:0]*, describe which ports are the members of this VLAN. The RTL8305SC forwards packets to the members of this VLAN only (excluding the input port of this frame). A port that is not included in a VLAN's member set cannot transmit packets to this VLAN.

Figure 15 illustrates a typical application. VLAN indexes and VLAN member definitions are set to form three different VLAN groups.

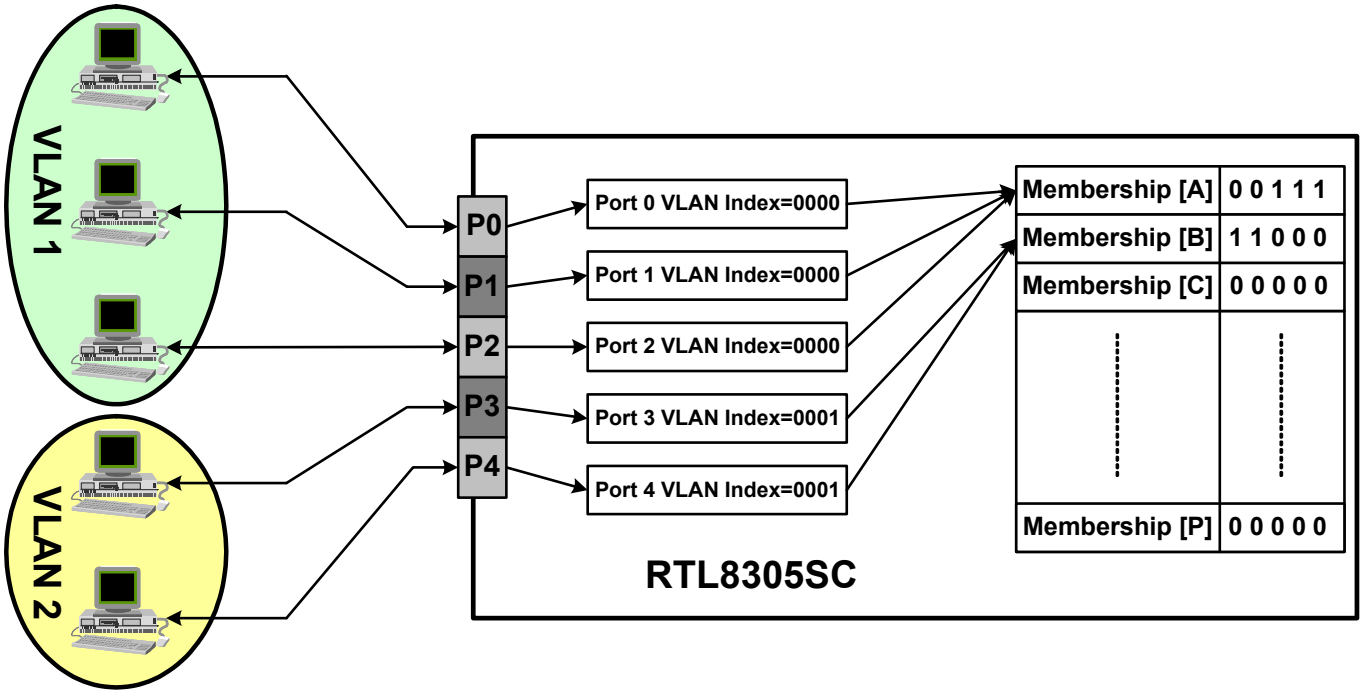


Figure 15. VLAN Grouping Example

For port-based VLAN configuration, each ingress port is allotted an index register to index to this port's 'Port VLAN Membership' register, which can be defined in one of the registers from 'VLAN ID [A] Membership bit [4:0]' to 'VLAN ID [P] Membership bit [4:0]' register.

Using the default value as an example:

- Port 0 VLAN Index[3:0]=2'b0000 means the member set of port 0 is defined in the 'VLAN ID [A] Membership' register
- Port 1 VLAN Index[3:0]=2'b0001 means the member set of port 0 is defined in the 'VLAN ID [B] Membership' register
- Port 2 VLAN Index[3:0]=2'b0010 means the member set of port 0 is defined in the 'VLAN ID [C] Membership' register
- Port 3 VLAN Index[3:0]=2'b0011 means the member set of port 0 is defined in the 'VLAN ID [A] Membership' register
- Port 4 VLAN Index[3:0]=2'b0100 means the member set of port 0 is defined in the 'VLAN ID [A] Membership' register

For non-VLAN tagged frames, the RTL8305SC performs port-based VLAN. It will use *'Port n VLAN Index [3:0]'* register to index to a VLAN membership. The VLAN ID associated with this indexed VLAN membership is the Port VID (PVID) of this port.

8.3.7. IEEE 802.1Q Tagged-VID Based VLAN

The RTL8305SC supports 16 VLAN entries to perform 802.1Q tagged-VID based VLAN mapping. In 802.1Q VLAN mapping, the RTL8305SC uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The 16 groups of VLAN membership registers, 'VLAN ID [A] membership [4:0] ~ VLAN ID [P] membership [4:0]', consist of the ports that are in the same VLAN corresponding to the registers defined in register 'VLAN ID [A] [11:0] ~ VLAN ID [P] [11:0]'. If the VID of a VLAN-tagged frame does not hit any one of the registers in 'VLAN ID [A] [11:0] ~ VLAN ID [P] [11:0]', the RTL8305SC will perform port-based VLAN mapping to the member set indexed by register 'Port n VLAN index [3:0]'. Otherwise, the RTL8305SC compares the explicit identifier in the VLAN tag with the 16 VLAN ID registers to determine the VLAN association of this packet, and then forwards this packet to the member set of this VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' at PHY0 Reg.16.10 is enabled, the RTL8305SC performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8305SC performs only port-based VLAN mapping both on non-tagged and tagged frames. Figure 16 illustrates the processing flow when '802.1Q tag aware VLAN' is disabled.

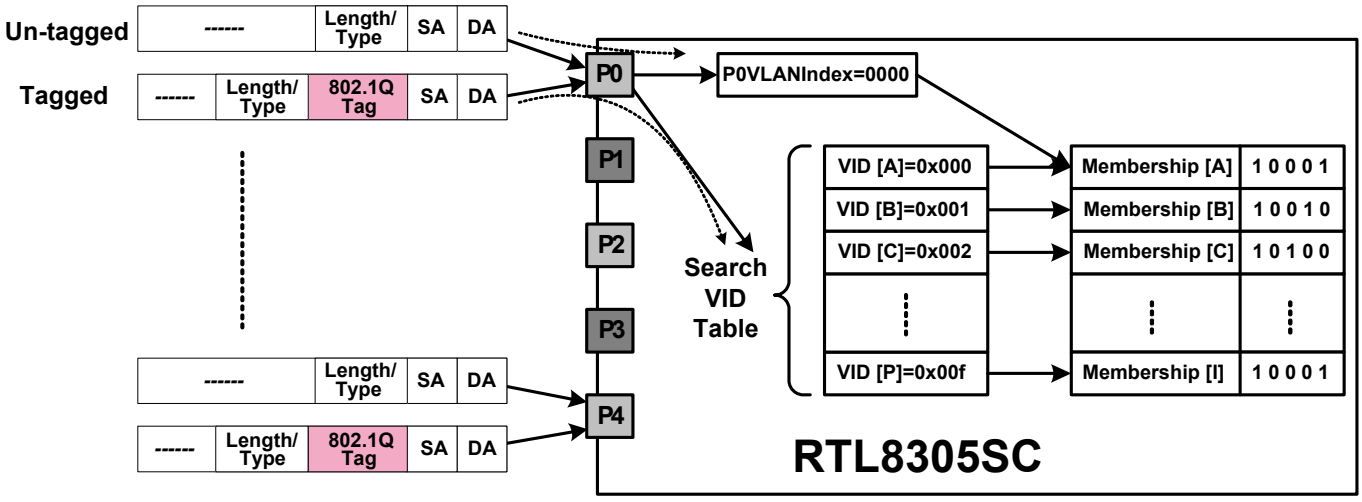


Figure 16. Tagged and Untagged Packet Forwarding when 802.1Q Tag Aware VLAN is Disabled

Two VLAN ingress filtering functions are supported by the RTL8305SC in registers. One is the 'VLAN tag admit control' defined in PHY0 Reg.16.8, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering' defined in PHY0 Reg.16.9, which will drop frames if the receive port is not in the member set.

There are also two optional egress filtering functions supported by the RTL8305SC through strapping. One is 'Leaky VLAN' at PHY0 Reg18.11, which e . That is, if the layer 2 lookup table search has a hit, then the unicast packet will be forwarded to the egress port, ignoring the egress rule. The other is 'ARP VLAN' at PHY0 Reg.18.10, which will broadcast ARP packets to all other ports, ignoring the egress rule.

8.3.8. Port VID (PVID)

In a router application, the router may want to know which input port this packet came from. The RTL8305SC supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on an egress packet. The VID information carried in the VLAN tag will be changed to a PVID. The RTL8305SC also provides an option to admit VLAN tagged packets with a specific PVID only. When this function is enabled, packets with an incorrect PVID, and non-tagged packets will be dropped.

The RTL8305SC uses an internal register, *Port n VLAN index [3:0,]* to index to one of the 16 VLAN entries. The VLAN ID associated with this indexed VLAN entry is the PVID for this port. Users may select VLAN insert/remove type 10 or 00 to insert a PVID on egress packets.

In 802.1Q tag-based VLAN applications, do not use a port-based VLAN PVID applications as the VID information carried in the VLAN tag will be replaced with a PVID.

8.3.9. Lookup Table Access

The RTL8305SC supports registers for the CPU to read or write an internal 1024-entry lookup table via the SMI interface. Before reading/writing from/to the internal forwarding table, the contents of internal register, Indirect Access Control [15:0] at PHY4 Register 16, should be filled correctly.

In the write cycle, the user must assign the write data in register Indirect Access Data 0, 1, 2, and 3 at PHY4 Register 17~20 first. Register 17, bits [1:0] along with bits [15:8] form a 10-bit field (Entry Index [9:0]), which is indirectly mapped to an entry in the lookup table. To execute write access, bit 0 in the Indirect Access Control register should be set to 0, and bit 1 should be set to 1. The CPU will poll bit 1 in Indirect Access Control to determine whether the write access is complete on not.

In the read cycle, the user only has to enter the read address of the lookup table in register Indirect Access Data 0, 1, 2, and 3 at PHY4 Register 17~20 first. Register 17, bits [1:0] along with bits [15:8] form a 10-bit field (Entry Index [9:0]). To execute read access, bit 0 in the Indirect Access Control register should be set to 1, and bit 1 should be set to 1 to trigger this command. The CPU will poll bit 1 in Indirect Access Control to determine whether read access is complete or not.

8.3.10. QoS Function

The RTL8305SC can recognize the QoS priority information of incoming packets to give a different egress service priority. The RTL8305SC identifies the packets as high priority based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q VLAN priority tag
- TCP/IP's TOS/DiffServ (DS) priority field

There are two priority queues; a high-priority queue, and a low-priority queue. The queue service rate is based on the Weighted Round Robin algorithm, the packet-based service weight ratio of the high-priority queue and low-priority queue can be set to 4:1, 8:1, 16:1 or 'Always high priority first' by hardware pins upon reset, or internal register via SMI after reset.

Port-Based Priority

When port-based priority is applied, packets received from the high-priority port are sent to the high-priority queue of the destination port. High priority ports can be partially set by hardware pins, and wholly configured by registers.

802.1p-Based Priority

When 802.1p VLAN tag priority is enabled, the RTL8305SC recognizes the 802.1Q VLAN tag frames and extracts the 3-bit User Priority information from the VLAN tag. The RTL8305SC default sets the threshold of User Priority as 4. Therefore, VLAN tagged frames with User Priority value = 4~7 will be treated as high priority frames, and User Priority values=0~3 will be treated as low priority frames (follows the IEEE 802.1p standard). The threshold value can be modified in internal registers via an SMI interface or configured in EEPROM.

DiffServ-Based Priority

When TCP/IP's TOS/DiffServ(DS) based priority is enabled, the RTL8305SC recognizes TCP/IP Differentiated Services Codepoint (DSCP) priority information from the DS-field defined in RFC 2474. The DS field byte in IPv4 is a Type-of-Service (TOS) octet. The recommended DiffServ Codepoint is defined in RFC 2597 to classify the traffic into different service classes. The RTL8305SC extracts the codepoint value of DS-fields from IPv4 packets, and identifies the priority of the incoming IP packet according to the following definition:

High priority: Where the DS-field = (EF, Expected Forwarding:) 101110 or
(AF, Assured Forwarding:) 001010; 010010; 011010; 100010 or
(Network Control:) 110000 and 111000.

Low priority: Where the DS-field = Other values.

The VLAN-tagged frame and 6-bit DS-field in the IPv4 frame format are shown below:

Table 146. 802.1Q VLAN Tag Frame Format

6 bytes	6 bytes	2 bytes	3 bits	
DA	SA	81-00	User-Priority (0~3: Low-pri; 4~7: High-pri)	----

Table 147. IPv4 Frame Format

6 bytes	6 bytes	4 bytes	2 bytes	4 bits	4 bits	6 bits	
DA	SA	802.1Q Tag (optional)	08-00	Version IPv4= 0100	IHL	TOS[0:5]= DS- field	----

8.3.11. Insert/Remove VLAN Tag

The RTL8305SC supports four types of insert/remove VLAN packet tags, controlled by internal registers on a per-port basis. They are classified as follows:

Type 11: Do not change packets (Default).

Type 10: Insert input port's VLAN tags for non-tagged packets. Do not change packets if they are already tagged.

Type 01: Remove VLAN tags from tagged packets. Do not change packets if they are not tagged.

Type 00: Remove VLAN tags from tagged packets, then insert the input port's VLAN tags. For non-tagged packets, insert the input port's VLAN tags.

If a tagged frame is less than 64 bytes after removal of the tag, it will be padded with an 0x20 pattern before the packet's CRC field to fit the 64-byte minimum packet length of the IEEE 802.3 spec. The RTL8305SC will recalculate the FCS (Frame Check Sequence) if the frame has been changed.

8.3.12. Filtering/Forwarding Reserved Control Frame

The RTL8305SC supports the ability to forward or drop the frames of the IEEE 802.1D specified reserved multicast addresses.

Table 148. Reserved Multicast Address

Address	Function	Control Bit	Control Bit=0	Control Bit=1
01-80-C2-00-00-00	Bridge Group Address	N/A	Broadcast	
01-80-C2-00-00-01	Pause Control Frame	N/A	Drop	
01-80-C2-00-00-03	IEEE802.1X Control Frame	N/A	Broadcast	
01-80-C2-00-00-02 and 01-80-C2-00-00-04 to 01-80-C2-00-00-0F	Reserved	EnForward	Drop	*Broadcast
Any other multicast Address	-	N/A	Broadcast	

*Note: * Indicates the default setting.*

8.3.13. Broadcast Storm Control

According to the latched value of the DISBRDCTRL pin upon reset, the RTL8305SC determines whether or not to proceed with broadcast storm control. Once enabled (DISBRDCTRL=0), after 64 consecutive broadcast packets (DID=FF-FF-FF-FF-FF-FF) are received by a particular port, this port will discard following incoming broadcast packets for approximately 800ms. Any non-broadcast packet can reset the time window and broadcast counter such that the scheme restarts.

Note: Trigger condition: consecutive 64 DID = FF-FF-FF-FF-FF-FF packets. Release condition: receive non-broadcast packet on or after 800ms.

8.3.14. Broadcast In/Out Drop

If some destination ports are blocking and the buffer is full, broadcast frames are dropped according to configuration.

1. Input Drop: Do not forward to any port and drop the frame directly
2. Output Drop: Forward only to non-blocking ports (Broadcast becomes multicast)

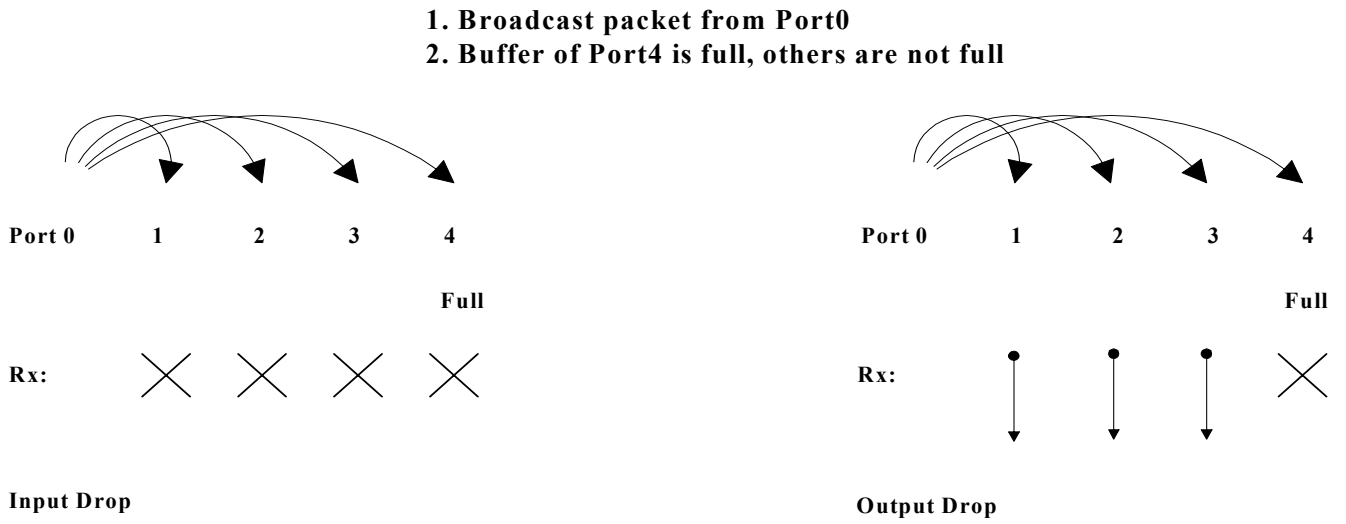


Figure 17. Input Drop vs. Output Drop

8.3.15. Loop Detection

Loops should be avoided between switch applications. The simplest loop as shown below results in: 1) Unicast frame duplication; 2) Broadcast frame multiplication; 3) Address table non-convergence. Frames may be transmitted from Switch1 to Switch 2 via Link 1, then returned to Switch 1 via Link 2.

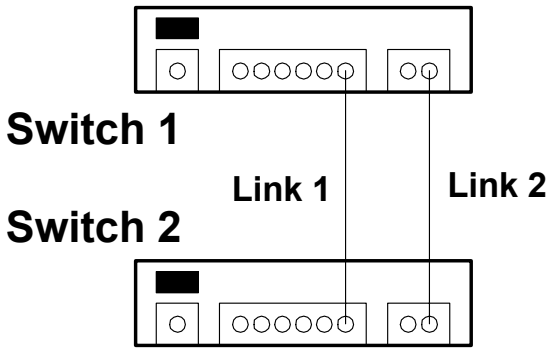


Figure 18. Loop Example

When the loop detection function is enabled, the RTL8305SC periodically sends out a broadcast 64-byte packet every 3~5 minutes and automatically detects whether there is a network loop (or bridge loop). If a loop is detected, the LoopLED# will be ON (active low or high). The LED goes out when both RTL8305SC ports of the loop are unplugged. The Loop frame length is 64 bytes and its format is shown below.

Table 149. Loop Frame Format

FFFF FFFF FFFF	SID	8899	0300 000…0000	CRC

In order to achieve loop detection, each switch device needs a unique SID (the source MAC address). If the EEPROM is not used, a unique SID should be assigned via SMI after reset, and the default SID (52-54-4c-83-05-c0) should not be used.

8.3.16. MAC Local Loopback Return to External

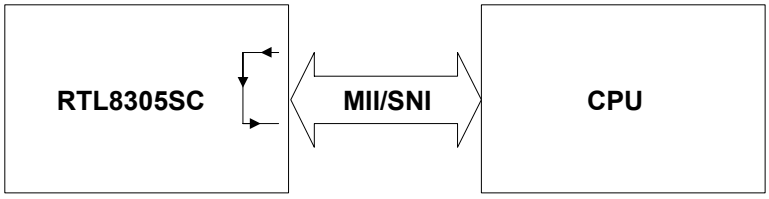
Each port supports loopback of the MAC (return to external device) for diagnostic purposes.

Example 1: If the internal register, PHY4 Reg.22.13=0 (Local loopback), the RTL8305SC will forward local and broadcast packets from the input of Port 4 to the output of Port 4, and drop unicast packets from the input of Port 4. Other ports can still forward broadcast or unicast packets to Port 4.

Example 2: If the internal register, PHY3 Reg.22.13=0 (Local loopback), the RTL8305SC will "forward local and broadcast packets from the input of Port3 to the output of Port3" and "drop unicast packets from the input of Port3". Other ports can still forward broadcast or unicast packets to port3.

This is especially useful for router applications performing mass production tests. This function is independent of PHY type (GxMode/GyMode/P4Mode[1:0]) and can be done on each mode. Below are two examples: In Example 1 the external device (CPU) is connected to the MII or SNI interface of Port 4. In Example 2, the external device (CPU) does not have an MII or SNI interface, so it uses the PCI interface to connect an RTL8139 to the UTP port of Port 4.

Example 1: LoopBack in External PHY Mode



Example 2: LoopBack in UTP Mode

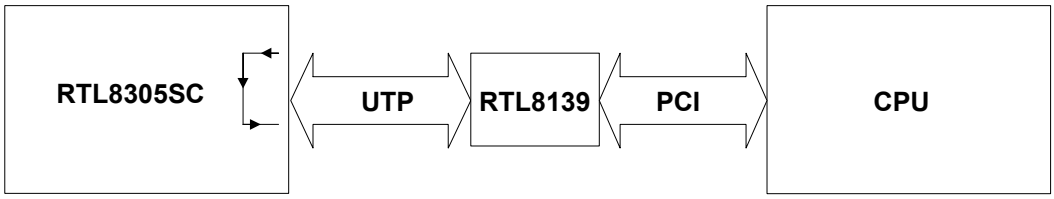


Figure 19. Port 4 Loopback

8.3.17. Reg.0.14 PHY Digital Loopback Return to Internal

The digital loopback mode of the PHY (return to internal MAC) may be enabled on a per-port basis by setting MII Reg.0.14 to 1. In digital loopback mode, the TXD of PHY is transferred directly to the RXD of PHY with TXEN changed to CRS_DV, and returns to MAC via an internal MII. The data stream coming from the MAC will not egress to the physical medium, and an incoming data stream from the network medium will be blocked in this mode. The packets will be looped back in 10Mbps full duplex or 100Mbps full duplex mode. This function is especially useful for diagnostic purposes. For example, a NIC can be used to send broadcast frames into port0 of the RTL8305SC and set Port1 to Reg0.14 Loopback. The frame will be looped back to port 0, so the received packet count can be checked to verify that the switch device is good. In this example, port0 can be 10M or 100M and full or half duplex.

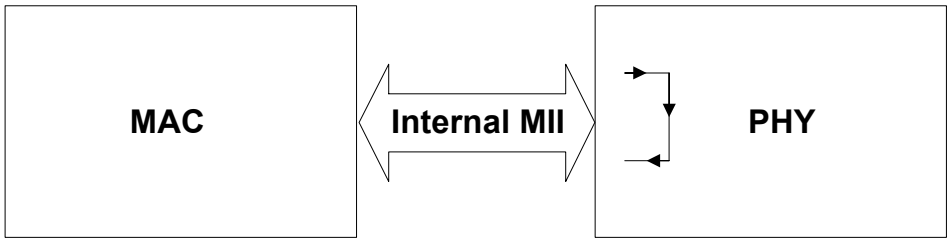


Figure 20. Reg. 0.14 Loopback

As the RTL8305SC only supports digital loopback in full duplex mode, PHY Reg.0.8 for each port will always be kept on 1 when digital loopback is enabled. The digital loopback only functions on broadcast packets (DA=FF-FF-FF-FF-FF-FF). In loopback mode, the link LED of the loopback port should always be ON, and the Speed and Duplex LED combined to reflect the link status (100full/10full) correctly, regardless of what the previous status of this loopback port was.

Consider a case where a port is initially unlinked. When we set this port to digital loopback mode, the RTL8305SC can get this port linked up within 100ms at the configured speed, and will block the sending of UTP or Fiber signals from this port.

8.3.18. LEDs

The RTL8305SC supports four parallel LEDs for each port, and two special LEDs (SELMIIMAC# and LOOPLED#). Each port has four LED indicator pins. Each pin may have different indicator meanings set by pins LEDMode[1:0]. Refer to the pin descriptions for details (Port LED Pins, on page 20). Upon reset, the RTL8305SC supports chip diagnostics and LED functions by blinking all LEDs once for 320ms. This function can be disabled by asserting EN_RST_LINK to 0. LED_BLINK_TIME determines the LED blinking period for activity and collision (1=43ms and 0=120ms). The parallel LEDs corresponding to

port 4 can be tri-stated (disable LED functions) for MII port application by setting ENP4LED in EEPROM to 0. In UTP applications, this bit should be set to 1.

All LED pins are dual function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is floating upon reset, the pin output is active low after reset. Otherwise, if the pin input is pulled down upon reset, the pin output is active high after reset. Exception: Bi-color Link/Act mode of pin LED_ADD[4:0] when LEDMode[1:0]=10.

Below is an example circuit for LEDs. The typical values for pull-down resistors are 10KΩ.

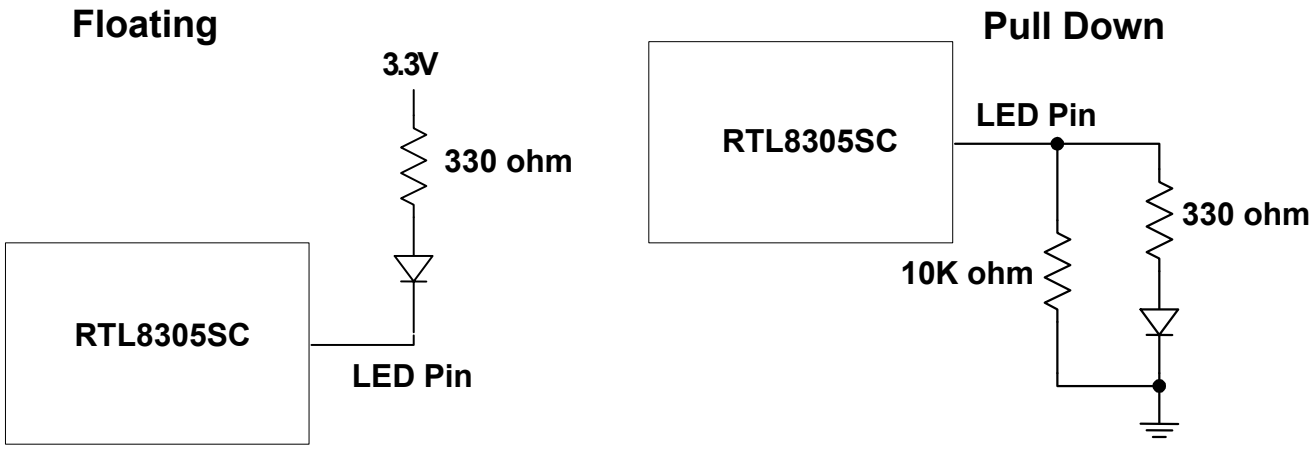


Figure 21. Floating and Pull-Down of LED Pins

For two-pin Bi-color LED mode (LEDMode[1:0]=10), Bi-color Link/Act (pin LED_ADD) and Spd (pin LED_SPD) can be used for one Bi-color LED package, which is a single LED package with two LEDs connected in parallel with opposite polarity. When LEDMode[1:0]=10, the active status of LED_ADD is the opposite of LED_SPD.

Table 150. Spd and Bi-Color Link/Act Truth Table

Indication	**Bi-Color State**	**Spd: Input=Floating, Active Low. Bi-color Link/Act:** The active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.		**Spd: Input=Pull-down, Active High. Bi-color Link/Act:** The active status of LED_ADD is the opposite of LED_SPD and does not interact with input upon reset.	
		Spd	**Link/Act**	**Spd**	**Link/Act**
No Link	Both Off	1	1	0	0
100M Link	Green On	0	1	1	0
10M Link	Yellow On	1	0	0	1
100M Act	Green Flash	0	Flash	1	Flash
10M Act	Yellow Flash	1	Flash	0	Flash

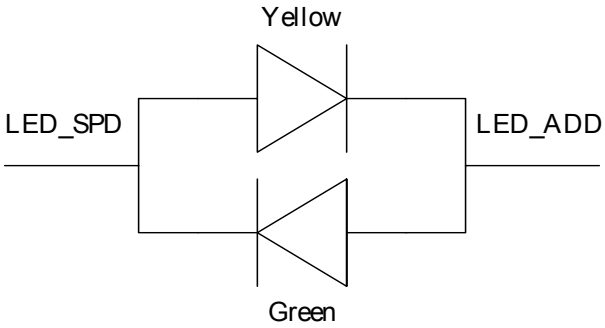


Figure 22. Two Pin Bi-color LED for SPD Floating or Pull-high

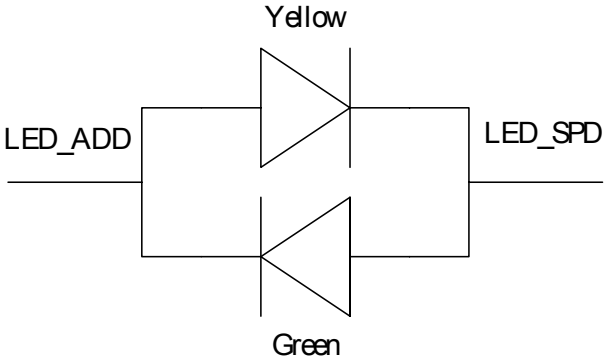


Figure 23. Two Pin Bi-color LED for SPD Pull-down

8.3.19. 1.8V Power Generation

The RTL8305SC can use a PNP transistor to generate 1.8V from a 3.3V power supply. This 1.8V is used for the digital core and analog receiver circuits. Do not use one PNP transistor for more than one RTL8305SC chip, even if the rating is enough. Use one transistor for each RTL8305SC chip.

Do not connect an inductor (bead) directly between the collector of the PNP transistor and AVDD18. This will adversely affect the stability of the 1.8V power to a significant degree.

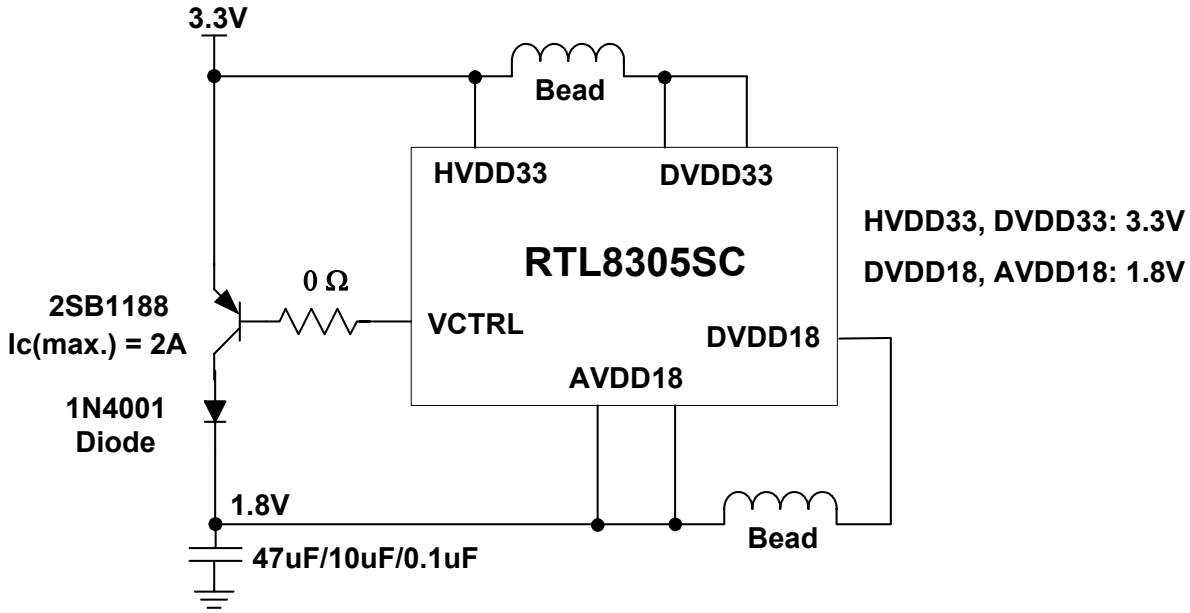


Figure 24. Using a PNP Transistor to Transform 3.3V Into 1.8V

Table 151. An Example Using Power Transistor 2SB1188

Parameter	Symbol	Limits	Unit
Collector-base voltage	VCBO	-40	V
Collector-emitter voltage	VCEO	-32	V
Emitter-base voltage	VEBO	-5	V
Collector current	IC	-2	A(DC)
Collector power dissipation	PC	0.5	W
Junction temperature	Tj	150	°C
Storage temperature	Tstg	-55~+150	°C

Note: Absolute maximum ratings (Ta=25°C).
For more information, refer to http://www.rohm.com

8.3.20. Crystal/Oscillator

The frequency is 25Mhz. The maximum Frequency Tolerance is +/-50ppm. The maximum Jitter is 150ps Peak-to-Peak.

9. Characteristics

9.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 152. Electrical Characteristics/Ratings

Parameter	Min	Max	Units
Vcc Supply Referenced to GND	-0.5	+4.0	V
Digital Input Voltage	-0.5	VDD	V
DC Output Voltage	-0.5	VDD	V

9.2. Operating Range

Parameter	Min	Max	Units
Storage Temperature	-55	+150	°C
Ambient Operating Temperature (Ta)	0	+70	°C
3.3V Vcc Supply Voltage Range (HVDD33, DVDD33)	3.15	3.45	V
1.8V Vcc Supply Voltage Range (DVDD18, AVDD18)	1.71	1.95	V

9.3. DC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Power Supply Current for 1.8V	Icc	10Base-T, idle 10Base-T, Peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Power saving Power down	40 500 460 470 40 40	45 525 470 480 45 45	50 550 480 490 50 50	mA
Power Supply Current for 3.3V	Icc	10Base-T, idle 10Base-T, Peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Power saving Power down	110 100 110 100 60 60	120 110 120 110 65 65	130 120 130 120 70 70	mA
Total Power Consumption for all Ports	PS	10Base-T, idle 10Base-T, Peak continuous 100% utilization 100Base-TX, idle 100Base-TX, Peak continuous 100% utilization Power saving Power down	295 1230 1191 1176 270 270	477 1308 1242 1227 295.5 295.5	519 1386 1293 1278 321 321	mW
TTL Input High Voltage	V_{ih}		2.0			V
TTL Input Low Voltage	V_{il}				0.8	V
TTL Input Current	I_{in}		-10		10	uA
TTL Input Capacitance	C_{in}			3		pF
Output High Voltage	V_{oh}		2.25			V
Output Low Voltage	V_{ol}				0.4	V
Output Three State Leakage Current	$\|I_{OZ}\|$				10	uA

9.4. AC Characteristics

Parameter	SYM	Condition	Min	Typical	Max	Units
Transmitter, 100Base-TX						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc, Best-fit over 14 bit times		1.007		V
Differential Output Voltage Symmetry	V_{OS}	50Ω from each output to Vcc, |Vp+|/ |Vp-|		99.1		%
Differential Output Overshoot	V_{OO}	Percent of Vp+ or Vp-		3.1		%
Rise/Fall Time	t_r ,t_f	10-90% of Vp+ or Vp-		4.1		ns
Rise/Fall Time Imbalance	$\|t_r - t_f\|$			0.17		ns
Duty Cycle Distortion		Deviation from best-fit time-grid, 010101 … Sequence		0.2		ns
Timing Jitter		Idle pattern		0.87		ns
TD Differential Output Impedance (return loss)		Return loss margin from 2Hz to 80MHz for reference resistance of 100Ω. The margin is the minimum difference between the limit line and the return loss curve	4.6			dB
RD Differential Output Impedance (return loss)		Return loss margin from 2Hz to 80MHz for reference resistance of 100Ω. The margin is the minimum difference between the limit line and the return loss curve	4.6			dB
Transmitter, 10Base-T						
Differential Output Voltage, Peak-to-Peak	V_{OD}	50Ω from each output to Vcc, all pattern		2.36		V
TP_IDL Silence Duration		Period of time from start of TP_IDL to link pulses or period of time between link pulses		10.48		ms
TD Short Circuit Fault Tolerance		Peak output current on TD short circuit for 10 seconds.		24		mA
TD Common-Mode Output Voltage	Ecm	Terminate each end with 50Ω resistive load		43.2		mV
Transmitter Output Jitter				6		ns
Harmonic Content		dB below fundamental, 20 cycles of all ones data		28		dB
Start-of-idle Pulse Width		TP_IDL width		256		ns

9.5. Digital Timing Characteristics

Table 153. LED Timing

Parameter	SYM	Condition	Min	Typical	Max	Units
LED Timing						
LED On Time	tLEDon	While LED blinking	43		120	ms
LED Off Time	tLEDoff	While LED blinking	43		120	ms

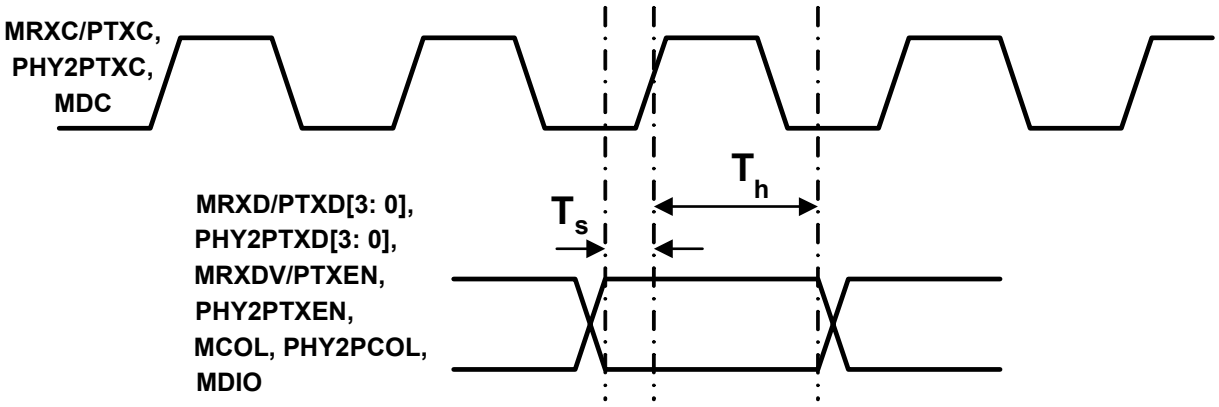


Figure 25. Reception Data Timing of MII/SNI/SMI Interface

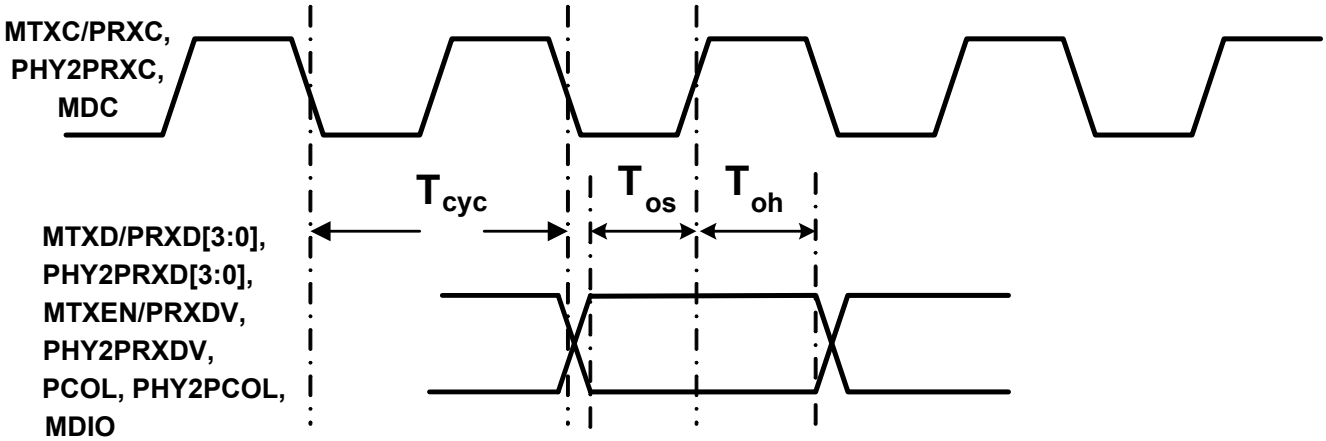


Figure 26. Transmission Data Timing of MII/SNI/SMI Interface

Table 154. MII & SMI DC Timing

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
MAC Mode MII Timing							
100BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		40±50 ppm		ns
10BaseT MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC clock cycle time	I		400±50 ppm		ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Setup Time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	34	34.8	36	ns
MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV Output Hold Time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], MTXEN/PRXDV	O	4	5.2	6	ns
MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN, MCOL/PCOL Setup Time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD, MRXDV/PTXEN, MCOL/PCOL Hold Time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns
PHY Mode MII Timing							
100BaseT MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		40±50 ppm		ns
10BaseT MTXC/PRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC	T_{cyc}	MTXC/MRXC, MRXC/PTXC, PHY2PTXC, PHY2PRXC clock cycle time	O		400±50 ppm		ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Setup Time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	17.2	18.2	19.2	ns
MTXD/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL Output Hold Time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[3:0]/PRXD[3:0], PHY2PRXD[3:0], MTXEN/PRXDV, PHY2PRXDV MCOL/PCOL, PHY2PCOL	O	20.8	21.8	22.8	ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Setup Time	T_s	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MRXD/PTXD[3:0], PHY2PTXD[3:0], MRXDV/PTXEN, PHY2PTXEN Hold Time	T_h	MRXD[3:0]/PTXD[3:0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns

Parameter	SYM	Condition	I/O	Min	Type	Max	Units
PHY Mode SNI Timing							
MTXC/MRXC, MRXC/PTXC	T_{cyc}	MTXC/PRXC, MRXC/PTXC clock cycle time	O		100±50 ppm		ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Setup Time	T_{os}	Output Setup time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	36	38	40	ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Output Hold Time	T_{oh}	Output Hold time from MTXC/PRXC rising edge to MTXD[0]/PRXD[0], MTXEN/PRXDV, MCOL/PCOL	O	59	60	61	ns
MRXD/PTXD[0], MRXDV/PTXEN Setup Time	T_s	MRXD[0]/PTXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge setup time	I	4			ns
MTXD/PRXD[0], MTXEN/PRXDV, MCOL/PCOL Hold Time	T_h	MTXD[0]/PRXD[0], MRXDV/PTXEN to MRXC/PTXC rising edge hold time	I	2			ns
SMI Timing							
MDC	T_{cyc}	MDC clock cycle	I	40			ns
MDIO Setup Time	T_s	Write cycle	I	10			ns
MDIO Hold Time	T_h	Write cycle	I			10	ns
MDIO Output Delay Relative to Rising Edge of MDC	T_{ov}	Read cycle	O			10	µs

9.6. Thermal Characteristics

9.6.1. Package Description

Table 155. Package Description

Item	Parameter
Type	QFP128
Device	RTL8305SC
Dimension (L x W)	14 x 20 mm
Thickness	2.85 mm

9.6.2. PCB Description

Table 156. PCB Description

Item	Parameter
Dimension (L x W)	50 x 70 mm
Number of Cu Layer	2 layers (80% of Cu trace coverage of top/bottom layer)

9.6.3. Assembly Material

Table 157. Assembly Material

Item	Material	Thermal Conductivity K (w/m-k)
Die	Silicon	147
Lead Frame	C7025	168
Silver Paste	AG03*7	2.0
Mold Compound	6300HG	0.63
PCB	FR4	0.21
	Cu	393

9.6.4. Simulation Analysis Conditions

Table 158. Simulation Analysis Conditions

Item	Parameter
Air Flow Rate	0, 1, 2, 3 m/s
Control Condition	Power=1.386 W
Ambient Temperature	60°C

9.6.5. Results

Table 159. Results

Air Flow (m/s)	0	1	2	3
Tj (°C)	117.3	112.1	109.6	108.2
Tc (°C)	111.0	104.7	101.8	100.2
θJA (°C/W)	41.3	37.6	35.8	34.8
ψJT (°C/W)	4.51	5.33	5.61	5.79

Where:

Tj is the maximum junction temperature.

Tc is the maximum case temperature.

θJA is the junction-to-ambient thermal resistance.

θJC is the junction-to-case thermal resistance.

10. Application Information

10.1. UTP (10Base-T/100Base-TX) Application

In reviewing this material, please be advised that the center-tap on the primary side of the transformer must be left floating and should not be connected to ground through capacitors.

Table 160. Transformer Vendors

Vendor	Quad	Single
Pulse	H1164	H1102
Magnetic 1	ML164	ML102

Two types of transformers are generally used for the RTL8305SC. One is a Quad (4 port) transformer with one common pin on both sides for an internal connected central tap. Another is a Single (1 port) transformer with two pins on both sides for a separate central tap.

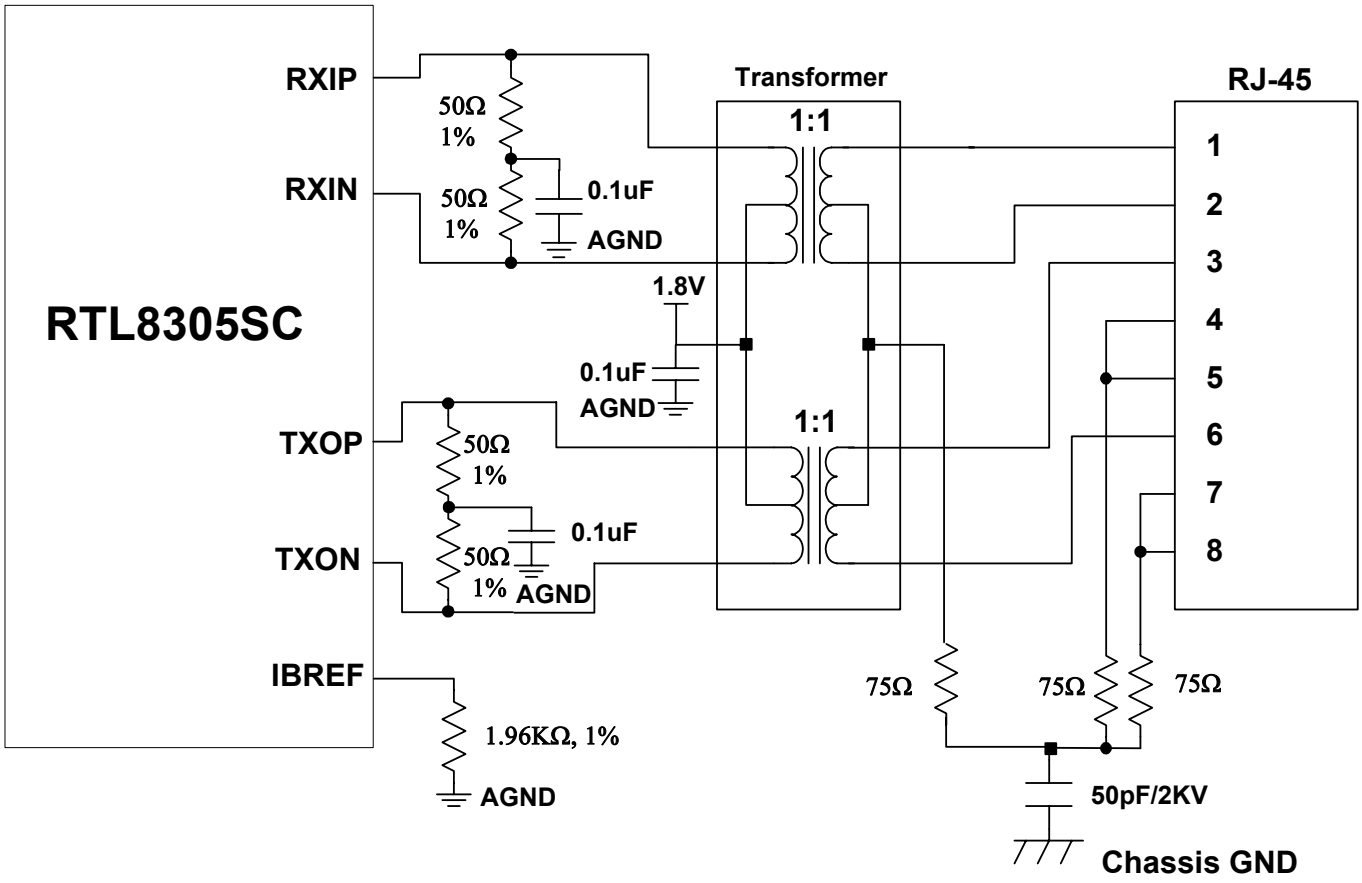


Figure 27. UTP Application for Transformer with Connected Central Tap

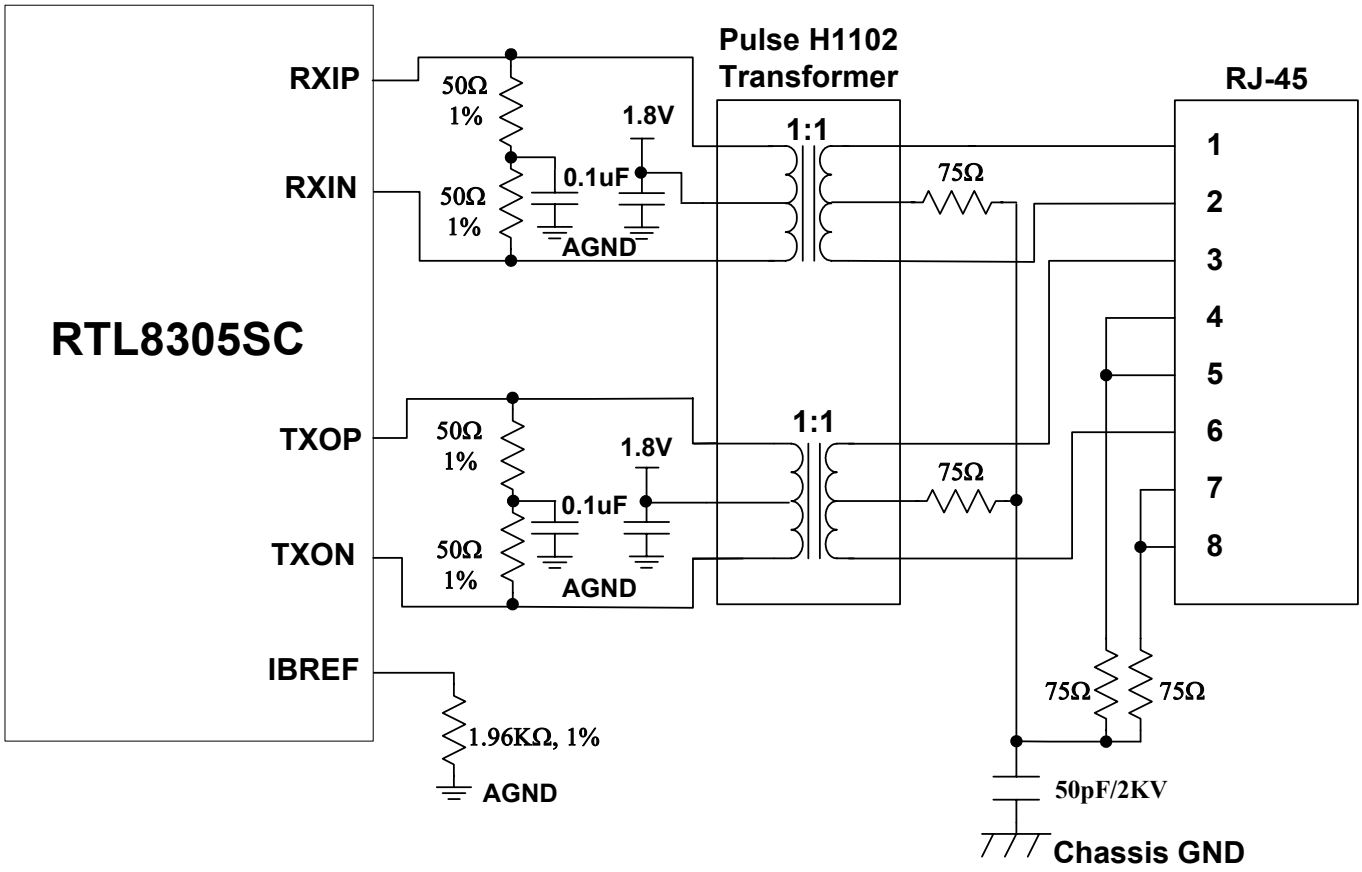


Figure 28. UTP Application for Transformer with Separate Central Tap

10.2. 100Base-FX Application

The following is an example of an RTL8305SC connecting to a 3.3V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300 nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

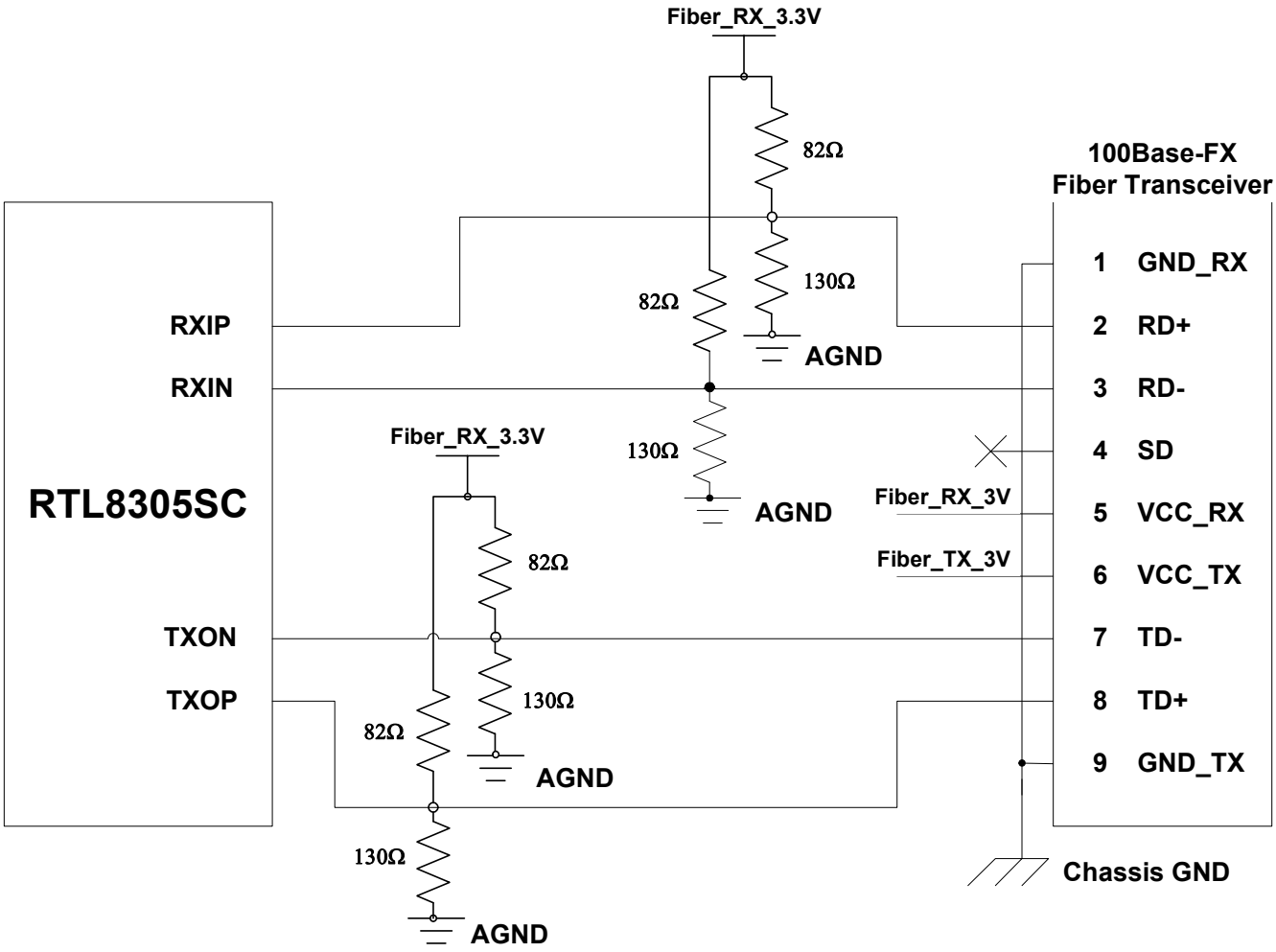


Figure 29. 100Base-FX with 3.3V Fiber Transceiver Application

Figure 30 shows an example of an RTL8305SC connected to a 5V fiber transceiver application circuit with a SIEMENS V23809-C8-C10 (3.3V~5V fiber transceiver, 1*9 SC Duplex Multimode 1300nm LED Fast Ethernet/FDDI/ATM Optical Transceiver Module).

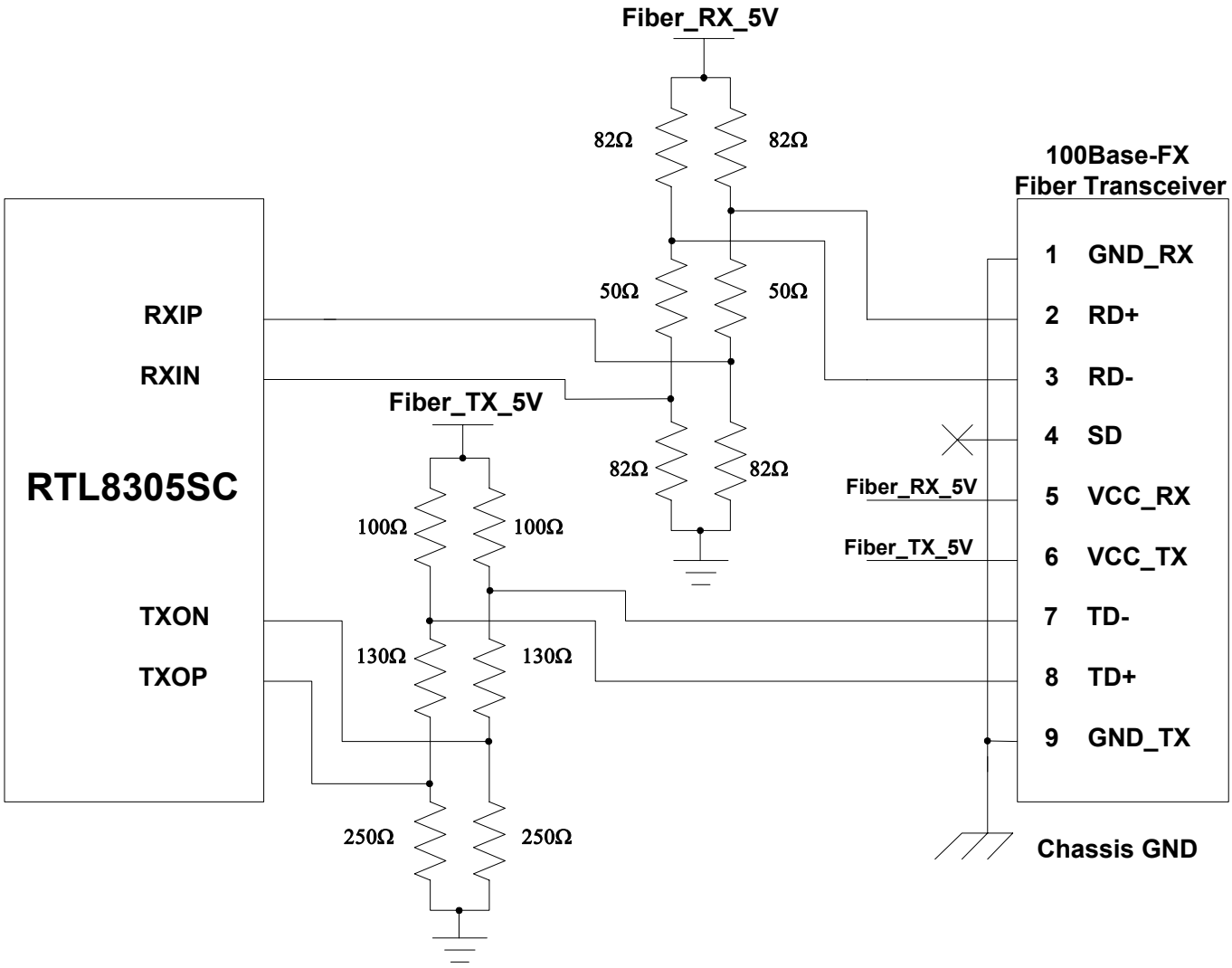


Figure 30. 100Base-FX with 5V Fiber Transceiver Application

11. Design and Layout Guide

In order to achieve maximum performance using the RTL8305SC, good design attention is required throughout the design and layout process. The following are some suggestions to implement a high performance system.

General Guidelines

- Provide a good power source, minimizing noise from switching power supply circuits (<50mV).
- Verify the ability of critical components, e.g. clock source and transformer, to meet application requirements.
- Keep power and ground noise levels below 50mV.
- Use bulk capacitors (4.7µF-10µF) between the power and ground planes.
- Use 0.1µF de-coupling capacitors to reduce high-frequency noise on the power and ground planes.
- Keep de-coupling capacitors as close as possible to the RTL8305SC chip.

Differential Signal Layout Guidelines

- Keep differential pairs as close as possible and route both traces as identically as possible.
- Avoid vias and layer changes if possible.
- Keep transmit and receive pairs away from each other. Run orthogonal or separate by a ground plane.

Clock Circuit

- If possible, surround the clock by ground trace to minimize high-frequency emissions.
- Keep the crystal or oscillator as close to the RTL8305SC as possible.

1.8V Power

- Do not connect a bead directly between the collector of the PNP transistor and AVDD18. This will significantly affect the stability of the 1.8V power supply.
- Use a bulk capacitor (4.7µF-10µF) between the collector of the PNP transistor and the ground plane.
- Do not use one PNP transistor for more than one RTL8305SC chip, even if the rating is enough. Use one transistor for each RTL8305SC chip.

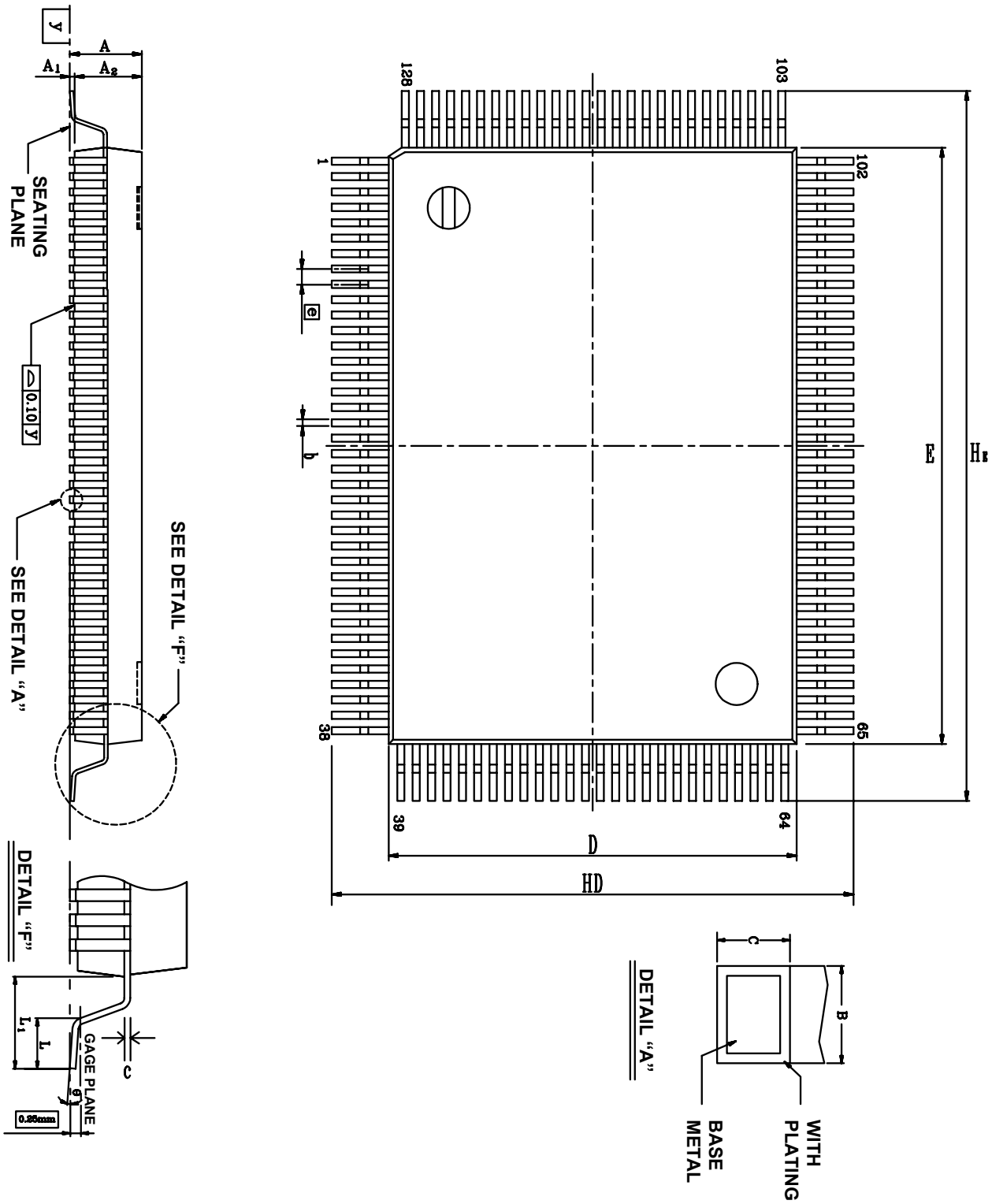
Power Plane

- Divide the power plane into 1.8V digital, 3.3V digital, and 1.8V analog.
- Use 0.1µF decoupling capacitors and bulk capacitors between each power plane and the ground plane.
- Power line connects from the source to the RTL8305SC pin should be at least 10 mil wide.

Ground Plane

- Keep the system ground region as one continuous, unbroken plane that extends from the primary side of the transformer to the rest of the board.
- Place a moat (gap) between the system ground and chassis ground.
- Ensure the chassis ground area is voided at some point such that no ground loop exists on the chassis ground area.

12. Mechanical Dimensions



See the Mechanical Dimensions notes on the next page.

12.1. Mechanical Dimensions Notes

Symbol	Dimensions in inches			Dimensions in mm		
	Min	Typical	Max	Min	Typical	Max
A	-	-	0.134	-	-	3.40
A1	0.004	0.010	0.036	0.10	0.25	0.91
A2	0.102	0.112	0.122	2.60	2.85	3.10
b	0.005	0.009	0.013	0.12	0.22	0.32
c	0.002	0.006	0.010	0.05	0.15	0.25
D	0.541	0.551	0.561	13.75	14.00	14.25
E	0.778	0.787	0.797	19.75	20.00	20.25
e	0.010	0.020	0.030	0.25	0.5	0.75
HD	0.665	0.677	0.689	16.90	17.20	17.50
HE	0.902	0.913	0.925	22.90	23.20	23.50
L	0.027	0.035	0.043	0.68	0.88	1.08
L1	0.053	0.063	0.073	1.35	1.60	1.85
y	-	-	0.004	-	-	0.10
θ	0°	-	12°	0°	-	12°

Notes:
1. Dimensions D & E do not include interlead flash.
2. Dimension b does not include dambar rotrusion/intrusion.
3. Controlling dimension: Millimeter
4. General appearance spec. Should be based on final visual inspection.

TITLE: PQFP-128 -CU L/F, FOOTPRINT 3.2 mm			
LEADFRAME MATERIAL:			
APPROVE		DOC. NO.	
		VERSION	1.2
		PAGE	
CHECK		DWG NO.	Q128 - 1
		DATE	12 February 2003
REALTEK SEMICONDUCTOR CORP.			

13. Ordering Information

Table 161. Ordering Information

Part Number	Package	Status
RTL8305SC	128-pin PQFP	
RTL8305SC-LF	128-pin PQFP Lead (Pb)-Free package	

Realtek Semiconductor Corp.
Headquarters
No. 2, Industry East Road IX, Science-based
Industrial Park, Hsinchu, 300, Taiwan, R.O.C.
Tel: 886-3-5780211 Fax: 886-3-5776047
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