NIPPON PRECISION CIRCUITS INC

SM5160CM/DM

Programable PLL Frequency Synthesizer

OVERVIEW

The SM5160CM/DM is a PLL frequency synthesizer IC with programmable input and reference frequency dividers.

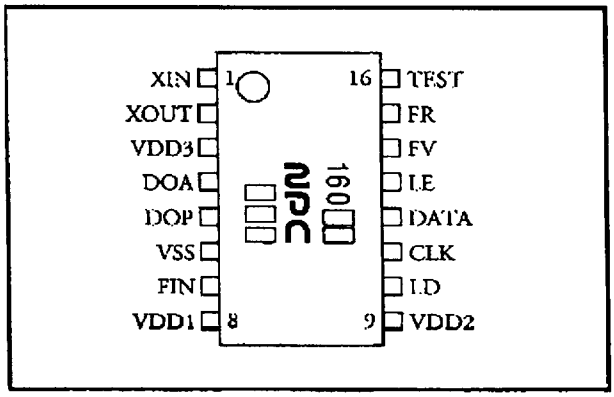
The SM5160CM/DM features an unlock detector, outputs for use with active passive lowpass filters and direct frequency divider outputs.

The SM5160CM/DM operates from 0.95 to 2.00 V and 2.0 to 3.3 V supplies and is available in 16-pin SSOPs.

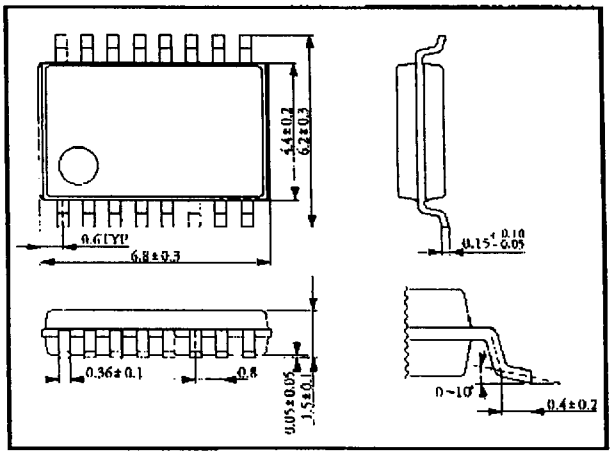
FEATURES

- Up to 95 MHz input frequency (FIN, V_{DD}= 0.98V)
- Up to 90 MHz input frequency (FIN, V_{DD}= 0.95V)
- Up to 13.0 MHz reference frequency (XIN)
- 1056 to 65535 programmable input frequency divider ratio
- 20 to 65532 programmable reference frequency divider ratio (SM5160CM)
- 20 to 8188 programmable reference frequency divider ratio (SM5160DM)
- Unlock detector
- Outputs for use with active and passive lowpass filters
- Direct outputs from frequency dividers
- 0.95 to 2.0 V and 2.0 to 3.3 V supplies
- Molybdenum- gate CMOS process
- 16-pin SSOP

PINOUT (Top View)



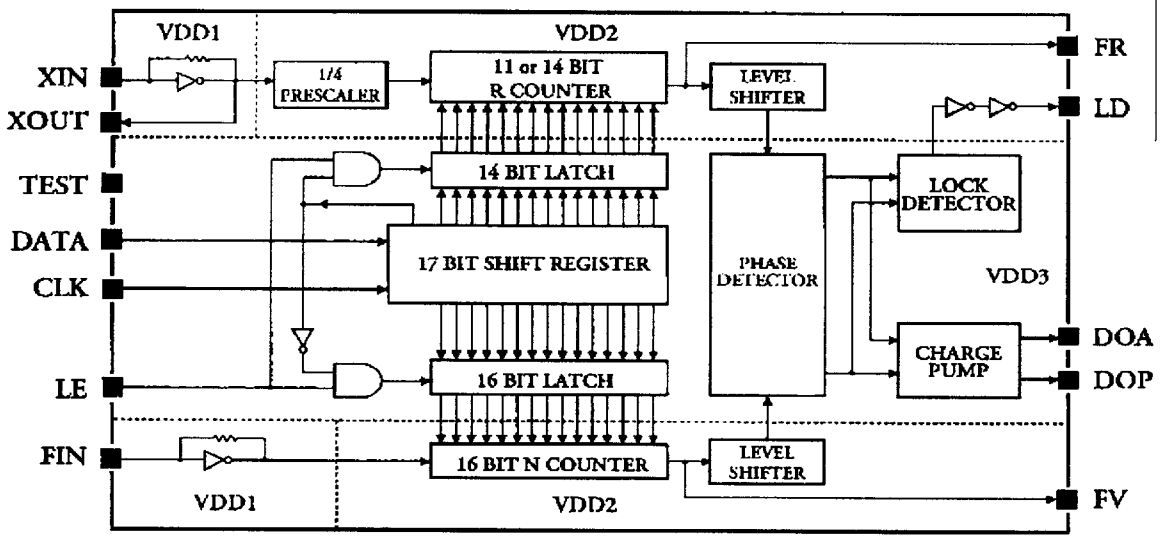
PACKAGE DIMENSIONS (Unit: mm)



SERIES LINEUP

		XIN	FIN
SM5160CM	Divider range	20 to 65532 (4 step)	1056 to 65535
	Counter bits	14 bit	16 bit
SM5160DM	Divider range	20 to 8188 (4 step)	1056 to 65535
	Counter bits	11 bit	16 bit

BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Description
1	XIN	Reference oscillator or external clock input. Internal feedback resistor for AC coupling
2	XOUT	Reference oscillator or external clock output. Oscillator is OFF when VDD1 is LOW.
3	VDD3	Supply voltage for sections not supplied by VDD1 and VDD2
4	DOA	Output to active lowpass filter. Single-ended, tristate output. Floating when VDD1 is LOW
5	DOP	Output to passive lowpass filter. Single-ended, tristate output Floating when VDD1 is LOW
6	VSS	Ground
7	FIN	Comparison frequency input. Internal feedback resistor for AC coupling
8	VDD1	Supply voltage for XIN and FIN amplifiers
9	VDD2	Supply voltage for N counter and R counter
10	LD	Unlock detector output. LOW when PLL is unlocked.
11	CLK	Shift register clock input
12	DATA	Serial data input
13	LE	Latch enable input
14	FV	Input frequency divider buffered output. This is level-shifted and input to the phase detector.
15	FR	Reference frequency divider buffered output. This is level-shifted and input to the phase detector.
16	TEST	Test input. Internal pull-down resistor

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage range 1	V_{DD1}–V_{SS} V_{DD2}–V_{SS}		−0.3 to +7.0	V
Supply voltage range 2	V_{DD3}-V_{SS}		−0.3 to +7.0	V
Input voltage range	V_{IN}		V_{SS}−0.3 to V_{DD3}+0.3	V
Operating temperature range	T_{OPR}		−10 to +60	℃
Storage temperature range	T_{STG}		−40 to +125	℃
Soldering temperature range	T_{SLD}		250	℃
Soldering time range	t_{SLD}		10	sec

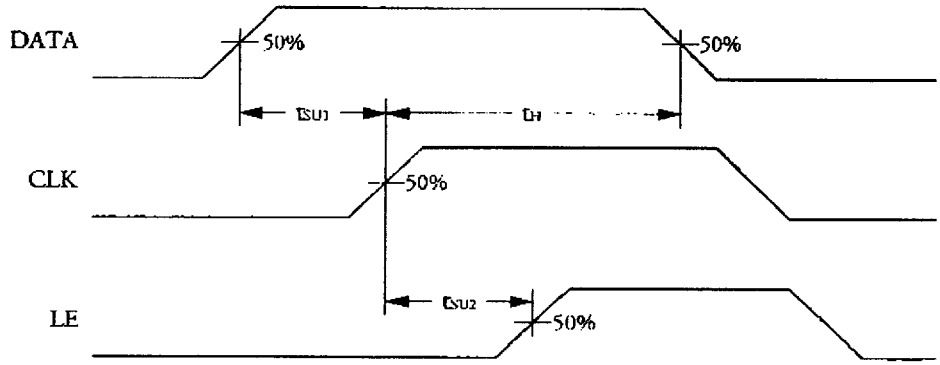
Electrical Characteristics

(V_{DD1}= V_{DD2}= 0.95 to 2.0V, V_{DD3}= 2.0 to 3.3V, V_{SS}= 0V, Ta= −10～+60℃ unless otherwise noted)

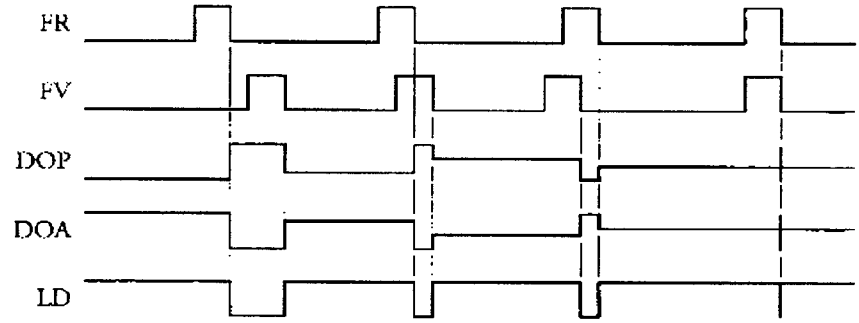
Parameter	Symbol	Condition	Rating min	Rating typ	Rating max	Unit
Supply voltage 1	V_{DD1},V_{DD2}	VDD1 and VDD2 pins	0.95	1.00	2.0	V
Supply voltage 2	V_{DD3}	VDD3 pin	2.0	3.0	3.3	V
Current consumption (*1)	I_{DD1}	F_{IN}= 90MHz, 0.5V_{P-P} sine wave X_{IN}= 12.8MHz, 0.5V_{P-P} sine wave V_{DD1}= V_{DD2}= 0.95 to 1.05V		0.80	1.20	mA
		F_{IN}= 95MHz, 0.5V_{P-P} sine wave X_{IN}= 12.8MHz, 0.5V_{P-P} sine wave V_{DD1}= V_{DD2}= 0.98 to 1.08V		0.85	1.40	mA
Standby-mode current consumption	I_{DD2}	V_{DD1}= V_{DD2}= 0V			10	μA
FIN maximum operating frequency	f_{MAX1}	F_{IN}: 0.5V_{P-P} sine wave V_{DD1}= V_{DD2}= 0.95 to 2.0V	90			MHz
		F_{IN}: 0.5V_{P-P} sine wave V_{DD1}= V_{DD2}= 0.98 to 2.0V	95			MHz
XIN maximum operating frequency	f_{MAX2}	X_{IN}: 0.5V_{P-P} sine wave	13			MHz
FIN minimum operating frequency	f_{MIN1}	F_{IN}: 0.5V_{P-P} sine wave			40	MHz
XIN minimum operating frequency	f_{MIN2}	X_{IN}: 0.5V_{P-P} sine wave			7	MHz
FIN and XIN input voltage	V_{IN}	FIN and XIN pins	0.5		V_{DD1}	V_{P-P}
CLK, DATA and LE input voltage	V_{IH}		V_{DD3}− 0.3			V
	V_{IL}				0.3	V
XIN input current	I_{IH1}	V_{IH}= V_{DD1}			10	μA
	I_{IL1}	V_{IL}= 0V			10	μA
FIN input current	I_{IH2}	V_{IH}= V_{DD1}			60	μA
	I_{IL2}	V_{IL}= 0V			60	μA
DOA and DOP output current	I_{OH1}	V_{DD3}= 2.7 to 3.3V, V_{OH}= V_{DD3}− 0.4V	1.0			mA
	I_{OL1}	V_{DD3}= 2.7 to 3.3V, V_{OL}= 0.4V	1.0			mA
LD, FV and FR output current	I_{OH1}	V_{OH}= V_{DD2}− 0.4V	0.1			mA
	I_{OL1}	V_{OH}= 0.4V	0.1			mA
DATA to CLK and CLK to LE setup time	t_{SU1}		2			μs
	t_{SU2}		2			μs
hold time	t_H		2			μs

*1 Current consumption is the current consumed from V_{DD1} and V_{DD2}.

Serial data input timing



Phase detector timing



FUNCTIONAL DESCRIPTION

Lowpass Filter Connection

An external lowpass filter connects to DOP or DOA. The output form the filter is fed to a voltage-controlled oscillator (VCO) which generates the PLL output.

DOP is intended for use with a passive filter as shown in figure 1. DOA is intended for use with an active filter as shown in figure 2.

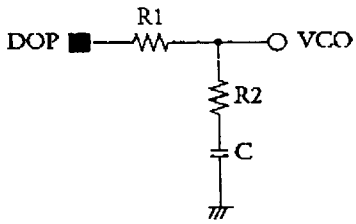


Figure 1. Passive lowpass filter circuit

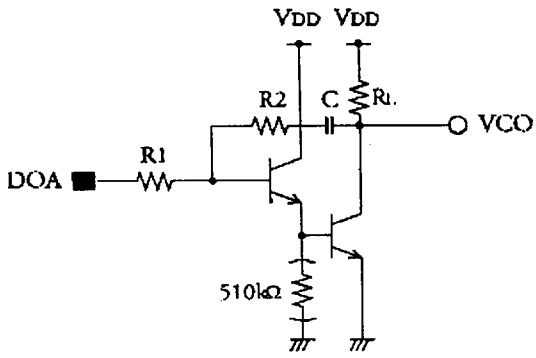


Figure 2. Active lowpass filter circuit

Programmable Frequency Divider

The input frequency divider and reference frequency divider ratios can be programmed using the serial data input.

Input data consists of 16 data bits, in the order msb to lsb, followed by a control bit, as shown in figure 3 and 4.

SM5160CM

If the control bit is set to 0, the data is written to the 16-bit latch and then passed to the input frequency divider.

If the control bit is set to 1, the 2 lsbs are ignored and the remaining data is written to the 14-bit latch and then passed to the reference frequency divider.

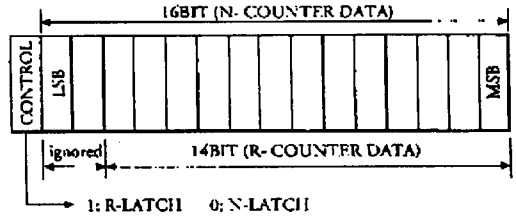


Figure 3. Serial data format (SM5160CM)

SM5160DM

If the control bit is set to 0, the data is written to the 16-bit latch and then passed to the input frequency divider.

If the control bit is set to 1, the 2 lsbs and 3msbs are ignored and the remaining data is written to the 11-bit latch and then passed to the reference frequency divider.

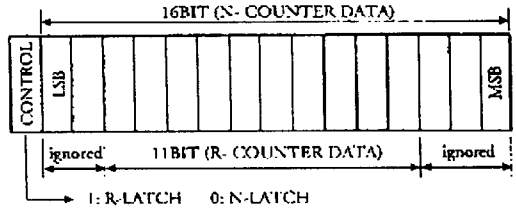


Figure 4. Serial data format (SM5160DM)

Serial data input timing

Serial data input timing is shown in figure 5. Data is read on the rising edge of CLK. The state on DATA should be changed in sync with the falling edge of CLK.

LE should be LOW while data is being written to the shift register. When LE goes HIGH, data is transferred from the shift register to one of the frequency divider latches.

Stand-by mode

The stand-by mode is entered by setting VDD1, VDD2 to 0V while the device is operation.

In the stand-by mode, the amplifiers of XIN, FIN and N/R counter are stopped. As long as voltage is provide to VDD3, data written in latch is kept. Exit from this mode to normal operation, therefore, is made by providing voltage to VDD1, VDD2. In this mode, input to FIN must be done AC coupling, input to XIN must be done AC coupling or by crystal oscillator. In this mode, DOA, DOP should be in state of floating.

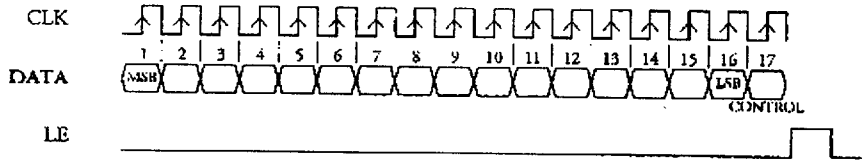
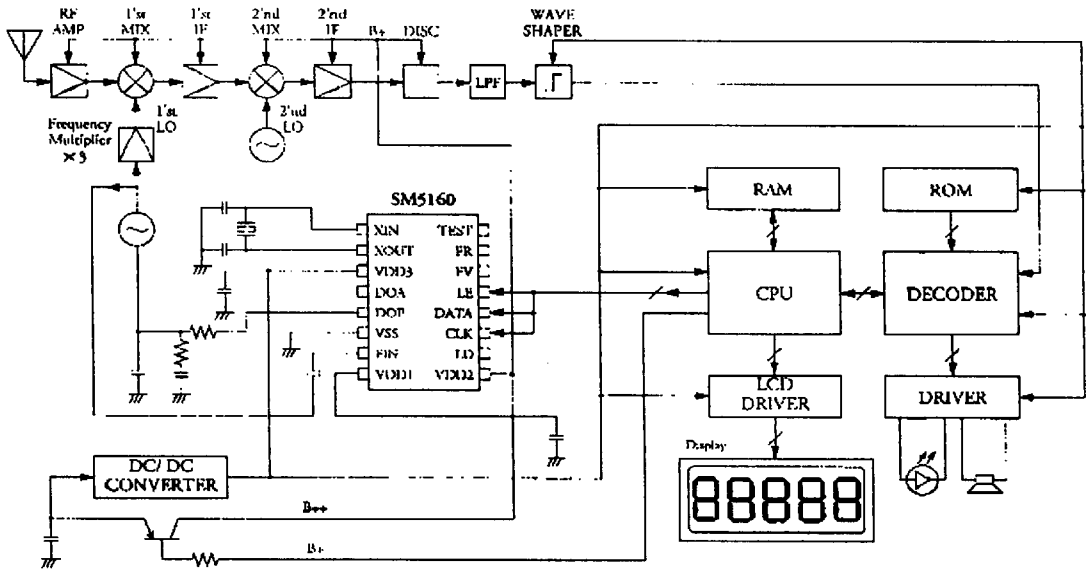


Figure 5. Serial data input

TYPICAL APPLICATION

(For Ex. : in case of Pager)



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