A product Line of Diodes Incorporated

PI6C4853111

2.5V/3.3V 500MHz Low Skew 1-to-10 Differential to LVPECL Fanout Buffer with 2 to 1 Differential Clock Input Mux

Features

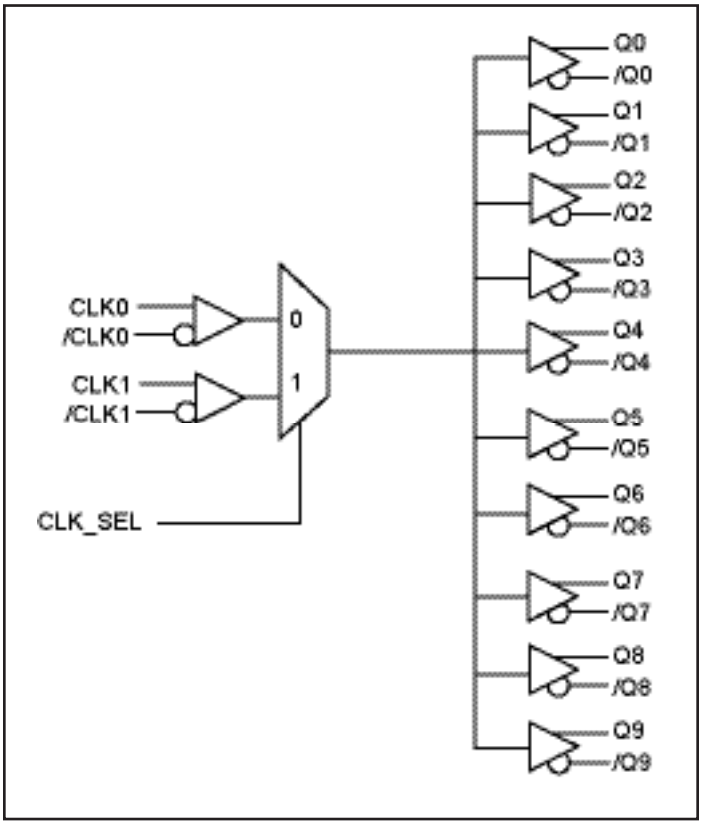
- F_{MAX} = 500MHz
- 10 pairs of differential LVPECL outputs
- Low additive jitter, <100fs 12k-20MHz
- Selectable differential input pairs with single ended input option
- Input CLK accepts: LVPECL, LVDS, CML, SSTL input level
- Output skew: 35ps (typ)
- Operating Temperature: -40°C to 85°C
- Core Power supply: 3.3V ±10%, Output Power supply: 2.5V ±5% & 3.3V ±10%
- Packaging (Pb-free & Green):
  - –32-pin TQFP (FA)

Description

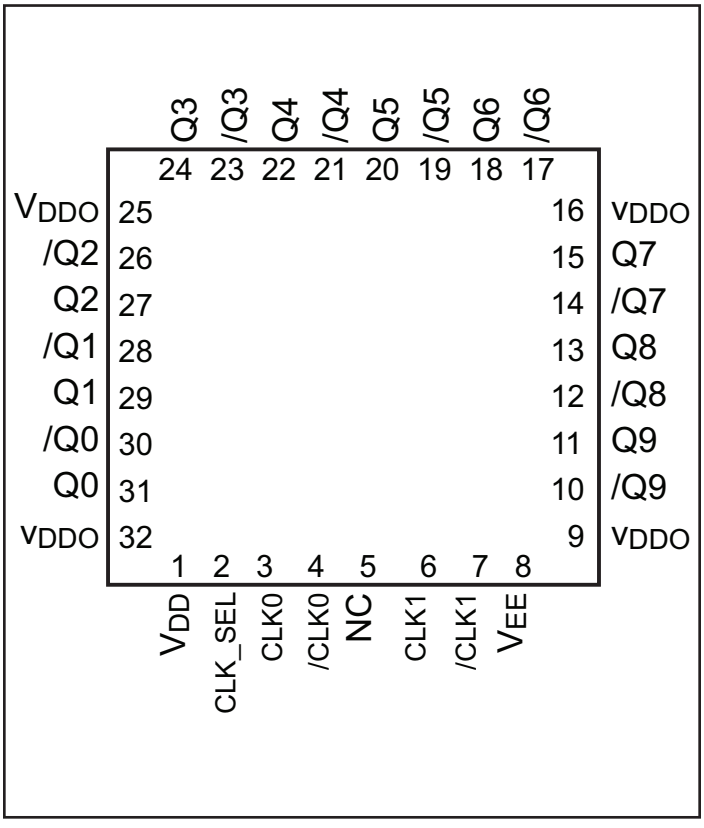
The PI6C4853111 is a high-performance low-skew 1-to-10 LVPECL fanout buffer. The PI6C4853111 features two selectable differential clock inputs and translates to ten LVPECL outputs. The CLK inputs accept LVPECL, LVDS, CML and SSTL signals.

PI6C4853111 is ideal for clock distribution applications such as providing fanout for low noise SaRonix-eCera oscillators.

Block Diagram



Pin Configuration



Pin Description(1)

Name	Pin #	Type	Description
V_{EE}	8	P	Connect to negative power supply
CLK_SEL	2	I	Clock select input. When high, selects CLK1 input. When low, selects CLK0 input. LVCMOS/LVTTL level with 50kΩ pull down.
CLK0	3	I	Differential LVPECL clock input with 75kΩ pull-down
/CLK0	4	I	Inverting differential LVPECL clock input. Defaults to $V_{DD}/2$ if left floating.
CLK1	6	I	Differential LVPECL clock input with 75kΩ pull-down
/CLK1	7	I	Inverting differential LVPECL clock input. Defaults to $V_{DD}/2$ if left floating.
NC	5		No Connect
V_{DDO}	9,16, 25,32	P	Output Power pin
V_{DD}	1	P	Core Power Supply
Q3, /Q3	24,23	O	Differential output pair, LVPECL interface level.
Q2, /Q2	27,26	O	Differential output pair, LVPECL interface level.
Q1, /Q1	29,28	O	Differential output pair, LVPECL interface level.
Q0, /Q0	31,30	O	Differential output pair, LVPECL interface level.
Q9, /Q9	11,10	O	Differential output pair, LVPECL interface level.
Q8, /Q8	13,12	O	Differential output pair, LVPECL interface level.
Q7, /Q7	15,14	O	Differential output pair, LVPECL interface level.
Q6, /Q6	18,17	O	Differential output pair, LVPECL interface level.
Q5, /Q5	20,19	O	Differential output pair, LVPECL interface level.
Q4, /Q4	22,21	O	Differential output pair, LVPECL interface level.

Note:
1. I = Input, O = Output, P = Power supply connection.

Pin Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
R	Input Pullup/Pulldown Resistance			50		kΩ

Control Input Function Table

Inputs	Outputs
0	CLK0
1	CLK1

Absolute Maximum Ratings(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Supply voltage	Referenced to GND			4.6	V
V_{IN}	Input voltage	Referenced to GND	-0.5		V_{DD}+0.5V	V
I_{OUT}	Surge Current				100	mA
T_{STG}	Storage temperature		-65		150	°C
V_{BB}	Smk/source Current, I_{BB}		-0.5		+0.5	mA
T_J	Junction Temperature				125	°C

Note:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These ratings are stress specifications only and correct functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{DD}	Power Supply Voltage		3.0		3.6	V
V_{DDO}	Output Power Supply Voltage		2.375		3.6	V
T_A	Ambient Temperature		-40		85	°C

LVCMOS/LVTTL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±5%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Input High Voltage	CLK_SEL		2		V_{DD}+0.3	V
V_{IL}	Input Low Voltage	CLK_SEL		-0.3		0.8	
I_{IH}	Input High Current	CLK_SEL	V_{IN} = V_{DD} = 3.6V			150	µA
I_{IL}	Input Low Current	CLK_SEL	V_{IN} = 0V, V_{DD} = 3.6V	-5			µA

LVPECL DC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter		Conditions	Min	Typ	Max	Units
I_{IH}	Input High Current	CLK0, CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
		/CLK0, /CLK1	$V_{IN} = V_{DD}$ = 3.6V			150	µA
I_{IL}	Input Low Current	CLK0, CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-5			µA
		/CLK0, /CLK1	V_{DD} = 3.6V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-peak Voltage			0.3		1	V
V_{CMR}	Common Mode Input Voltage(1)			V_{EE}+1.5		V_{DD}	V
V_{OH}	Output High Voltage(2)		V_{DDO} = 2.5V or 3.3V	V_{DDO}-1.4		V_{DDO}-0.9	V
V_{OL}	Output Low Voltage(2)		V_{DDO} = 2.5V or 3.3V	V_{DDO}-2.0		V_{DDO}-1.7	V
V_{SWING}	Peak-to-peak Output Voltage Swing			0.6		1.0	V
I_{EE}	Power Supply Current		@ 400 MHz		120	140	mA

Notes:
1. For single-ended applications, the maximum input voltage for CLK and /CLK is V_{DD}+0.3V
2. Outputs terminated with 50Ω to V_{DD}-2.0V

AC Characteristics (T_A = -40°C to +85°C, V_{DD} = 3.3V ±10%, V_{DDO} = 2.5V ±5% to 3.3V ±10%)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
f_{max}	Output Frequency				500	MHz
t_{pd}	Propagation Delay(1)				4	ns
Tsk	Output-to-output Skew(2)			35	60	ps
t_r/t_f	Output Rise/Fall time	20% - 80%	150		700	ps
odc	Output duty cycle	f ≤ 400 MHz	45		55	%
J_{add}	Additive jitter	V_{DD} = V_{DDO} = 2.5V or 3.3V		75		fs

Notes:
1. Measured from the differential input to the differential output crossing point
2 Defined as skew between outputs at the same supply voltage and with equal loads. Measured at the output differential crossing point

Additive Jitter Calculation

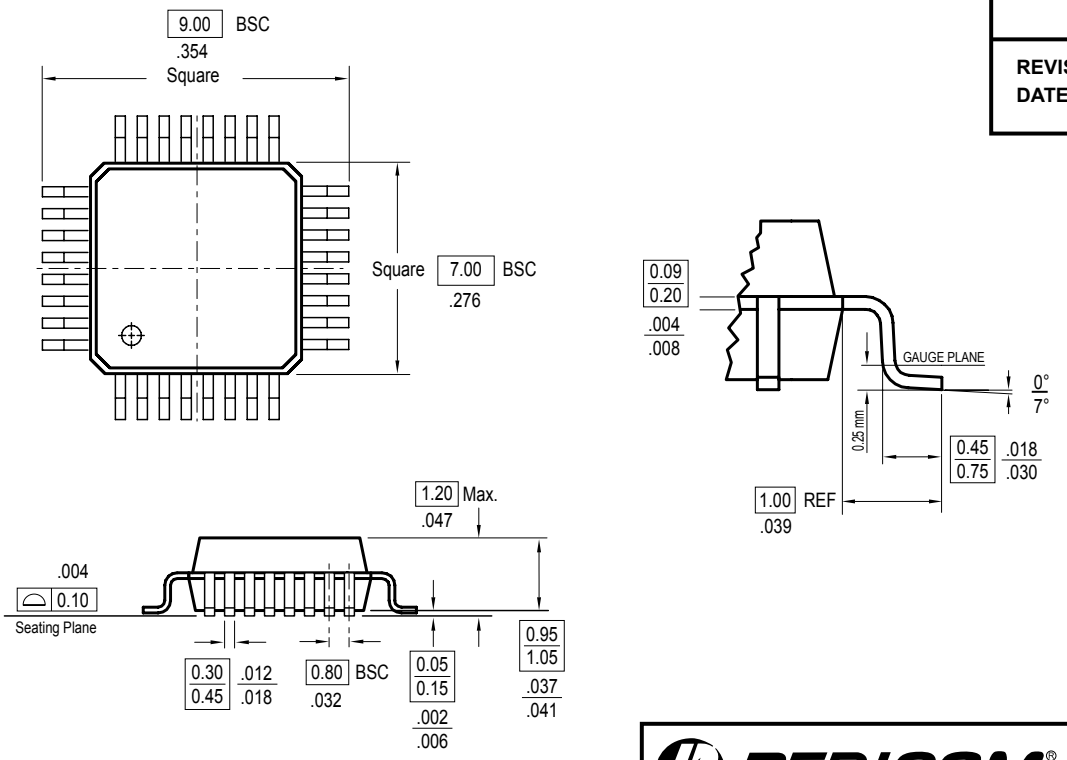
The additive jitter is measured at 12KHz to 20MHz standard noise band with the LVPECL differential input clock at 156.25MHz.

$$additive\ jitter = \sqrt{jitter\_out^2 - jitter\_in^2}$$

Summary of Phase Jitter (Diff. Input and Diff. Output)

	Input	Output	Additive Jitter	Unit
V_{DD} = 3.3V, 12kHz-20MHz	253.7	259.7	55.5	fs RMS
V_{DD} = 2.5V, 12kHz-20MHz	186.6	201.3	75.5	fs RMS

Packaging Mechanical: 32-pin TQFP (FA)



DOCUMENT CONTROL NO.
PD - 1814

REVISION: C
DATE: 03/09/05

X.XX
X.XX DENOTES DIMENSIONS IN MILLIMETERS

Notes:
1. Controlling dimensions in millimeters
2. Ref.: JEDEC MS-026D/ABA
3. Package Outline Exclusive of Mold Flash and Metal Burr

PERICOM®
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DESCRIPTION: 32-Pin, Thin Quad Flat Package, TQFP

PACKAGE CODE: FA

Ordering Information(1,2,3)

Ordering Code	Package Code	Package Description
PI6C4853111FAE	FA	Pb-free & Green, 32-pin TQFP
PI6C4853111FAEX	FA	Pb-free & Green, 32-pin TQFP, pin 1 orientation on top right in tape and reel
PI6C4853111FAE+CWX	FA	Pb-free & Green, 32-pin TQFP, pin 1 orientation on top left in tape and reel

Notes:
1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. E = Pb-free & Green
3. X suffix = Tape/Reel

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