20 V, 200 mA, Low Noise, CMOS LDO Linear Regulator

Data Sheet **ADP7118**

FEATURES

- Low noise: 11 µV rms independent of fixed output voltage
- PSRR of 88 dB at 10 kHz, 68 dB at 100 kHz, 50 dB at 1 MHz, $V_{OUT} \leq 5$ V, $V_{IN} = 7$ V
- Input voltage range: 2.7 V to 20 V
- Maximum output current: 200 mA
- Initial accuracy: ±0.8%
- Accuracy over line, load, and temperature
  - −1.2% to +1.5%, T_J = −40°C to +85°C
  - ±1.8%, T_J = −40°C to +125°C
- Low dropout voltage: 200 mV (typical) at a 200 mA load, $V_{OUT} = 5$ V
- User programmable soft start (LFCSP and SOIC only)
- Low quiescent current, I_{GND} = 50 µA (typical) with no load
- Low shutdown current: 1.8 µA at $V_{IN} = 5$ V, 3.0 µA at $V_{IN} = 20$ V
- Stable with a small 2.2 µF ceramic output capacitor
- Fixed output voltage options: 1.8 V, 2.5 V, 3.3 V, 4.5 V, and 5.0 V
- 16 standard voltages between 1.2 V and 5.0 V are available
- Adjustable output from 1.2 V to $V_{IN} - V_{DO}$, output can be adjusted above initial set point
- Precision enable
- 2 mm × 2 mm, 6-lead LFCSP, 8-Lead SOIC, 5-Lead TSOT

APPLICATIONS

- Regulation to noise sensitive applications
  - ADC and DAC circuits, precision amplifiers, power for VCO V_{TUNE} control
- Communications and infrastructure
- Medical and healthcare
- Industrial and instrumentation
- Supported by ADIsimPower tool

TYPICAL APPLICATION CIRCUITS

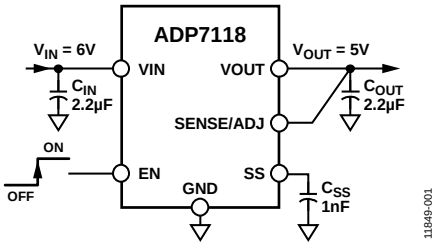

Figure 1. ADP7118 with Fixed Output Voltage, 5 V

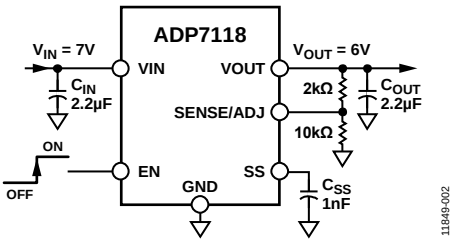

Figure 2. ADP7118 with 5 V Output Adjusted to 6 V

GENERAL DESCRIPTION

The ADP7118 is a CMOS, low dropout (LDO) linear regulator that operates from 2.7 V to 20 V and provides up to 200 mA of output current. This high input voltage LDO is ideal for the regulation of high performance analog and mixed-signal circuits operating from 20 V down to 1.2 V rails. Using an advanced proprietary architecture, the device provides high power supply rejection, low noise, and achieves excellent line and load transient response with a small 2.2 µF ceramic output capacitor. The ADP7118 regulator output noise is 11 µV rms independent of the output voltage for the fixed options of 5 V or less.

The ADP7118 is available in 16 fixed output voltage options. The following voltages are available from stock: 1.2 V (adjustable), 1.8 V, 2.5 V, 3.3 V, 4.5 V, and 5.0 V.

Additional voltages available by special order are 1.5 V, 1.85 V, 2.0 V, 2.2 V, 2.75 V, 2.8 V, 2.85 V, 3.8 V, 4.2 V, and 4.6 V.

Each fixed output voltage can be adjusted above the initial set point with an external feedback divider. This allows the ADP7118 to provide an output voltage from 1.2 V to $V_{IN} - V_{DO}$ with high PSRR and low noise.

User programmable soft start with an external capacitor is available in the LFCSP and SOIC packages.

The ADP7118 is available in a 6-lead, 2 mm × 2 mm LFCSP making it not only a very compact solution, but it also provides excellent thermal performance for applications requiring up to 200 mA of output current in a small, low profile footprint. The ADP7118 is also available in a 5-lead TSOT and an 8-lead SOIC.

Rev. D Document Feedback

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12/2014—Rev. 0 to Rev. A

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9/2014—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = V_{OUT} + 1 V or 2.7 V, whichever is greater, V_{OUT} = 5 V, EN = V_{IN}, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, C_{SS} = 0 pF, T_A = 25°C for typical specifications, T_J = −40°C to +125°C for minimum/maximum specifications, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}		2.7		20	V
OPERATING SUPPLY CURRENT	I_{GND}	I_{OUT} = 0 µA		50	140	µA
		I_{OUT} = 10 mA		80	190	µA
		I_{OUT} = 200 mA		180	320	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN = GND		1.8		µA
		EN = GND, V_{IN} = 20 V		3.0		µA
		EN = GND			10	µA
OUTPUT VOLTAGE ACCURACY						
Output Voltage Accuracy	V_{OUT}	I_{OUT} = 10 mA, T_J = 25°C	−0.8		+0.8	%
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V, T_J = −40°C to +85°C	−1.2		+1.5	%
		100 µA < I_{OUT} < 200 mA, V_{IN} = (V_{OUT} + 1 V) to 20 V	−1.8		+1.8	%
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 1 V) to 20 V	−0.015		+0.015	%/V
LOAD REGULATION[1]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 100 µA to 200 mA		0.002	0.004	%/mA
SENSE INPUT BIAS CURRENT	$SENSE_{I-BIAS}$	100 µA < I_{OUT} < 200 mA V_{IN} = (V_{OUT} + 1 V) to 20 V		10	1000	nA
DROPOUT VOLTAGE[2]	$V_{DROPOUT}$	I_{OUT} = 10 mA		30	60	mV
		I_{OUT} = 200 mA		200	420	mV
START-UP TIME[3]	$t_{START-UP}$	V_{OUT} = 5 V		380		µs
SOFT START SOURCE CURRENT	$SS_{I-SOURCE}$	SS = GND		1.15		µA
CURRENT-LIMIT THRESHOLD[4]	I_{LIMIT}		250	360	460	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		150		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
UNDERVOLTAGE THRESHOLDS						
Input Voltage Rising	$UVLO_{RISE}$				2.69	V
Input Voltage Falling	$UVLO_{FALL}$		2.2			V
Hysteresis	$UVLO_{HYS}$			230		mV
PRECISION EN INPUT		2.7 V ≤ V_{IN} ≤ 20 V				
Logic High	EN_{HIGH}		1.15	1.22	1.30	V
Logic Low	EN_{LOW}		1.06	1.12	1.18	V
Logic Hysteresis	EN_{HYS}			100		mV
Leakage Current	I_{EN-LKG}	EN = V_{IN} or GND		0.04	1	µA
Delay Time	t_{EN-DLY}	From EN rising from 0 V to V_{IN} to 0.1 × V_{OUT}		80		µs
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, all output voltage options		11		µV rms
POWER SUPPLY REJECTION RATIO	PSRR	1 MHz, V_{IN} = 7 V, V_{OUT} = 5 V		50		dB
		100 kHz, V_{IN} = 7 V, V_{OUT} = 5 V		68		dB
		10 kHz, V_{IN} = 7 V, V_{OUT} = 5 V		88		dB

[1] Based on an endpoint calculation using 100 µA and 200 mA loads. See Figure 7 for typical load regulation performance for loads less than 1 mA.
[2] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. Dropout applies only for output voltages above 2.7 V.
[3] Start-up time is defined as the time between the rising edge of EN to OUT being at 90% of the nominal value.
[4] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 5.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 5.0 V or 4.5 V.

INPUT AND OUTPUT CAPACITANCE, RECOMMENDED SPECIFICATIONS

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT AND OUTPUT CAPACITANCE						
Minimum Capacitance[1]	C_{MIN}	T_A = −40°C to +125°C	1.5			µF
Capacitor Effective Series Resistance (ESR)	R_{ESR}	T_A = −40°C to +125°C	0.001		0.3	Ω

[1] The minimum input and output capacitance must be greater than 1.5 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended, while Y5V and Z5U capacitors are not recommended for use with any LDO.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +24 V
VOUT to GND	−0.3 V to VIN
EN to GND	−0.3 V to +24 V
SENSE/ADJ to GND	−0.3 V to +6 V
SS to GND	−0.3 V to VIN or +6 V (whichever is less)
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J)	150°C
Operating Ambient Temperature (T_A) Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP7118 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated.

In applications with moderate power dissipation and low printed circuit board (PCB) thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature of the device is dependent on the ambient temperature, the power dissipation (P_D) of the device, and the junction-to-ambient thermal resistance of the package (θ_{JA}).

Maximum T_J is calculated from the T_A and P_D using the formula

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

θ_{JA} of the package is based on modeling and calculation using a 4-layer board. The θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified values of θ_{JA} are based on a 4-layer, 4 inches × 3 inches circuit board. See JESD51-7 and JESD51-9 for detailed information on the board construction.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. The Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance (θ_{JB}). Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum T_J is calculated from the board temperature (T_B) and P_D using the formula

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (2)$$

See JESD51-8 and JESD51-12 for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA}, θ_{JC}, and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

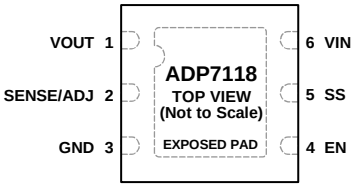
Package Type	θ_{JA}	θ_{JC}	Ψ_{JB}	Unit
6-Lead LFCSP	72.1	42.3	47.1	°C/W
8-Lead SOIC	52.7	41.5	32.7	°C/W
5-Lead TSOT	170	N/A[1]	43	°C/W

[1] N/A means not applicable.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD CONNECT TO THE GROUND PLANE ON THE BOARD.

11849-003

Figure 3. 6-Lead LFCSP Pin Configuration

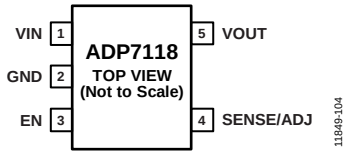


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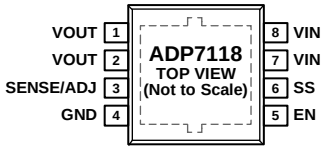
Figure 4. 5-Lead TSOT Pin Configuration



NOTES
1. THE EXPOSED PAD ON THE BOTTOM OF THE PACKAGE ENHANCES THERMAL PERFORMANCE AND IS ELECTRICALLY CONNECTED TO GND INSIDE THE PACKAGE. IT IS RECOMMENDED THAT THE EXPOSED PAD CONNECT TO THE GROUND PLANE ON THE BOARD.

11849-105

Figure 5. 8-Lead SOIC Pin Configuration

Table 5. Pin Function Descriptions

Pin No.				
6-Lead LFCSP	**8-Lead SOIC**	**5-Lead TSOT**	**Mnemonic**	**Description**
1	1, 2	5	VOUT	Regulated Output Voltage. Bypass VOUT to GND with a 2.2 µF or greater capacitor.
2	3	4	SENSE/ADJ	Sense Input (SENSE). Connect to load. An external resistor divider may also set the output voltage higher than the fixed output voltage (ADJ).
3	4	2	GND	Ground.
4	5	3	EN	The enable pin controls the operation of the LDO. Drive EN high to turn on the regulator. Drive EN low to turn off the regulator. For automatic startup, connect EN to VIN.
5	6	Not applicable	SS	Soft Start. An external capacitor connected to this pin determines the soft-start time. Leave this pin open for a typical 380 µs start-up time. Do not ground this pin.
6	7, 8	1	VIN	Regulator Input Supply. Bypass VIN to GND with a 2.2 µF or greater capacitor.
		Not applicable	EP	Exposed Pad. The exposed pad on the bottom of the package enhances thermal performance and is electrically connected to GND inside the package. It is recommended that the exposed pad connect to the ground plane on the board.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = V_{OUT} + 1 V or 2.7 V, whichever is greater, V_{OUT} = 5 V, I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 2.2 µF, T_A = 25°C, unless otherwise noted.

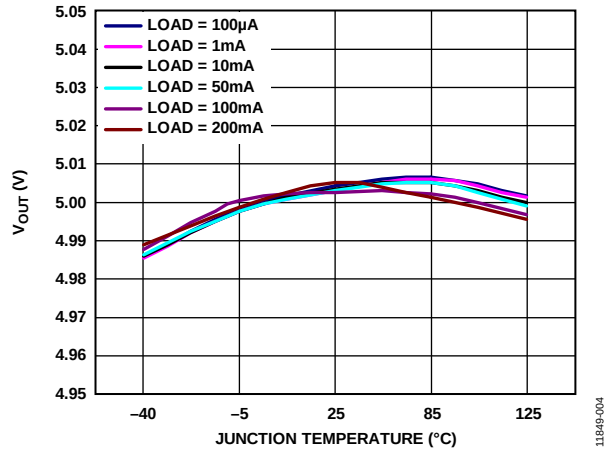


Figure 6. Output Voltage (V_{OUT}) vs. Junction Temperature

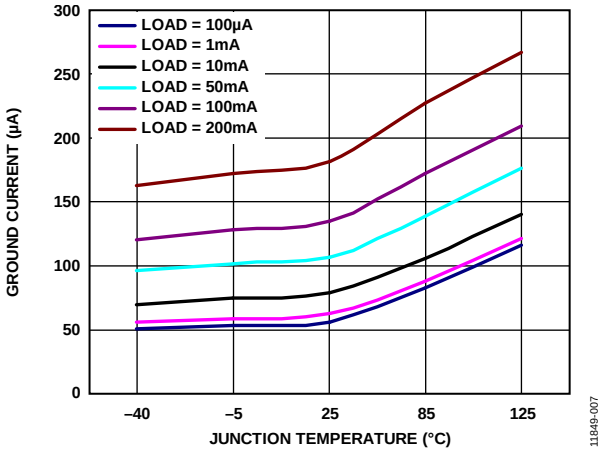


Figure 9. Ground Current vs. Junction Temperature

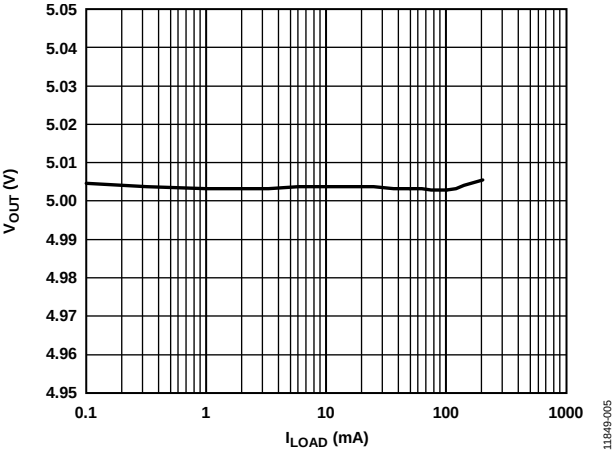


Figure 7. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD})

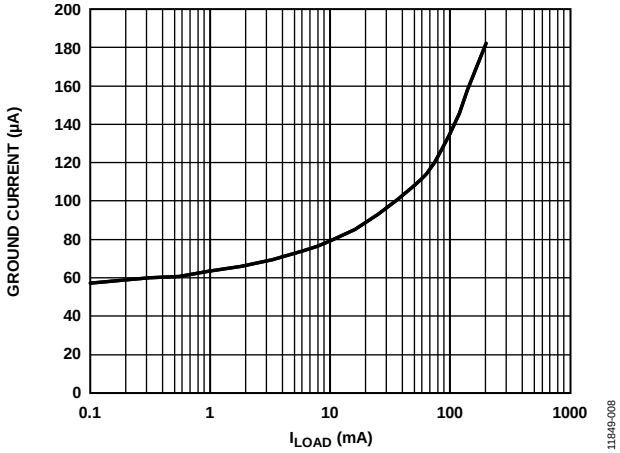


Figure 10. Ground Current vs. Load Current (I_{LOAD})

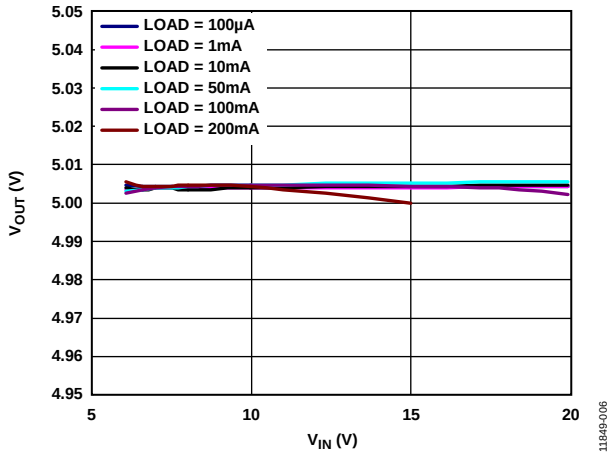


Figure 8. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN})

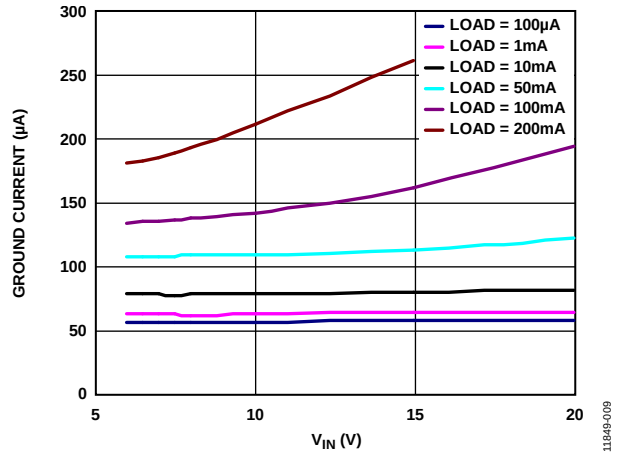


Figure 11. Ground Current vs. Input Voltage (V_{IN})

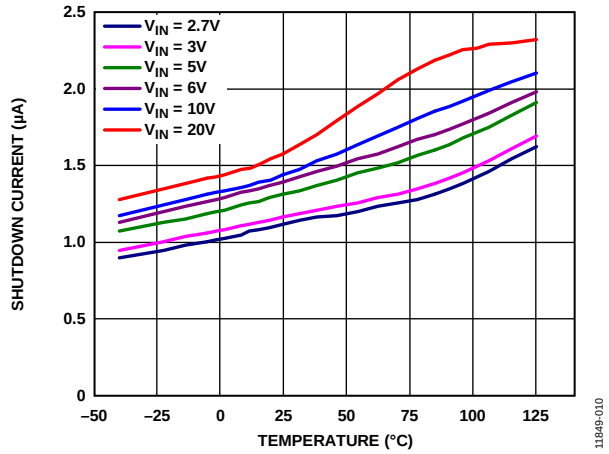


Figure 12. Shutdown Current vs. Temperature at Various Input Voltages

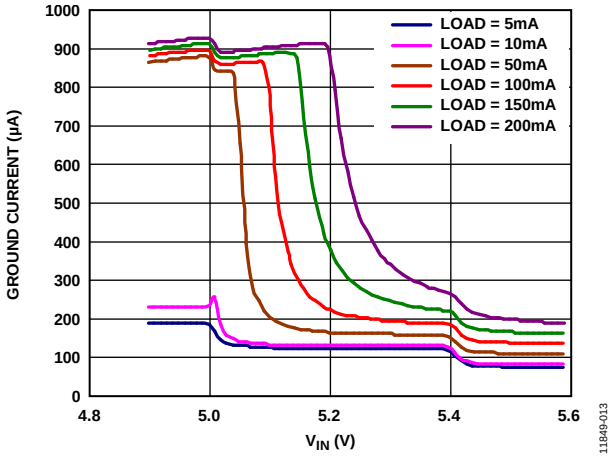


Figure 15. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 5 V

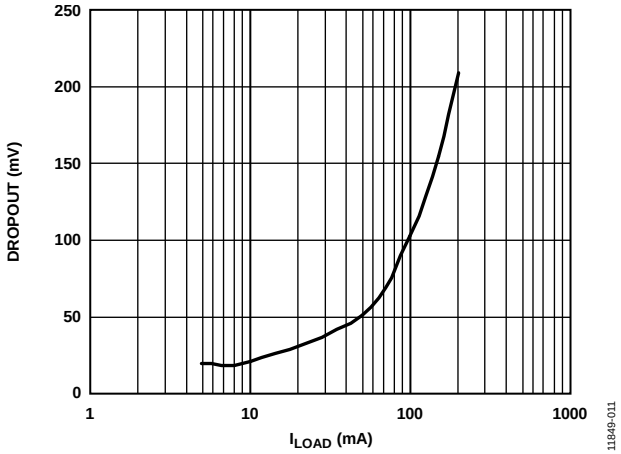


Figure 13. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = 5 V

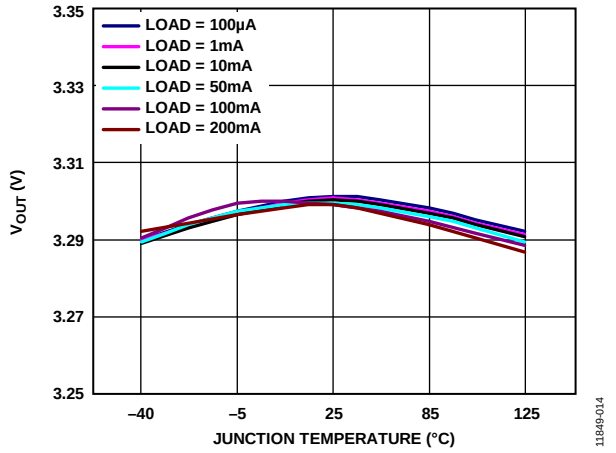


Figure 16. Output Voltage (V_{OUT}) vs. Junction Temperature, V_{OUT} = 3.3 V

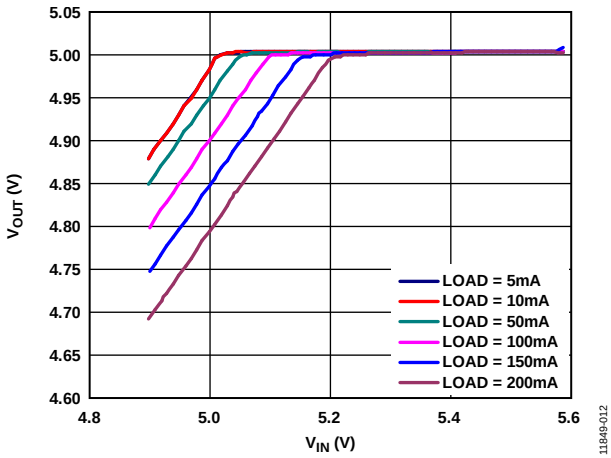


Figure 14. Output Voltage(V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 5 V

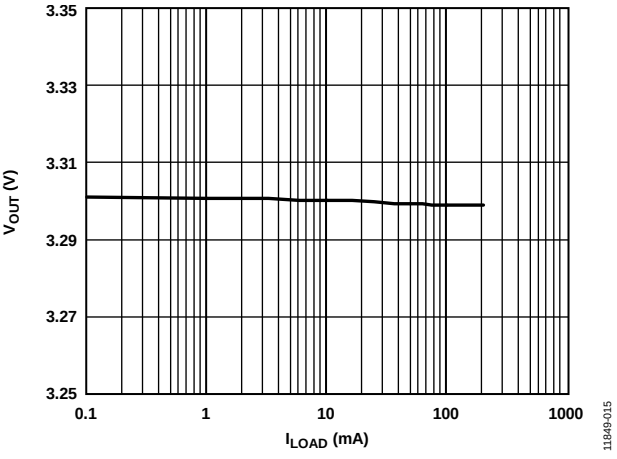


Figure 17. Output Voltage (V_{OUT}) vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

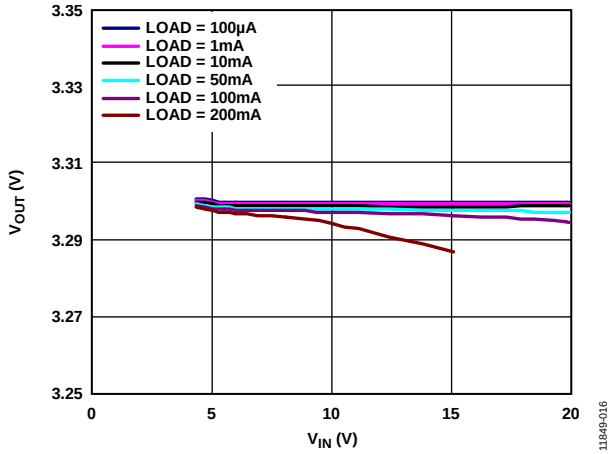


Figure 18. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}), V_{OUT} = 3.3 V

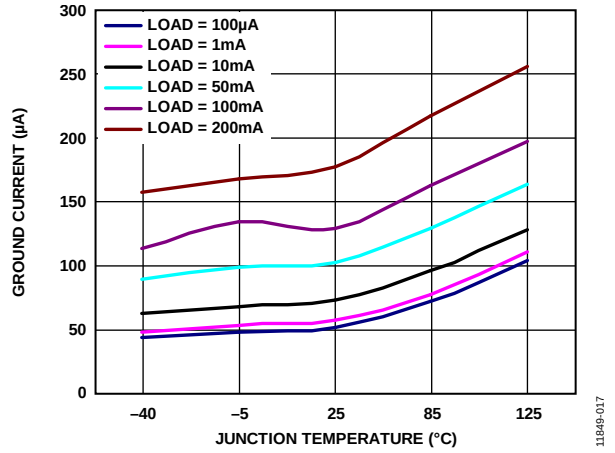


Figure 19. Ground Current vs. Junction Temperature, V_{OUT} = 3.3 V

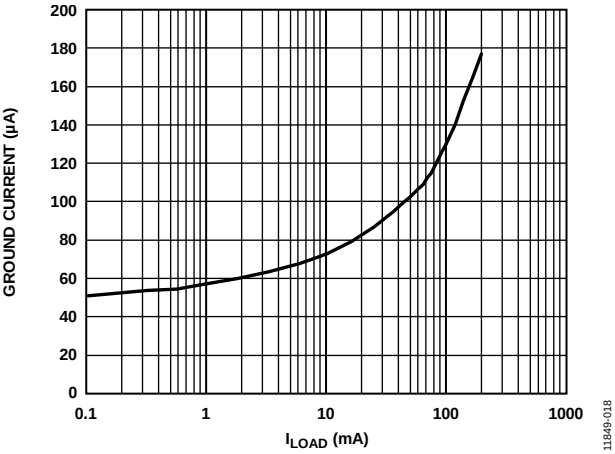


Figure 20. Ground Current vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

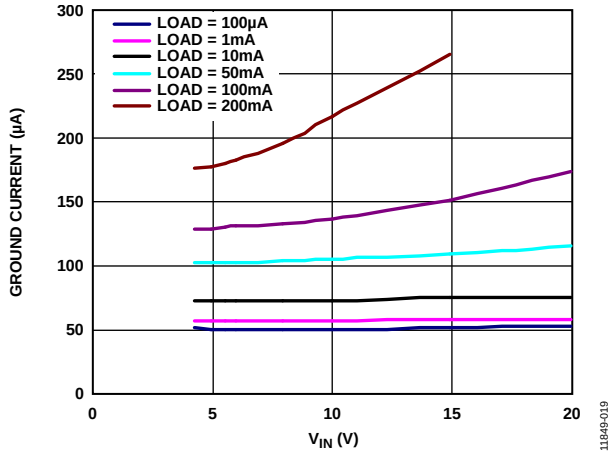


Figure 21. Ground Current vs. Input Voltage (V_{IN}), V_{OUT} = 3.3 V

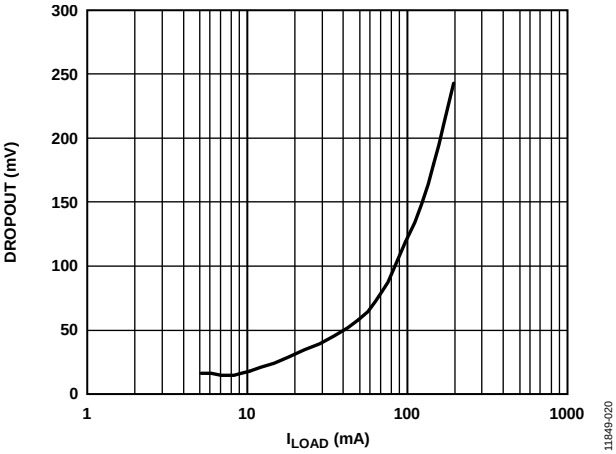


Figure 22. Dropout Voltage vs. Load Current (I_{LOAD}), V_{OUT} = 3.3 V

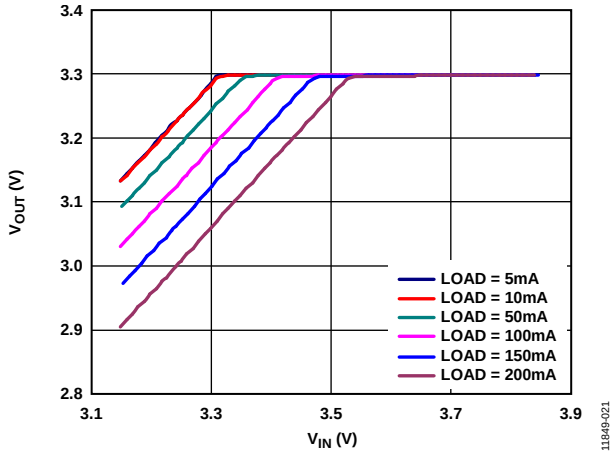


Figure 23. Output Voltage (V_{OUT}) vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

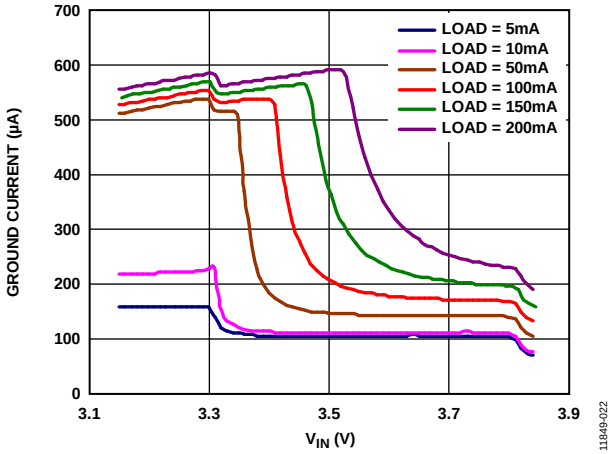


Figure 24. Ground Current vs. Input Voltage (V_{IN}) in Dropout, V_{OUT} = 3.3 V

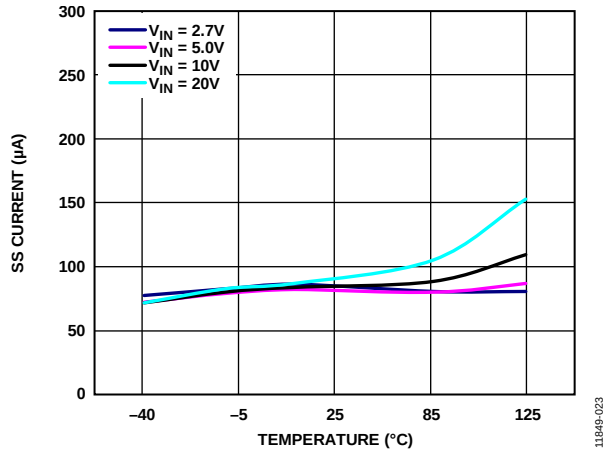


Figure 25. Soft Start (SS) Current vs. Temperature, Multiple Input Voltages, V_{OUT} = 5 V

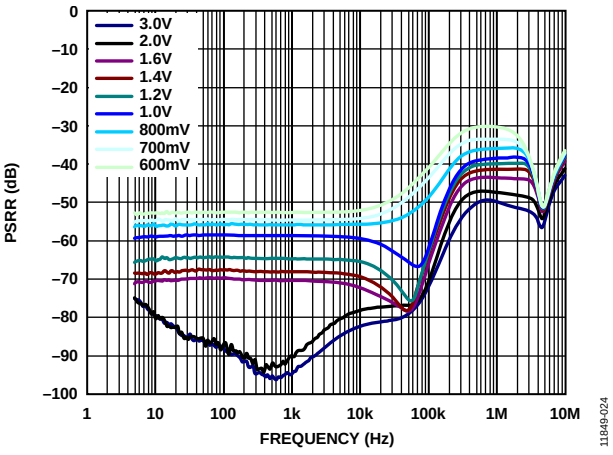


Figure 26. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 1.8 V, for Various Headroom Voltages

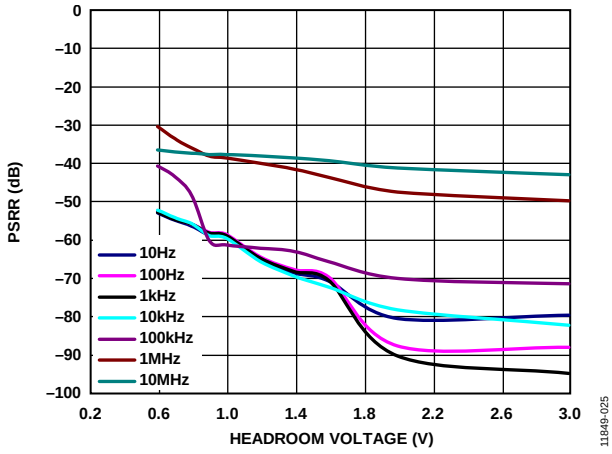


Figure 27. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = 1.8 V,for Different Frequencies

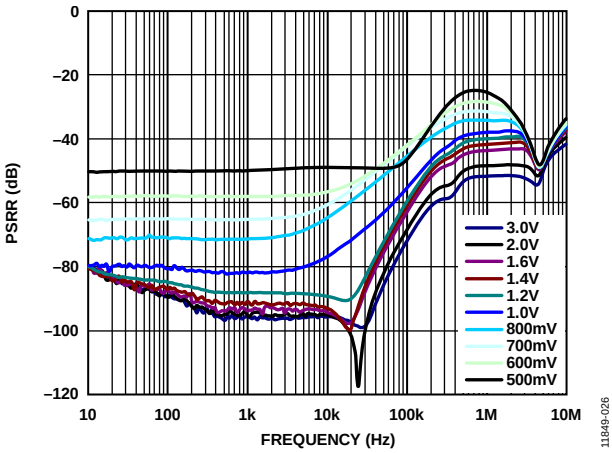


Figure 28. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 3.3 V, for Various Headroom Voltages

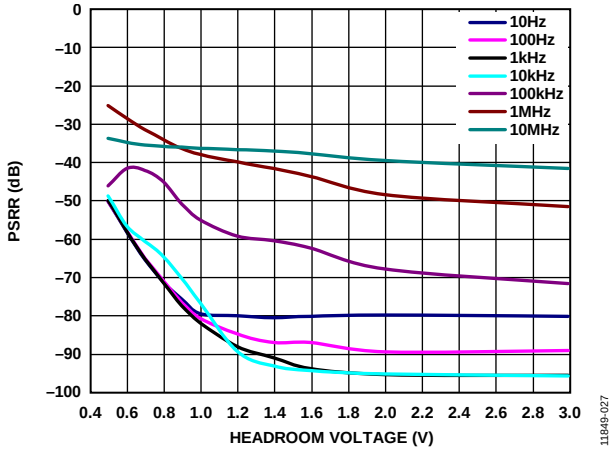


Figure 29. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = 3.3 V, for Different Frequencies

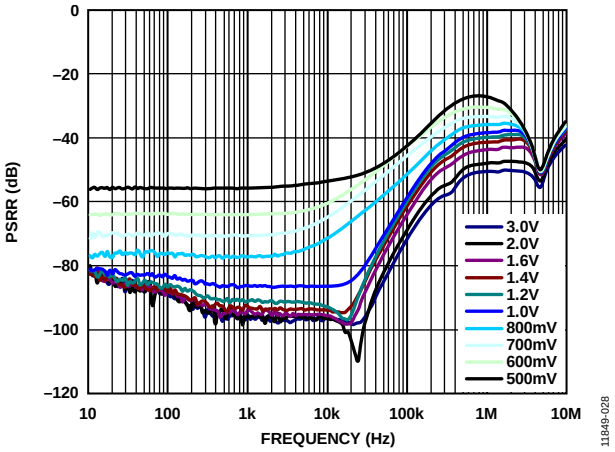


Figure 30. Power Supply Rejection Ratio (PSRR) vs. Frequency, V_{OUT} = 5 V, for Various Headroom Voltages

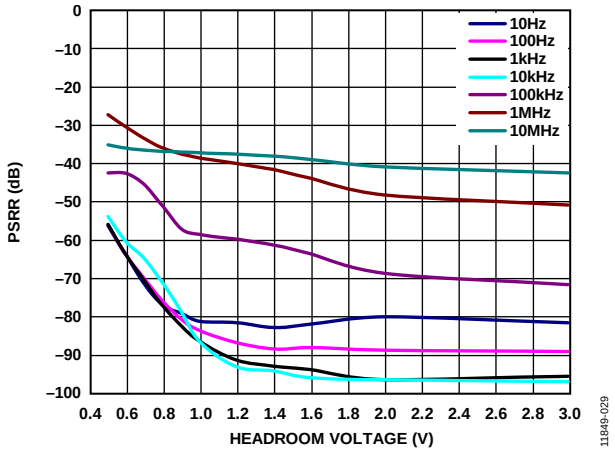


Figure 31. Power Supply Rejection Ratio (PSRR) vs. Headroom Voltage, V_{OUT} = 5 V, for Different Frequencies

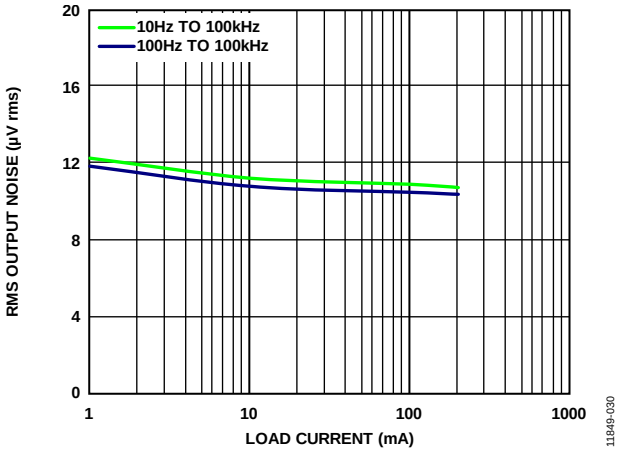


Figure 32. RMS Output Noise vs. Load Current

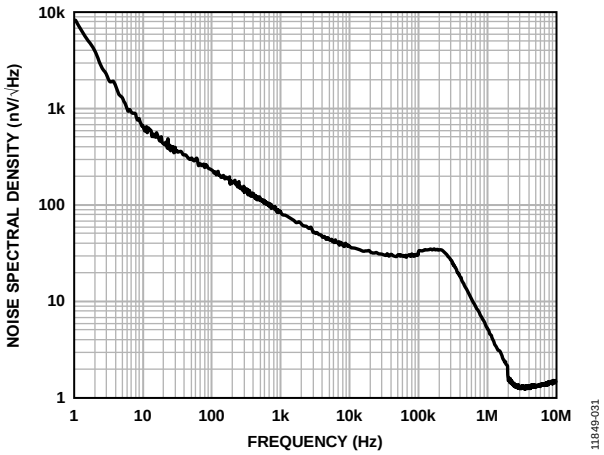


Figure 33. Output Noise Spectral Density vs. Frequency, I_{LOAD} = 10 mA

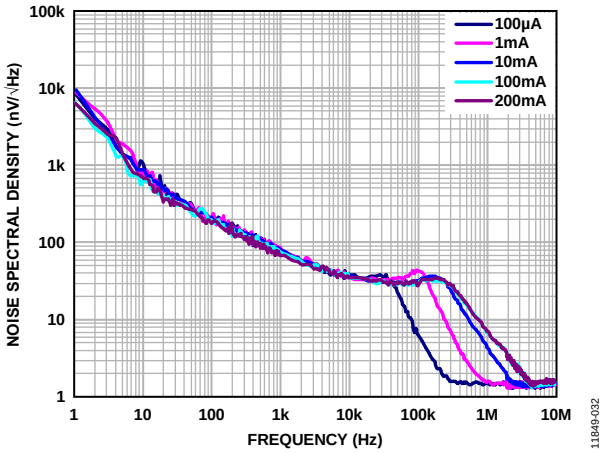


Figure 34. Output Noise Spectral Density vs. Frequency, for Different Loads

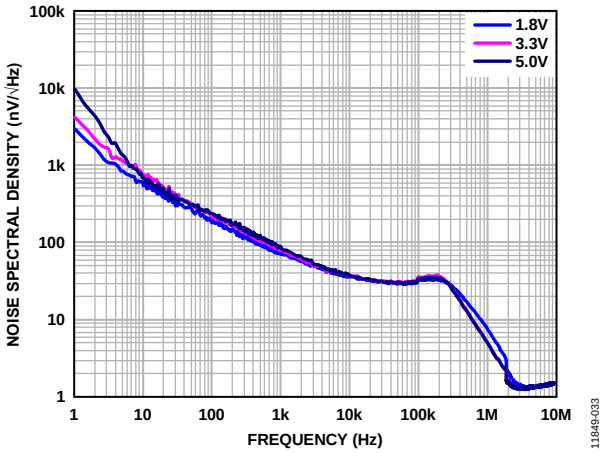


Figure 35. Output Noise Spectral Density vs. Frequency for Different Output Voltages

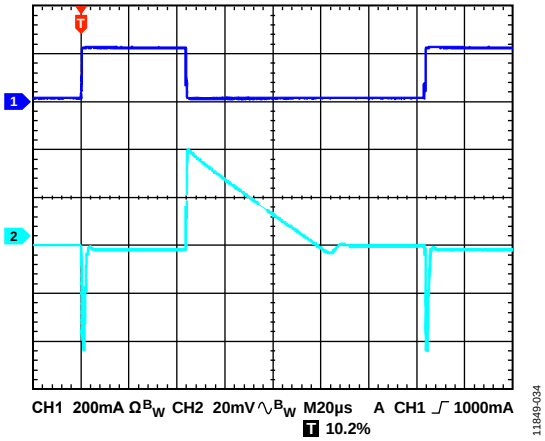


Figure 36. Load Transient Response, I_{LOAD} = 1 mA to 200 mA, V_{OUT} = 5 V, V_{IN} = 7 V, CH1 Load Current, CH2 V_{OUT}

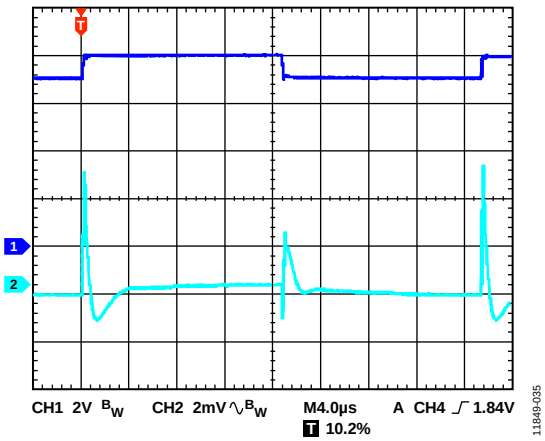


Figure 37. Line Transient Response, I_{LOAD} = 200 mA, V_{OUT} = 5 V, CH1 V_{IN}, CH2 V_{OUT}

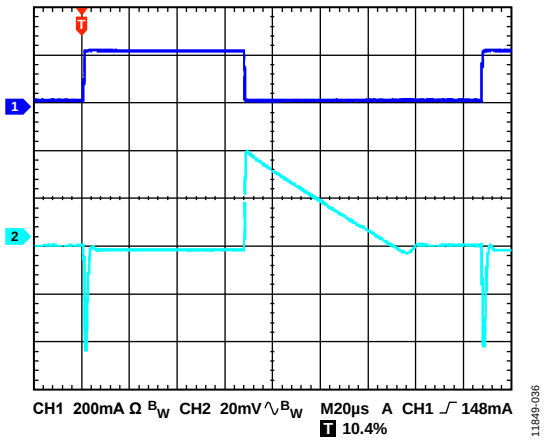


Figure 38. Load Transient Response, I_{LOAD} = 1 mA to 200 mA, V_{OUT} = 3.3 V, V_{IN} = 5 V, CH1 Load Current, CH2 V_{OUT}

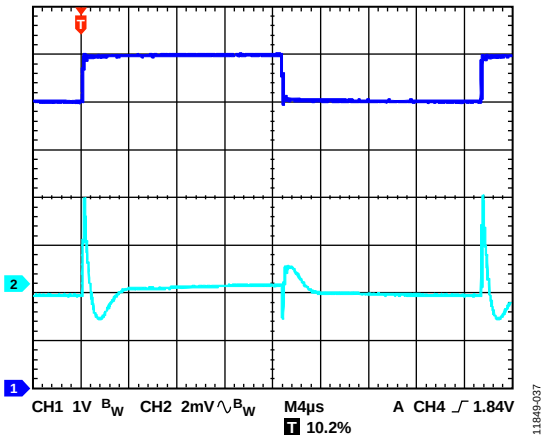


Figure 39. Line Transient Response, I_{LOAD} = 200 mA, V_{OUT} = 3.3 V, CH1 V_{IN}, CH2 V_{OUT}

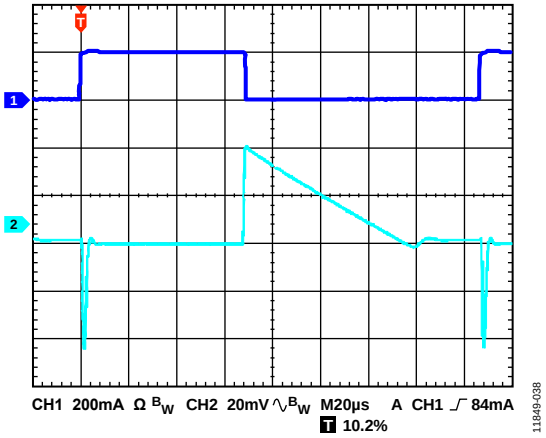


Figure 40. Load Transient Response, I_{LOAD} = 1 mA to 200 mA, V_{OUT} = 1.8 V, V_{IN} = 3 V, CH1 Load Current, CH2 V_{OUT}

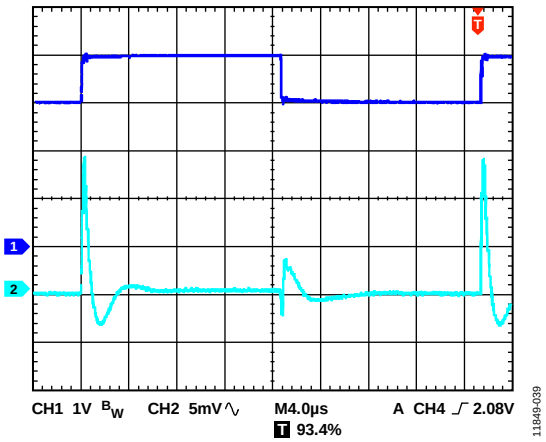


Figure 41. Line Transient Response, I_{LOAD} = 200 mA, V_{OUT} = 1.8 V, CH1 V_{IN}, CH2 V_{OUT}

THEORY OF OPERATION

The ADP7118 is a low quiescent current, LDO linear regulator that operates from 2.7 V to 20 V and provides up to 200 mA of output current. Drawing a low 180 µA of quiescent current (typical) at full load makes the ADP7118 ideal for portable equipment. Typical shutdown current consumption is less than 3 µA at room temperature.

Optimized for use with small 2.2 µF ceramic capacitors, the ADP7118 provides excellent transient performance.

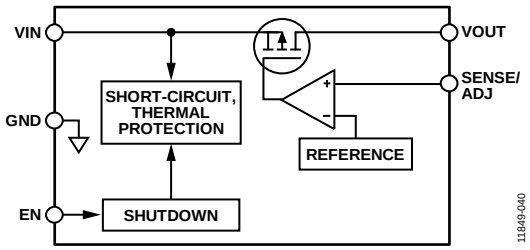


Figure 42. Internal Block Diagram

Internally, the ADP7118 consists of a reference, an error amplifier, a feedback voltage divider, and a PMOS pass transistor. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to pass and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to pass and decreasing the output voltage.

The ADP7118 is available in 16 fixed output voltage options, ranging from 1.2 V to 5.0 V. The ADP7118 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5 V output can be set to a 6 V output according to the following equation:

$$V_{OUT} = 5\ V(1 + R1/R2) \quad (3)$$

where R1 and R2 are the resistors in the output voltage divider shown in Figure 43.

To set the output voltage of the adjustable ADP7118, replace 5 V in Equation 3 with 1.2 V.

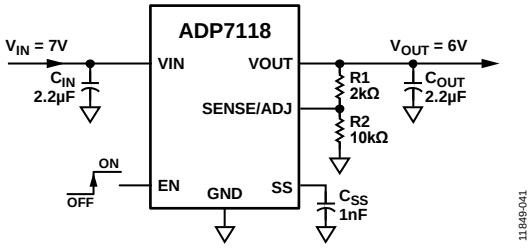


Figure 43. Typical Adjustable Output Voltage Application Schematic

It is recommended that the R2 value be less than 200 kΩ to minimize errors in the output voltage caused by the SENSE/ADJ pin input current. For example, when R1 and R2 each equal 200 kΩ and the default output voltage is 1.2 V, the adjusted output voltage is 2.4 V. The output voltage error introduced by the SENSE/ADJ pin input current is 1 mV or 0.04%, assuming a typical SENSE/ADJ pin input current of 10 nA at 25°C.

The ADP7118 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. When EN is high, VOUT turns on, and when EN is low, VOUT turns off. For automatic startup, EN can be tied to VIN.

APPLICATIONS INFORMATION

ADIsimPOWER DESIGN TOOL

The ADP7118 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs optimized for a specific design goal. The tools enable the user to generate a full schematic, bill of materials, and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and parts count, taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about, and to obtain ADIsimPower design tools, visit www.analog.com/ADIsimPower.

CAPACITOR SELECTION

Output Capacitor

The ADP7118 is designed for operation with small, space-saving ceramic capacitors, but functions with general-purpose capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 2.2 µF capacitance with an ESR of 0.3 Ω or less is recommended to ensure the stability of the ADP7118. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP7118 to large changes in load current. Figure 44 shows the transient responses for an output capacitance value of 2.2 µF.

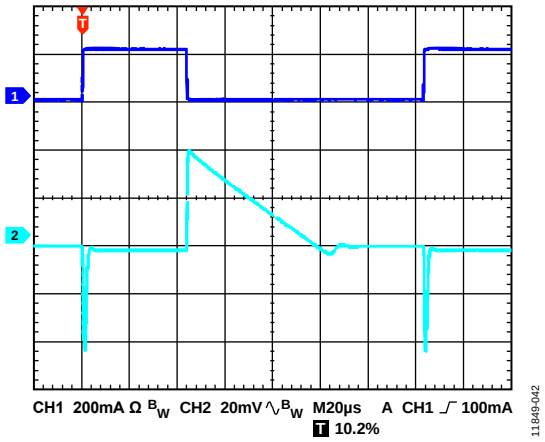


Figure 44. Output Transient Response, V_{OUT} = 5 V, C_{OUT} = 2.2 µF, CH1 Load Current, CH2 V_{OUT}

Input Bypass Capacitor

Connecting a 2.2 µF capacitor from VIN to GND reduces the circuit sensitivity to the PCB layout, especially when long input traces or high source impedance is encountered. If greater than 2.2 µF of output capacitance is required, increase the input capacitor to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP7118, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V to 100 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 45 depicts the capacitance vs. voltage bias characteristic of an 0805, 2.2 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

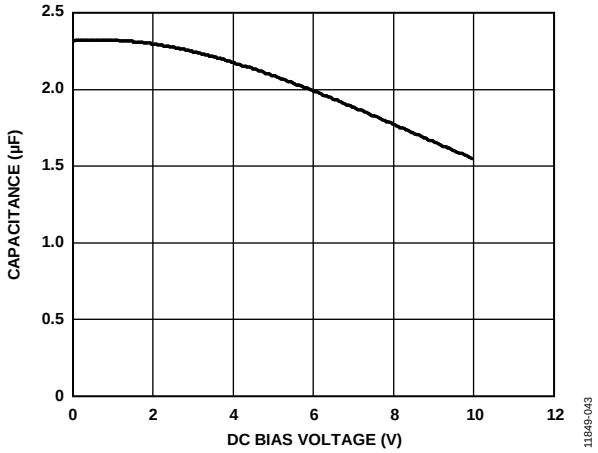


Figure 45. Capacitance vs. Voltage Characteristic

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (4)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 2.09 µF at 5 V, as shown in Figure 45.

These values in Equation 1 yield

$$C_{EFF} = 2.09\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 1.59\ \mu F \quad (5)$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP7118, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

PROGRAMABLE PRECISION ENABLE

The ADP7118 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 46, when a rising voltage on EN crosses the upper threshold, nominally 1.2 V, VOUT turns on. When a falling voltage on EN crosses the lower threshold, nominally 1.1 V, VOUT turns off. The hysteresis of the EN threshold is approximately 100 mV.

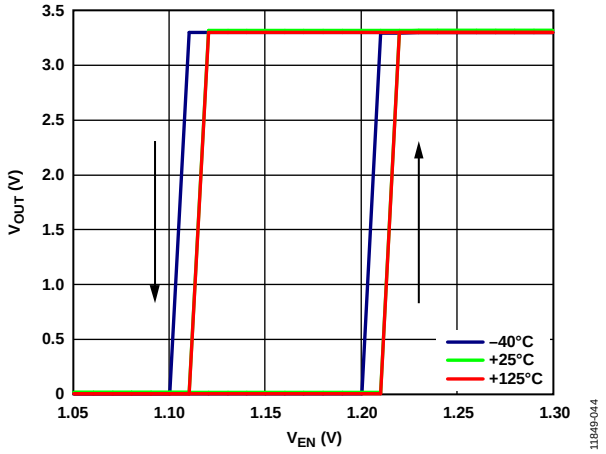


Figure 46. Typical V_{OUT} Response to EN Pin Operation

The upper and lower thresholds are user programmable and can be set higher than the nominal 1.2 V threshold by using two resistors. The resistance values, R_{EN1} and R_{EN2}, can be determined from the following:

$$R_{EN2} = \text{nominally 10 k}\Omega \text{ to 100 k}\Omega \quad (6)$$

$$R_{EN1} = R_{EN2} \times (V_{IN} - 1.2\text{ V})/1.2\text{ V} \quad (7)$$

where:
V_{IN} is the desired turn-on voltage.

The hysteresis voltage increases by the factor $(R_{EN1} + R_{EN2})/R_{EN2}$. For the example shown in Figure 47, the enable threshold is 3.6 V with a hysteresis of 300 mV.

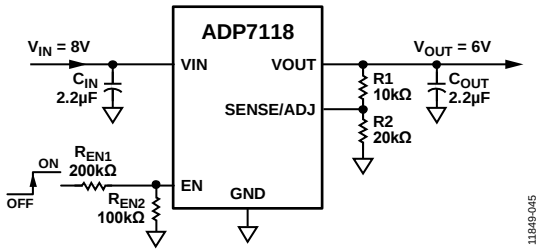


Figure 47. Typical EN Pin Voltage Divider

Figure 46 shows the typical hysteresis of the EN pin. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

SOFT START

The ADP7118 uses an internal soft start (SS pin open) to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 380 µs from the time the EN active threshold is crossed to when the output reaches 90% of the final value. As shown in Figure 48, the start-up time is independent on the output voltage setting.

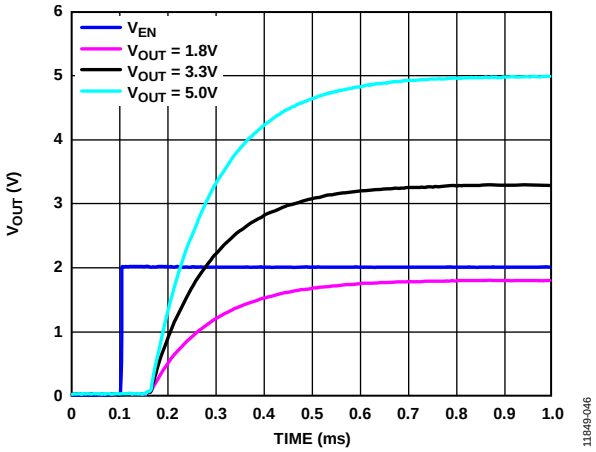


Figure 48. Typical Start-Up Behavior

An external capacitor connected to the SS pin determines the soft start time. This SS pin can be left open for a typical 380 µs start-up time. Do not ground this pin. When an external soft start capacitor (C_{SS}) is used, the soft start time is determined by the following equation:

$$SS_{TIME}\text{ (sec)} = t_{START\text{-}UP\ at\ 0\ pF} + (0.6 \times C_{SS})/I_{SS} \quad (8)$$

where:
$t_{START\text{-}UP\ at\ 0\ pF}$ is the start-up time at C_{SS} = 0 pF (typically 380 µs).
C_{SS} is the soft start capacitor (F).
I_{SS} is the soft start current (typically 1.15 µA).

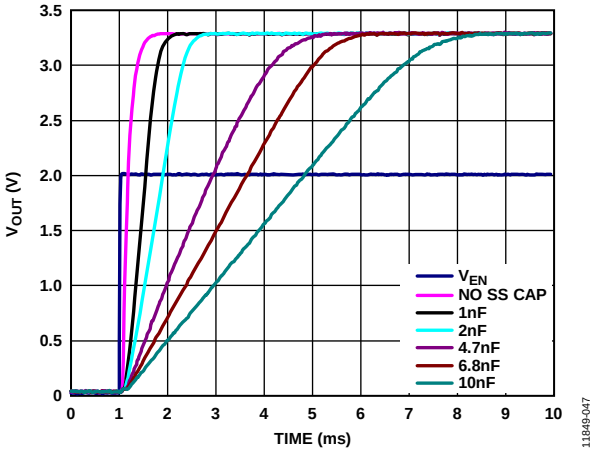


Figure 49. Typical Soft Start Behavior, Different C_{SS}

NOISE REDUCTION OF THE ADP7118 IN ADJUSTABLE MODE

The ultralow output noise of the ADP7118 is achieved by keeping the LDO error amplifier in unity gain and setting the reference voltage equal to the output voltage. This architecture does not work for an adjustable output voltage LDO in the conventional sense. However, the ADP7118 architecture allows any fixed output voltage to be set to a higher voltage with an external voltage divider. For example, a fixed 5 V output can be set to a 10 V output according to Equation 3 (see Figure 50):

$$V_{OUT} = 5\ V(1 + R1/R2)$$

The disadvantage in using the ADP7118 in this manner is that the output voltage noise is proportional to the output voltage. Therefore, it is best to choose a fixed output voltage that is close to the target voltage to minimize the increase in output noise.

The adjustable LDO circuit can be modified to reduce the output voltage noise to levels close to that of the fixed output ADP7118. The circuit shown in Figure 50 adds two additional components to the output voltage setting resistor divider. C_{NR} and R_{NR} are added in parallel with R1 to reduce the ac gain of the error amplifier. R_{NR} is chosen to be small with respect to R2. If R_{NR} is 1% to 10% of the value of R2, the minimum ac gain of the error amplifier is approximately 0.1 dB to 0.8 dB. The actual gain is determined by the parallel combination of R_{NR} and R1. This gain ensures that the error amplifier always operates at slightly greater than unity gain.

C_{NR} is chosen by setting the reactance of C_{NR} equal to$R1 - R_{NR}$ at a frequency between 1 Hz and 50 Hz. This setting places the frequency where the ac gain of the error amplifier is 3 dB down from the dc gain.

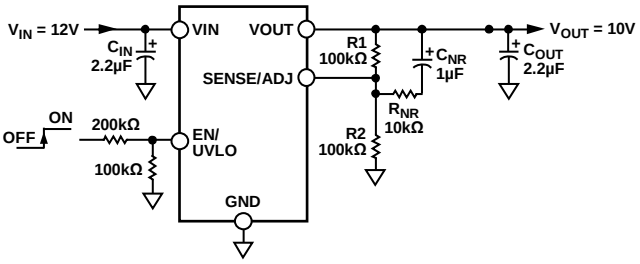


Figure 50. Noise Reduction Modification

The noise of the adjustable LDO is found by using the following formula, assuming the noise of a fixed output LDO is approximately 11 µV.

$$Noise = 11\ \mu V \times (R_{PAR} + R2)/R2 \quad (9)$$

where R_{PAR} is a parallel combination of *R1* and R_{NR}.

Based on the component values shown in Figure 50, the ADP7118 has the following characteristics:

- DC gain of 10 (20 dB)
- 3 dB roll-off frequency of 1.75 Hz
- High frequency ac gain of 1.099 (0.82 dB)
- Theoretical noise reduction factor of 9.1 (19.2 dB)
- Measured rms noise of the adjustable LDO without noise reduction is 70 µV rms
- Measured rms noise of the adjustable LDO with noise reduction is 12 µV rms
- Measured noise reduction of approximately 15.3 dB

Note that the measured noise reduction is less than the theoretical noise reduction. Figure 51 shows the noise spectral density of an adjustable ADP7118 set to 6 V and 12 V with and without the noise reduction network. The output noise with the noise reduction network is approximately the same for both voltages, especially beyond 100 Hz. The noise of the 6 V and 12 V outputs without the noise reduction network differs by a factor of 2 up to approximately 20 kHz. Above 40 kHz, the closed loop gain of the error amplifier is limited by the open loop gain characteristic. Therefore, the noise contribution from 20 kHz to 100 kHz is less than what it is if the error amplifier had infinite bandwidth. This is also the reason why the noise is less than what might be expected simply based on the dc gain, that is, 70 µV rms vs. 110 µV rms.

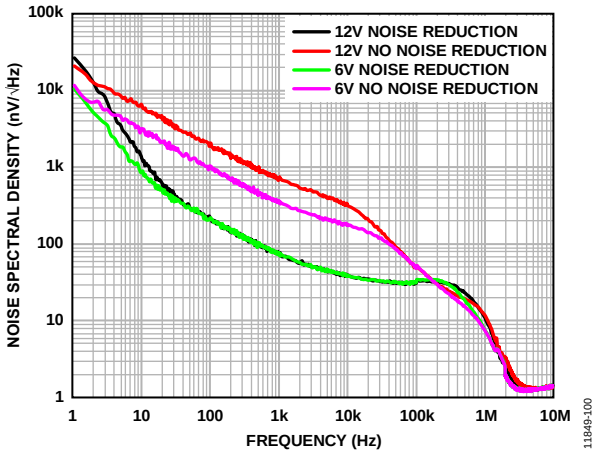


Figure 51. 6 V and 12 V Output Voltage with and Without Noise Reduction Network

EFFECT OF NOISE REDUCTION ON START-UP TIME

The start-up time of the ADP7118 is affected by the noise reduction network and must be considered in applications where power supply sequencing is critical.

The noise reduction circuit adds a pole in the feedback loop, slowing down the start-up time. To approximate the start-up time for an adjustable model with a noise reduction network using the following equation:

$$SSNR_{TIME}\ (\text{sec}) = 5.5 \times C_{NR} \times (R_{NR} + R_{FB1})$$

For a C_{NR}, R_{NR}, and R1 combination of 1 µF, 10 kΩ, and 100 kΩ, as shown in Figure 50, the start-up time is approximately 0.6 sec. When $SSNR_{TIME}$ is greater than SS_{TIME}, $SSNR_{TIME}$ dictates the length of the start-up time instead of the soft start capacitor.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP7118 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP7118 is designed to current limit when the output load reaches 400 mA (typical). When the output load exceeds 400 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to the operating value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP7118 current limits, so that only 400 mA is conducted into the short. If self heating of the junction is great enough to cause the temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 400 mA into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 400 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with a low input-to-output voltage differential, the ADP7118 does not dissipate much heat. However, in applications with high ambient temperature and/or high input voltage, the heat dissipated in the package may become large enough to cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 150°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP7118 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air (θ_{JA}). The θ_{JA} number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical θ_{JA} values of the 8-lead SOIC, 6-lead LFCSP, and 5-lead TSOT packages for various PCB copper sizes. Table 7 shows the typical Ψ_{JB} values of the 8-lead SOIC, 6-lead LFCSP, and 5-lead TSOT.

Table 6. Typical θ_{JA} Values

	θ_{JA} (°C/W)		
Copper Size (mm²)	**LFCSP**	**SOIC**	**TSOT**
25[1]	182.8	N/A[2]	N/A[2]
50	N/A[2]	181.4	152
100	142.6	145.4	146
500	83.9	89.3	131
1000	71.7	77.5	N/A[2]
6400	57.4	63.2	N/A[2]

[1] Device soldered to minimum size pin traces.
[2] N/A means not applicable.

Table 7. Typical Ψ_{JB} Values

Model	**Ψ_{JB} (°C/W)**
6-Lead LFCSP	24
8-Lead SOIC	38.8
5-Lead TSOT	43

To calculate the junction temperature of the ADP7118, use Equation 1.

$$T_J = T_A + (P_D \times \theta_{JA})$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (10)$$

where:
V_{IN} and V_{OUT} are input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (11)$$

As shown in Equation 4, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 52 to Figure 60 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

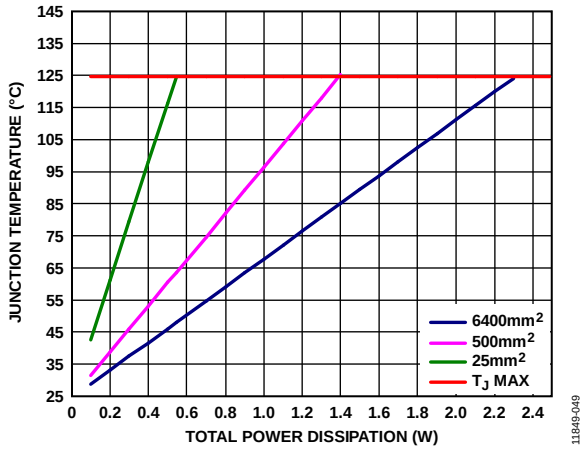


Figure 52. LFCSP, T_A = 25°C

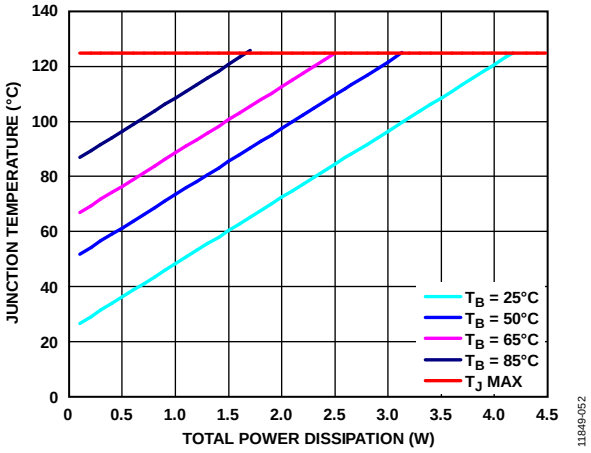


Figure 55. SOIC, T_A = 25°C

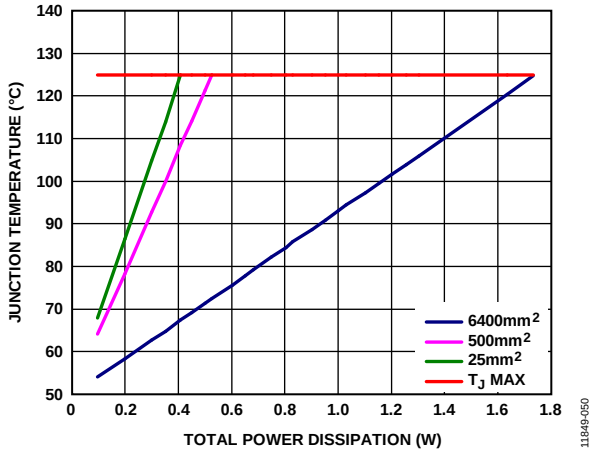


Figure 53. LFCSP, T_A = 50°C

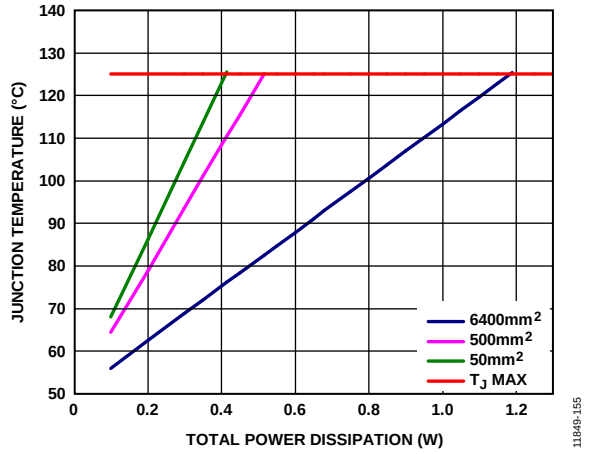


Figure 56. SOIC, T_A = 50°C

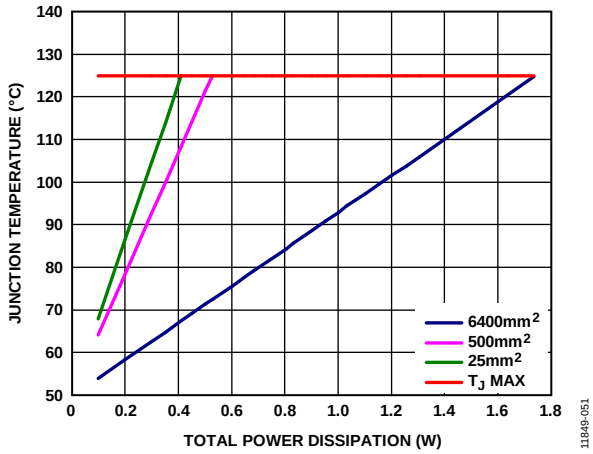


Figure 54. LFCSP, T_A = 85°C

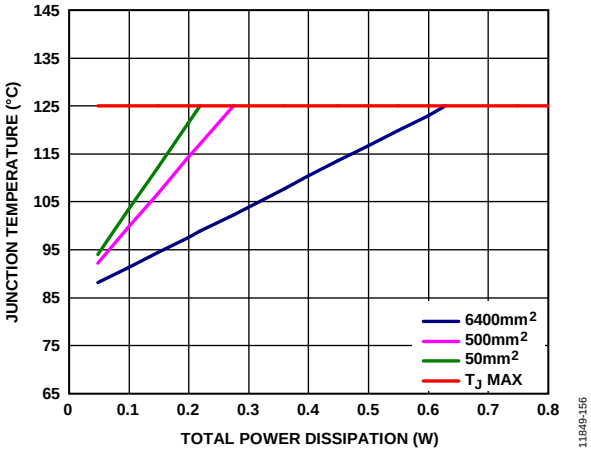


Figure 57. SOIC, T_A = 85°C

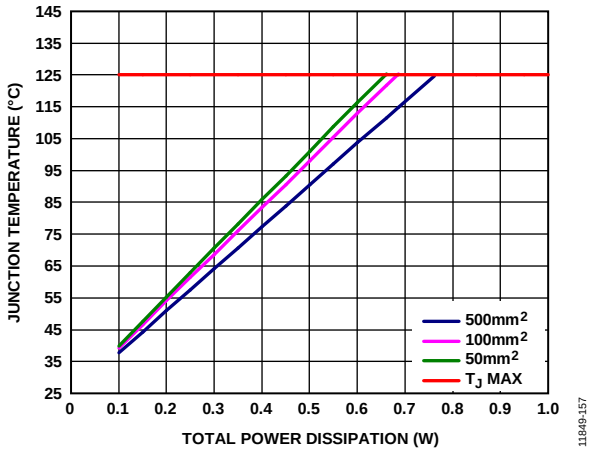


Figure 58. TSOT, T_A = 25°C

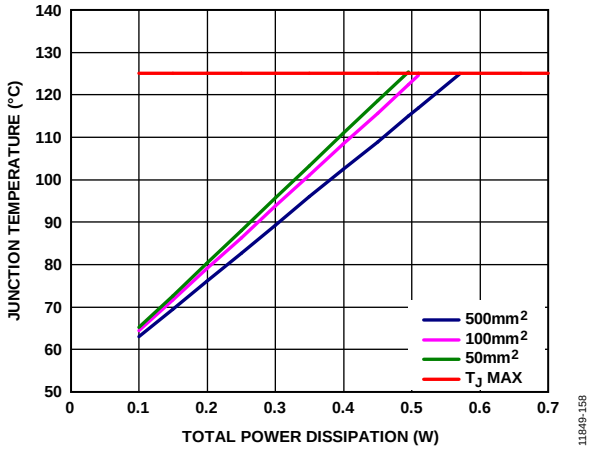


Figure 59. TSOT, T_A = 50°C

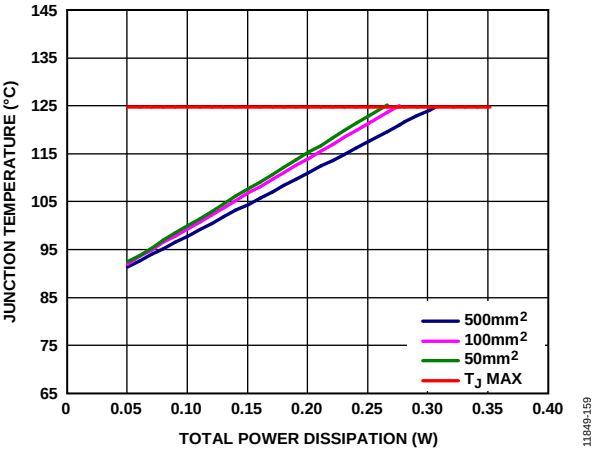


Figure 60. TSOT, T_A = 85°C

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 61, Figure 62, and Figure 63). Calculate the maximum junction temperature by using Equation 2.

$$T_J = T_B + (P_D \times \Psi_{JB})$$

The typical value of Ψ_{JB} is 24°C/W for the 8-lead LFCSP package, 38.8°C/W for the 8-lead SOIC package, and 43°C/W for the 5-lead TSOT package.

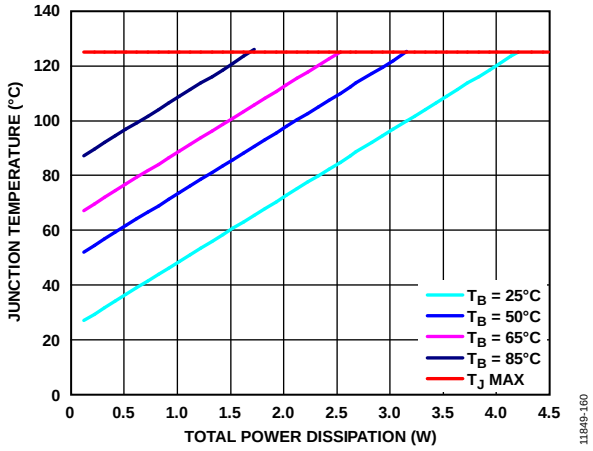


Figure 61. LFCSP Junction Temperature Rise, Different Board Temperatures

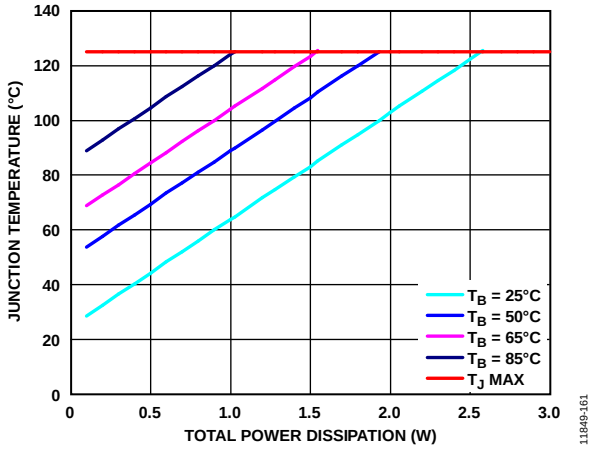


Figure 62. SOIC Junction Temperature Rise, Different Board Temperatures

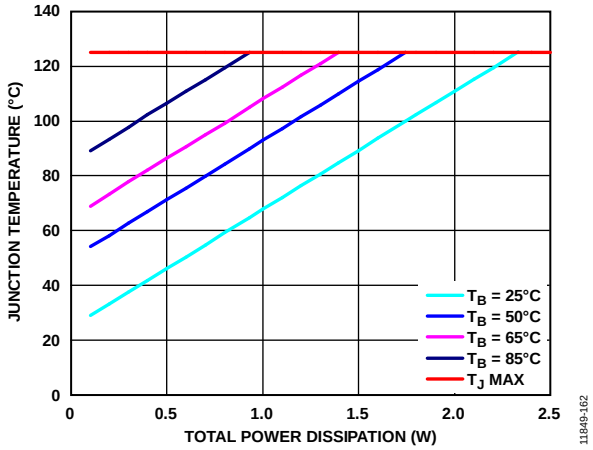


Figure 63. TSOT Junction Temperature Rise, Different Board Temperatures

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP7118. However, as listed in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUT and GND pins. Use of 0805 or 1206 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

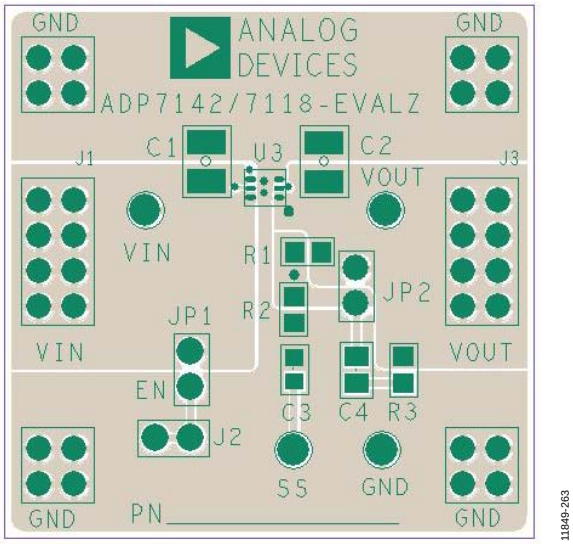


Figure 64. Example LFCSP PCB Layout

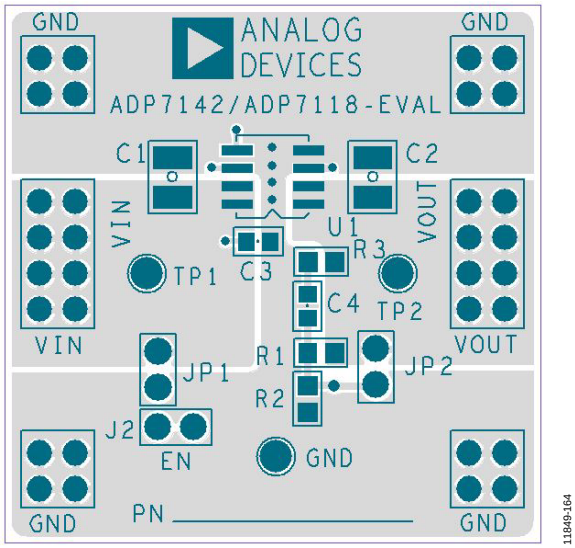


Figure 65. Example SOIC PCB Layout

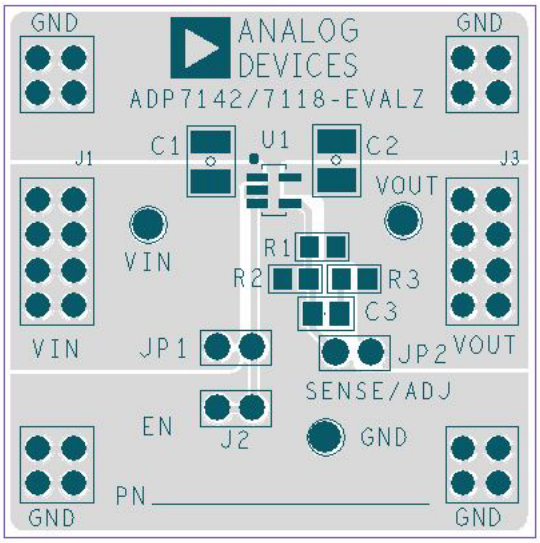


Figure 66. Example TSOT PCB Layout

Table 8. Recommended LDOs for Very Low Noise Operation

Device Number	V_{IN} Range (V)	V_{OUT} Fixed (V)	V_{OUT} Adjust (V)	I_{OUT} (mA)	I_Q at I_{OUT} (µA)	I_{GND-SD} Max (µA)	Soft Start	P_{GOOD}	Noise (Fixed) 10 Hz to 100 kHz (µV rms)	PSRR 100 kHz (dB)	PSRR 1 MHz	Package
ADP7102	3.3 to 20	1.5 to 9	1.22 to 19	300	750	75	No	Yes	15	60	40 dB	3 × 3mm 8-lead LFCSP, 8-lead SOIC
ADP7104	3.3 to 20	1.5 to 9	1.22 to 19	500	900	75	No	Yes	15	60	40 dB	3 × 3mm 8-lead LFCSP, 8-lead SOIC
ADP7105	3.3 to 20	1.8, 3.3, 5	1.22 to 19	500	900	75	Yes	Yes	15	60	40 dB	3 × 3mm 8-lead LFCSP, 8-lead SOIC
ADP7118	2.7 to 20	1.2 to 5	1.2 to 19	200	160	10	Yes	No	11	68	50 dB	2 × 2mm 6-lead LFCSP, 8-lead SOIC, 5-lead TSOT
ADP7142	2.7 to 40	1.2 to 5	1.2 to 39	200	160	10	Yes	No	11	68	50 dB	2 × 2mm 6-lead LFCSP, 8-lead SOIC, 5-lead TSOT
ADP7182	−2.7 to −28	−1.8 to −5	−1.22 to −27	−200	−650	−8	No	No	18	45	45 dB	2 × 2mm 6-lead LFCSP, 3 × 3mm 8-lead LFCSP, 5-lead TSOT

Table 9. Related Devices

Model	Input Voltage (V)	Output Current (mA)	Package
ADP7142ACP	2.7 to 40	200	6-Lead LFCSP
ADP7142ARD	2.7 to 40	200	8-Lead SOIC
ADP7142AUJ	2.7 to 40	200	5-Lead TSOT
ADP7112ACB	2.7 to 20	200	4-Lead WLCSP

OUTLINE DIMENSIONS

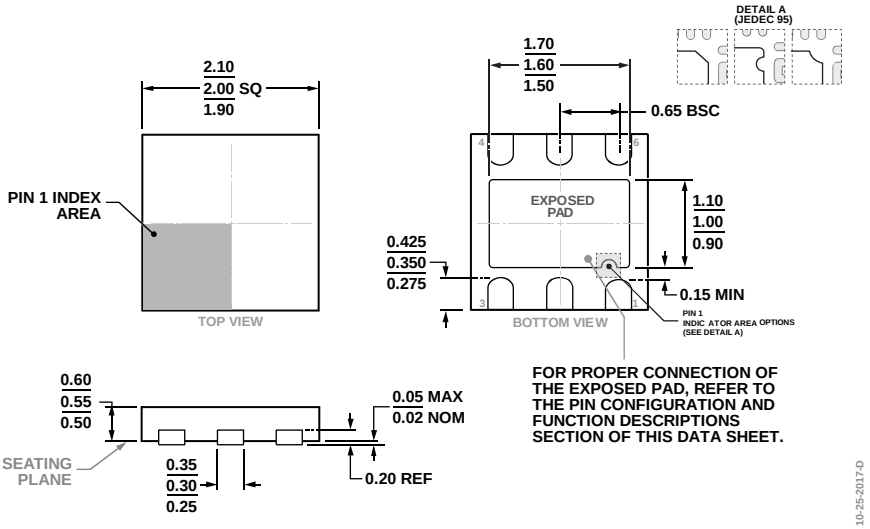
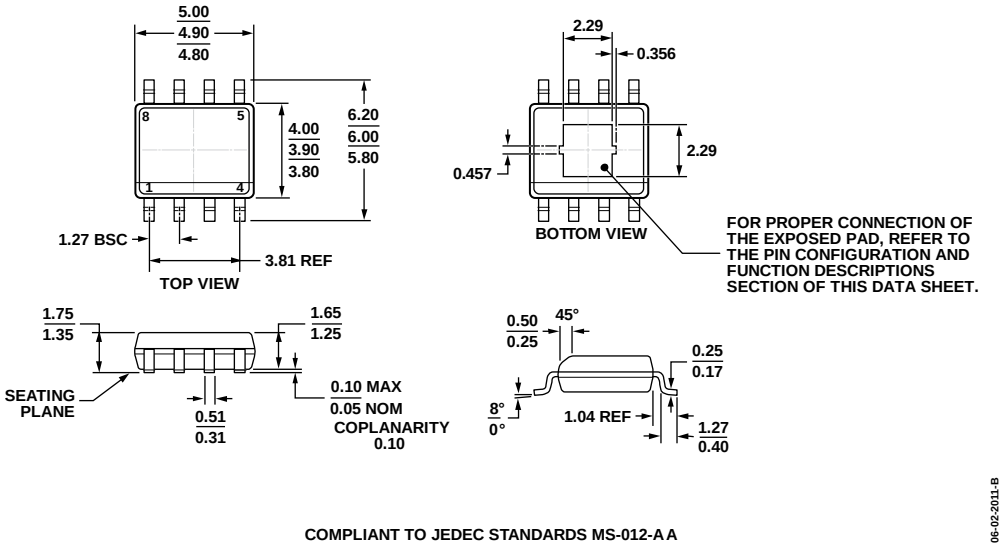
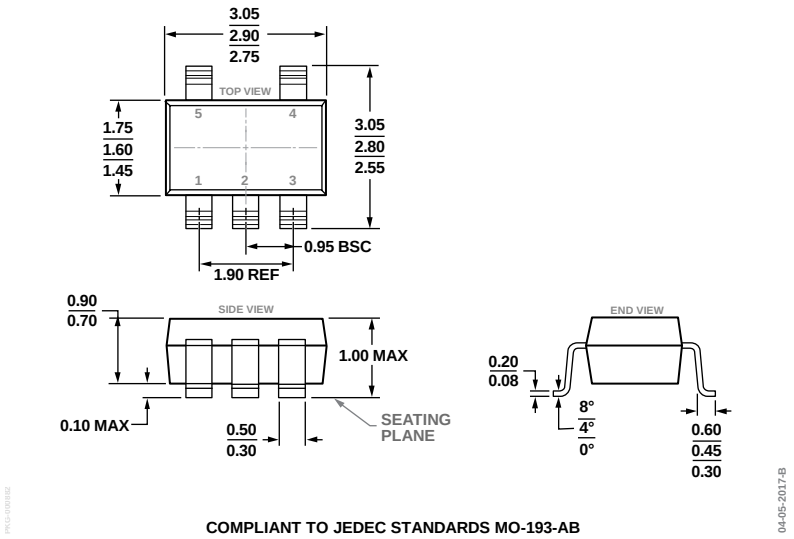


Figure 67. 6-Lead Lead Frame Chip Scale Package [LFCSP]
2.00 mm × 2.00 mm Body and 0.55 mm Package Height
(CP-6-3)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-A A

Figure 68. 8-Lead Standard Small Outline Package, with Exposed Pad [SOIC_N_EP]
Narrow Body
(RD-8-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-193-AB

Figure 69. 5-Lead Thin Small Outline Transistor Package [TSOT]
(UJ-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)[2, 3]	Package Description	Package Option	Marking Code
ADP7118ACPZN-R7	−40°C to +125°C	Adjustable (1.2 V)	6-Lead LFCSP	CP-6-3	LP9
ADP7118ACPZN1.8-R7	−40°C to +125°C	1.8	6-Lead LFCSP	CP-6-3	LPA
ADP7118ACPZN2.5-R7	−40°C to +125°C	2.5	6-Lead LFCSP	CP-6-3	LPB
ADP7118ACPZN3.3-R7	−40°C to +125°C	3.3	6-Lead LFCSP	CP-6-3	LPC
ADP7118ACPZN5.0-R7	−40°C to +125°C	5	6-Lead LFCSP	CP-6-3	LPD
ADP7118ARDZ	−40°C to +125°C	Adjustable (1.2 V)	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-R7	−40°C to +125°C	Adjustable (1.2 V)	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-1.8	−40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-1.8-R7	−40°C to +125°C	1.8	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-2.5	−40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-2.5-R7	−40°C to +125°C	2.5	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-3.3	−40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-3.3-R7	−40°C to +125°C	3.3	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-5.0	−40°C to +125°C	5	8-Lead SOIC_N_EP	RD-8-1	
ADP7118ARDZ-5.0-R7	−40°C to +125°C	5	8-Lead SOIC_N_EP	RD-8-1	
ADP7118AUJZ-R2	−40°C to +125°C	Adjustable (1.2 V)	5-Lead TSOT	UJ-5	LP9
ADP7118AUJZ-R7	−40°C to +125°C	Adjustable (1.2 V)	5-Lead TSOT	UJ-5	LP9
ADP7118AUJZ-1.8-R7	−40°C to +125°C	1.8	5-Lead TSOT	UJ-5	LPA
ADP7118AUJZ-2.5-R7	−40°C to +125°C	2.5	5-Lead TSOT	UJ-5	LPB
ADP7118AUJZ-3.3-R7	−40°C to +125°C	3.3	5-Lead TSOT	UJ-5	LPC
ADP7118AUJZ-4.5-R7	−40°C to +125°C	4.5	5-Lead TSOT	UJ-5	LUU
ADP7118AUJZ-5.0-R7	−40°C to +125°C	5	5-Lead TSOT	UJ-5	LPD
ADP7118UJ-EVALZ			TSOT Evaluation Board		
ADP7118CP-EVALZ			LFCSP Evaluation Board		
ADP7118RD-EVALZ			SOIC Evaluation Board		

[1] Z = RoHS compliant part.
[2] For additional voltage options, contact a local Analog Devices, Inc., sales or distribution representative.
[3] The evaluation boards are preconfigured with an adjustable ADP7118.

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