Features

- Fast Read Access Time – 70 ns
- Automatic Page Write Operation
  - Internal Address and Data Latches for 64 Bytes
  - Internal Control Timer
- Fast Write Cycle Times
  - Page Write Cycle Time: 3 ms or 10 ms Maximum
  - 1 to 64-byte Page Write Operation
- Low Power Dissipation
  - 80 mA Active Current
  - 3 mA Standby Current
- Hardware and Software Data Protection
- $\overline{\text{DATA}}$ Polling for End of Write Detection
- High Reliability CMOS Technology
  - Endurance: 10^4 or 10^5 Cycles
  - Data Retention: 10 Years
- Single 5V ±10% Supply
- CMOS and TTL Compatible Inputs and Outputs
- JEDEC Approved Byte-wide Pinout
- Full Military and Industrial Temperature Ranges
- Green (Pb/Halide-free) Packaging Option

256K (32K x 8) High-speed Parallel EEPROM

AT28HC256

1. Description

The AT28HC256 is a high-performance electrically erasable and programmable read-only memory. Its 256K of memory is organized as 32,768 words by 8 bits. Manufactured with Atmel's advanced nonvolatile CMOS technology, the AT28HC256 offers access times to 70 ns with power dissipation of just 440 mW. When the AT28HC256 is deselected, the standby current is less than 5 mA.

The AT28HC256 is accessed like a Static RAM for the read or write cycle without the need for external components. The device contains a 64-byte page register to allow writing of up to 64 bytes simultaneously. During a write cycle, the address and 1 to 64 bytes of data are internally latched, freeing the addresses and data bus for other operations. Following the initiation of a write cycle, the device will automatically write the latched data using an internal control timer. The end of a write cycle can be detected by $\overline{\text{DATA}}$ Polling of I/O7. Once the end of a write cycle has been detected a new access for a read or write can begin.

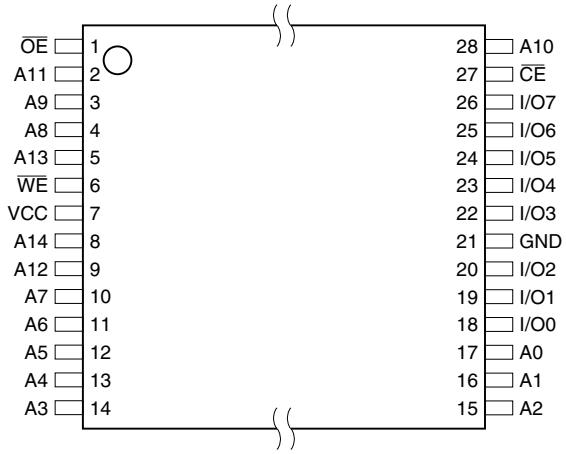
Atmel's 28HC256 has additional features to ensure high quality and manufacturability. The device utilizes internal error correction for extended endurance and improved data retention characteristics. An optional software data protection mechanism is available to guard against inadvertent writes. The device also includes an extra 64 bytes of EEPROM for device identification or tracking.

0007N–PEEPR–9/09

2. Pin Configurations

Pin Name	Function
A0 - A14	Addresses
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
NC	No Connect
DC	Don't Connect

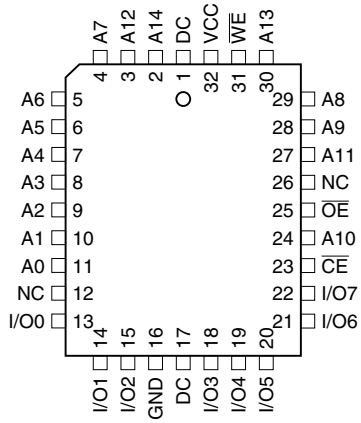
2.1 28-lead TSOP Top View



2.2 28-lead PGA Top View

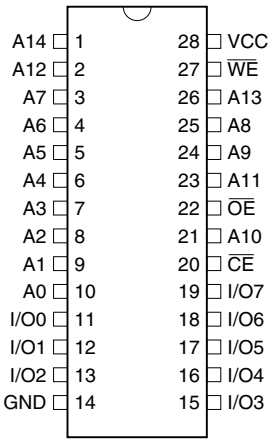
4 A6	3 A7	1 A14	27 $\overline{WE}$	26 A13
5 A5	2 A12	28 VCC	24 A9	25 A8
7 A3	6 A4		22 $\overline{OE}$	23 A11
9 A1	8 A2		20 $\overline{CE}$	21 A10
11 I/O0	10 A0	14 GND	16 I/O4	19 I/O7
12 I/O1	13 I/O2	15 I/O3	17 I/O5	18 I/O6

2.3 32-pad LCC, 32-lead PLCC Top View

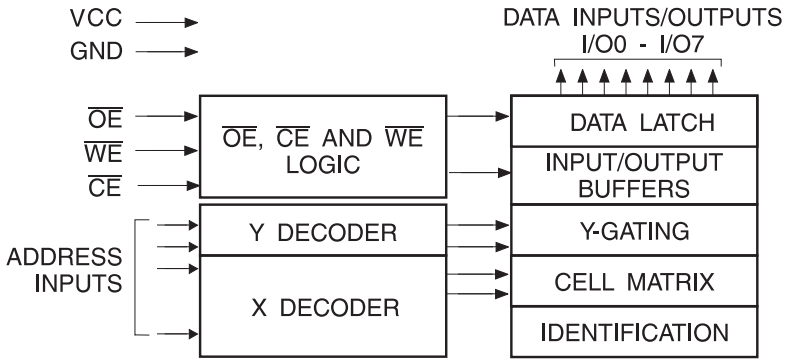


Note: PLCC package pins 1 and 17 are Don't Connect.

2.4 28-lead Cerdip/Flatpack/SOIC – Top View



3. Block Diagram



4. Device Operation

4.1 Read

The AT28HC256 is accessed like a Static RAM. When $\overline{CE}$ and $\overline{OE}$ are low and $\overline{WE}$ is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in the high impedance state when either $\overline{CE}$ or $\overline{OE}$ is high. This dual-line control gives designers flexibility in preventing bus contention in their system.

4.2 Byte Write

A low pulse on the $\overline{WE}$ or $\overline{CE}$ input with $\overline{CE}$ or $\overline{WE}$ low (respectively) and $\overline{OE}$ high initiates a write cycle. The address is latched on the falling edge of $\overline{CE}$ or $\overline{WE}$, whichever occurs last. The data is latched by the first rising edge of $\overline{CE}$ or $\overline{WE}$. Once a byte write has been started it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of t_{WC}, a read operation will effectively be a polling operation.

4.3 Page Write

The page write operation of the AT28HC256 allows 1 to 64 bytes of data to be written into the device during a single internal programming period. A page write operation is initiated in the same manner as a byte write; the first byte written can then be followed by 1 to 63 additional bytes. Each successive byte must be written within 150 µs (t_{BLC}) of the previous byte. If the t_{BLC} limit is exceeded the AT28C256 will cease accepting data and commence the internal programming operation. All bytes during a page write operation must reside on the same page as defined by the state of the A6 - A14 inputs. That is, for each $\overline{WE}$ high to low transition during the page write operation, A6 - A14 must be the same.

The A0 to A5 inputs are used to specify which bytes within the page are to be written. The bytes may be loaded in any order and may be altered within the same load period. Only bytes which are specified for writing will be written; unnecessary cycling of other bytes within the page does not occur.

4.4 $\overline{DATA}$ Polling

The AT28HC256 features $\overline{DATA}$ Polling to indicate the end of a write cycle. During a byte or page write cycle an attempted read of the last byte written will result in the complement of the written data to be presented on I/O7. Once the write cycle has been completed, true data is valid on all outputs, and the next write cycle may begin. $\overline{DATA}$ Polling may begin at anytime during the write cycle.

4.5 Toggle Bit

In addition to $\overline{\text{DATA}}$ Polling the AT28HC256 provides another method for determining the end of a write cycle. During the write operation, successive attempts to read data from the device will result in I/O6 toggling between one and zero. Once the write has completed, I/O6 will stop toggling and valid data will be read. Testing the toggle bit may begin at any time during the write cycle.

4.6 Data Protection

If precautions are not taken, inadvertent writes to any 5-volt-only nonvolatile memory may occur during transition of the host system power supply. Atmel® has incorporated both hardware and software features that will protect the memory against inadvertent writes.

4.6.1 Hardware Protection

Hardware features protect against inadvertent writes to the AT28HC256 in the following ways: (a) V_{CC} sense – if V_{CC} is below 3.8V (typical) the write function is inhibited; (b) V_{CC} power-on delay – once V_{CC} has reached 3.8V the device will automatically time out 5 ms typical) before allowing a write; (c) write inhibit – holding any one of $\overline{\text{OE}}$ low, $\overline{\text{CE}}$ high or $\overline{\text{WE}}$ high inhibits write cycles; and (d) noise filter – pulses of less than 15 ns (typical) on the $\overline{\text{WE}}$ or $\overline{\text{CE}}$ inputs will not initiate a write cycle.

4.6.2 Software Data Protection

A software controlled data protection feature has been implemented on the AT28HC256. When enabled, the software data protection (SDP), will prevent inadvertent writes. The SDP feature may be enabled or disabled by the user; the AT28HC256 is shipped from Atmel with SDP disabled.

SDP is enabled by the host system issuing a series of three write commands; three specific bytes of data are written to three specific addresses (refer to “Software Data Protection” algorithm). After writing the 3-byte command sequence and after t_{WC} the entire AT28HC256 will be protected against inadvertent write operations. It should be noted, that once protected the host may still perform a byte or page write to the AT28HC256. This is done by preceding the data to be written by the same 3-byte command sequence.

Once set, SDP will remain active unless the disable command sequence is issued. Power transitions do not disable SDP and SDP will protect the AT28HC256 during power-up and power-down conditions. All command sequences must conform to the page write timing specifications. It should also be noted that the data in the enable and disable command sequences is not written to the device and the memory addresses used in the sequence may be written with data in either a byte or page write operation.

After setting SDP, any attempt to write to the device without the three byte command sequence will start the internal write timers. No data will be written to the device; however, for the duration of t_{WC}, read operations will effectively be polling operations.

4.7 Device Identification

An extra 64 bytes of EEPROM memory are available to the user for device identification. By raising A9 to 12V ±0.5V and using address locations 7FC0H to 7FFFH the additional bytes may be written to or read from in the same manner as the regular memory array.

4.8 Optional Chip Erase Mode

The entire device can be erased using a 6-byte software code. Please see “Software Chip Erase” application note for details.

5. DC and AC Operating Range

		AT28HC256-70	AT28HC256-90	AT28HC256-12
Operating Temperature (Case)	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.		-55°C - 125°C	-55°C - 125°C
V_{CC} Power Supply		5V ±10%	5V ±10%	5V ±10%

6. Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}
Write[2]	V_{IL}	V_{IH}	V_{IL}	D_{IN}
Standby/Write Inhibit	V_{IH}	X[1]	X	High Z
Write Inhibit	X	X	V_{IH}	
Write Inhibit	X	V_{IL}	X	
Output Disable	X	V_{IH}	X	High Z
Chip Erase	V_{IL}	V_H[3]	V_{IL}	High Z

Notes: 1. X can be V_{IL} or V_{IH}.
2. Refer to AC programming waveforms.
3. V_H = 12.0V ± 0.5V.

7. Absolute Maximum Ratings*

Temperature under Bias ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C

All Input Voltages
(including NC Pins)
with Respect to Ground .....-0.6V to +6.25V

All Output Voltages
with Respect to Ground .....-0.6V to V_{CC} + 0.6V

Voltage on $\overline{OE}$ and A9
with Respect to Ground .....-0.6V to +13.5V

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

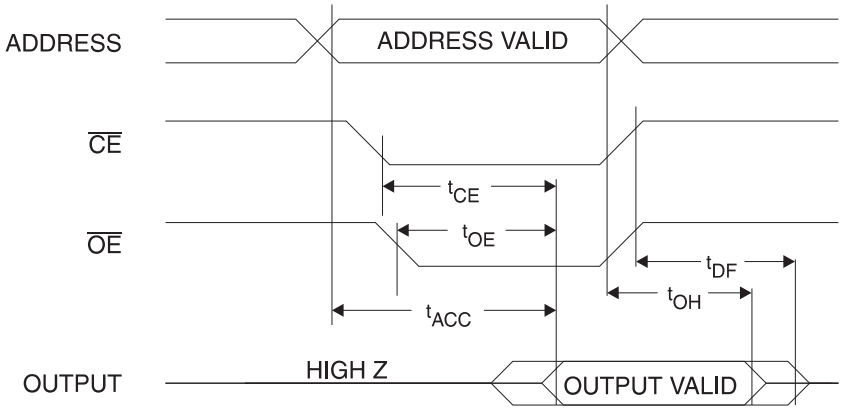
8. DC Characteristics

Symbol	Parameter	Condition		Min	Max	Units
I_{LI}	Input Load Current	V_{IN} = 0V to V_{CC} + 1V			10	µA
I_{LO}	Output Leakage Current	$V_{I/O}$ = 0V to V_{CC}			10	µA
I_{SB1}	V_{CC} Standby Current TTL	$\overline{CE}$ = 2.0V to V_{CC}	AT28HC256-90, -12		3	mA
			AT28HC256-70		60	mA
I_{SB2}	V_{CC} Standby Current CMOS	$\overline{CE}$ = V_{CC} - 0.3V to V_{CC}	AT28HC256-90, -12		300	µA
I_{CC}	V_{CC} Active Current	f = 5 MHz; I_{OUT} = 0 mA			80	mA
V_{IL}	Input Low Voltage				0.8	V
V_{IH}	Input High Voltage			2.0		V
V_{OL}	Output Low Voltage	I_{OL} = 6.0 mA			0.45	V
V_{OH}	Output High Voltage	I_{OH} = -4 mA		2.4		V

9. AC Read Characteristics

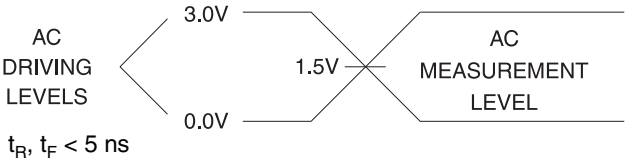
Symbol	Parameter	AT28HC256-70		AT28C256-90		AT28HC256-12		Units
		Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay		70		90		120	ns
t_{CE}[1]	$\overline{CE}$ to Output Delay		70		90		120	ns
t_{OE}[2]	$\overline{OE}$ to Output Delay	0	35	0	40	0	50	ns
t_{DF}[3][4]	$\overline{CE}$ or $\overline{OE}$ to Output Float	0	35	0	40	0	50	ns
t_{OH}	Output Hold from $\overline{OE}$, $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

10. AC Read Waveforms[1][2][3][4]

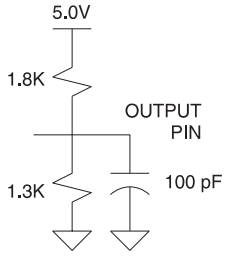


Notes:
1. $\overline{CE}$ may be delayed up to $t_{ACC} - t_{CE}$ after the address transition without impact on t_{ACC}.
2. $\overline{OE}$ may be delayed up to $t_{CE} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{CE} or by $t_{ACC} - t_{OE}$ after an address change without impact on t_{ACC}.
3. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first (C_L = 5 pF).
4. This parameter is characterized and is not 100% tested.

11. Input Test Waveforms and Measurement Level



12. Output Test Load



13. Pin Capacitance

f = 1 MHz, T = 25°C[1]

Symbol	Typ	Max	Units	Conditions
C_{IN}	4	6	pF	V_{IN} = 0V
C_{OUT}	8	12	pF	V_{OUT} = 0V

Note: 1. This parameter is characterized and is not 100% tested.

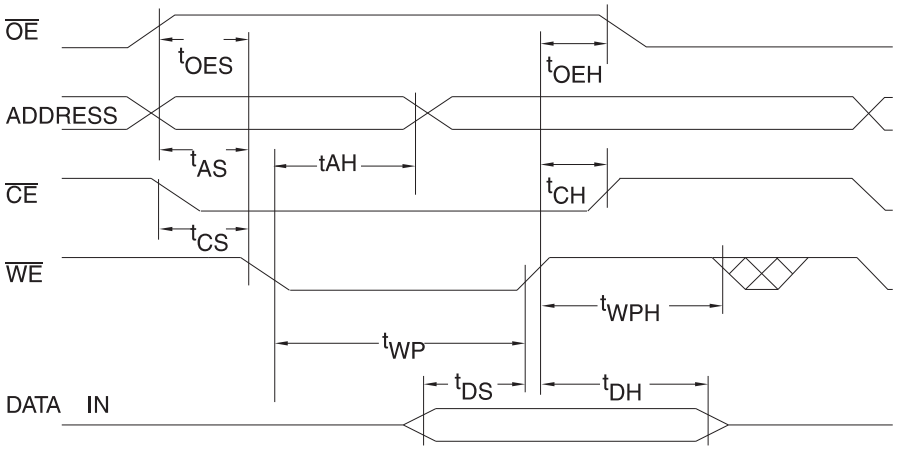
14. AC Write Characteristics

Symbol	Parameter	Min	Max	Units
t_{AS}, t_{OES}	Address, $\overline{OE}$ Setup Time	0		ns
t_{AH}	Address Hold Time	50		ns
t_{CS}	Chip Select Setup Time	0		ns
t_{CH}	Chip Select Hold Time	0		ns
t_{WP}	Write Pulse Width ($\overline{WE}$ or $\overline{CE}$)	100		ns
t_{DS}	Data Setup Time	50		ns
t_{DH}, t_{OEH}	Data, $\overline{OE}$ Hold Time	0		ns
t_{DV}	Time to Data Valid	NR[1]		

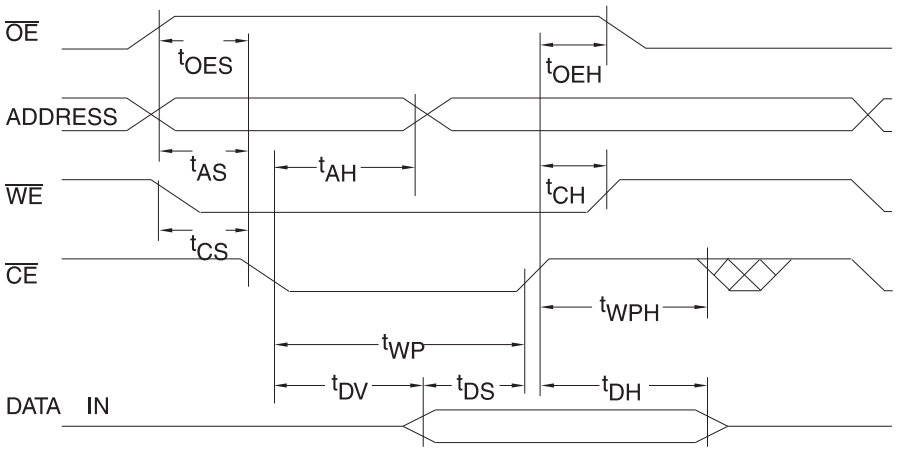
Note: 1. NR = No Restriction.

15. AC Write Waveforms

15.1 $\overline{WE}$ Controlled



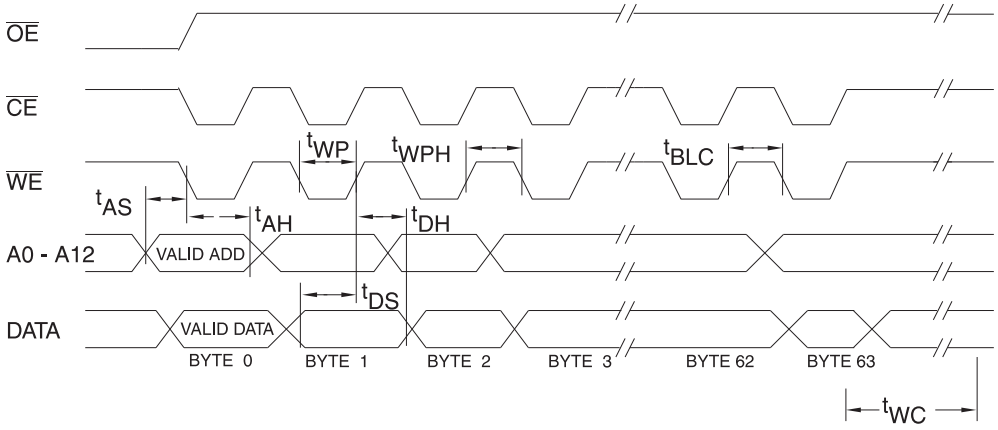
15.2 $\overline{CE}$ Controlled



16. Page Mode Write Characteristics

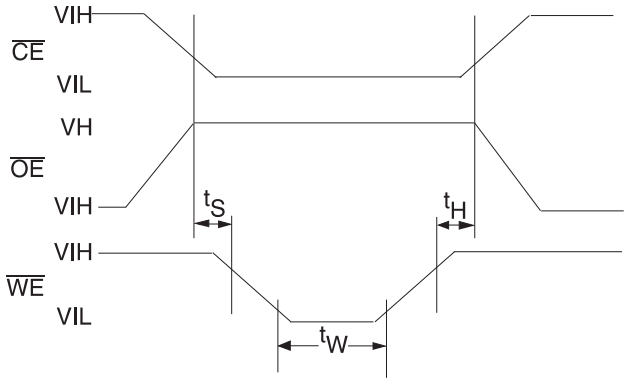
Symbol	Parameter		Min	Typ	Max	Units
t_{WC}	Write Cycle Time (option available)	AT28HC256		5	10	ms
		AT28HC256F		2	3	ms
t_{AS}	Address Setup Time		0			ns
t_{AH}	Address Hold Time		50			ns
t_{DS}	Data Setup Time		50			ns
t_{DH}	Data Hold Time		0			ns
t_{WP}	Write Pulse Width		100			ns
t_{BLC}	Byte Load Cycle Time				150	µs
t_{WPH}	Write Pulse Width High		50			ns

17. Page Mode Write Waveforms(1)(2)



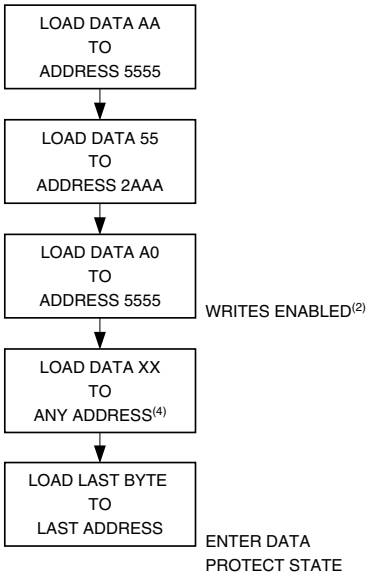
Notes: 1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$).
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

18. Chip Erase Waveforms



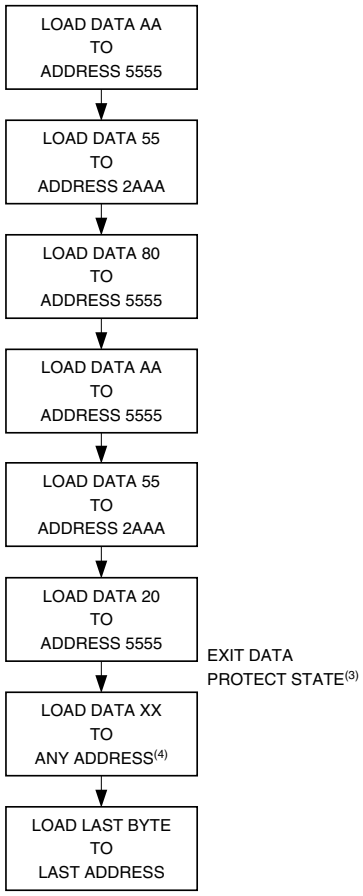
$t_S = t_H = 5$ µsec (min.)
$t_W = 10$ msec (min.)
$V_H = 12.0V \pm 0.5V$

19. Software Data Protection Enable Algorithm[1]

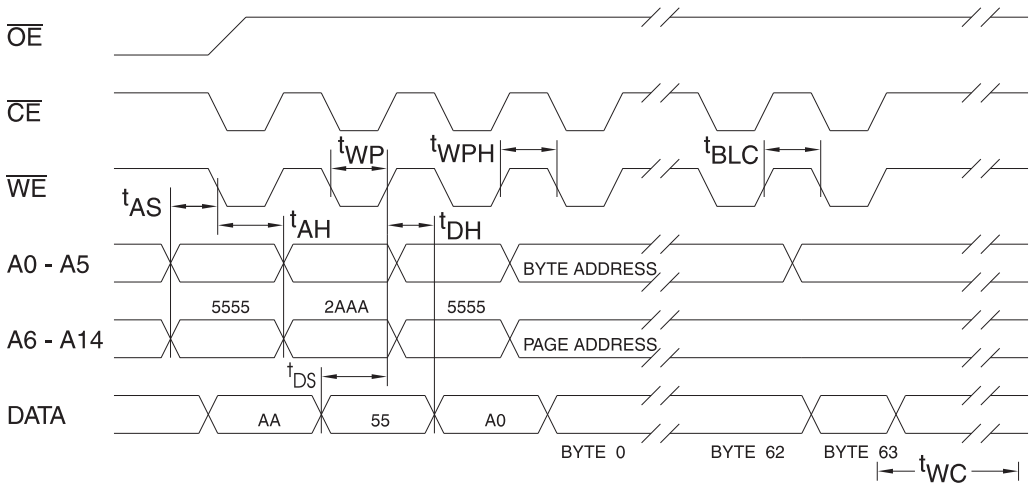


Notes:
1. Data Format: I/O7 - I/O0 (Hex);
   Address Format: A14 - A0 (Hex).
2. Write Protect state will be activated at end of write even if no other data is loaded.
3. Write Protect state will be deactivated at end of write period even if no other data is loaded.
4. 1 to 64 bytes of data are loaded.

20. Software Data Protection Disable Algorithm[1]



21. Software Protected Write Cycle Waveforms[1][2]



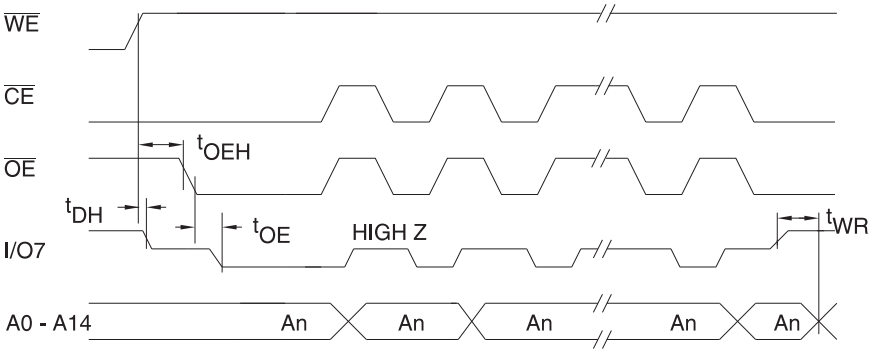
Notes:
1. A6 through A14 must specify the same page address during each high to low transition of $\overline{WE}$ (or $\overline{CE}$) after the software code has been entered.
2. $\overline{OE}$ must be high only when $\overline{WE}$ and $\overline{CE}$ are both low.

22. Data Polling Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	0			ns
t_{OEH}	$\overline{OE}$ Hold Time	0			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See "AC Read Characteristics" on page 6.

23. Data Polling Waveforms

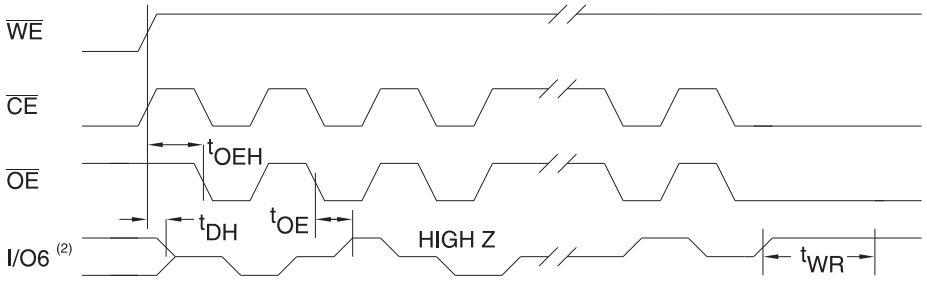


24. Toggle Bit Characteristics[1]

Symbol	Parameter	Min	Typ	Max	Units
t_{DH}	Data Hold Time	10			ns
t_{OEH}	$\overline{OE}$ Hold Time	10			ns
t_{OE}	$\overline{OE}$ to Output Delay[2]				ns
t_{OEHP}	$\overline{OE}$ High Pulse	150			ns
t_{WR}	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.
2. See "AC Read Characteristics" on page 6.

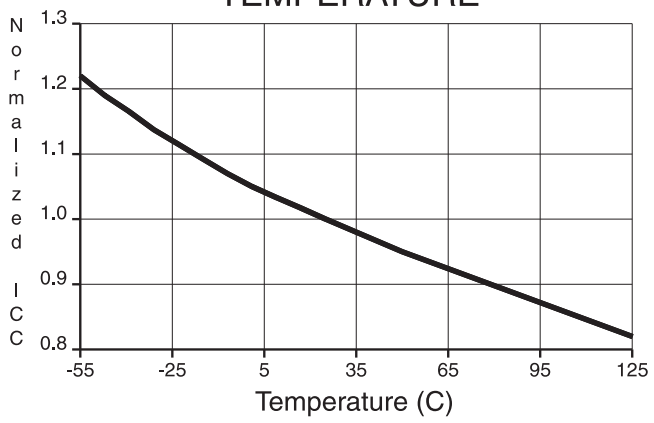
25. Toggle Bit Waveforms



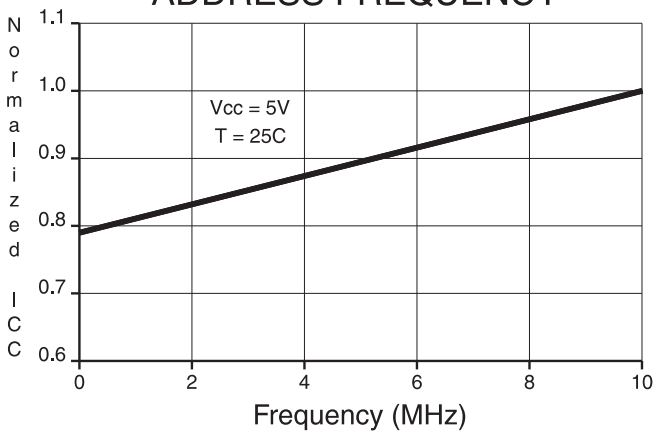
Notes: 1. Toggling either $\overline{OE}$ or $\overline{CE}$ or both $\overline{OE}$ and $\overline{CE}$ will operate toggle bit.
2. Beginning and ending state of I/O6 will vary.
3. Any address location may be used but the address should not vary.

26. Normalized I_{CC} Graphs

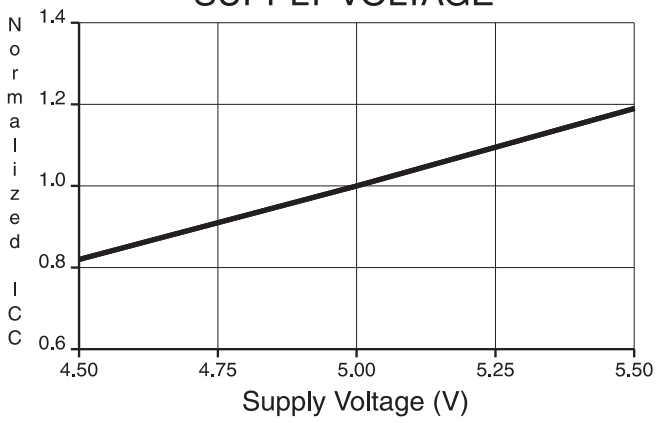
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



27. Ordering Information

27.1 Military Dual Marked Package

27.1.1 AT28HC256

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256-90DM/883 5962-88634 03 XX	28D6	Military/883C Class B, Fully Compliant (-55° C to 125° C)
			AT28HC256-90FM/883 5962-88634 03 ZX	28F	
			AT28HC256-90LM/883 5962-88634 03 YX	32L	
			AT28HC256-90UM/883 5962-88634 03 UX	28U	
120	80	0.3	AT28HC256-12DM/883 5962-88634 01 XX	28D6	
			AT28HC256-12FM/883 5962-88634 01 ZX	28F	
			AT28HC256-12LM/883 5962-88634 01 YX	32L	
			AT28HC256-12UM/883 5962-88634 01 UX	28U	

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

27.1.2 AT28HC256E[1]

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256E-90DM/883	28D6	Military/883C Class B, Fully Compliant (-55° C to 125° C)
			AT28HC256E-90FM/883	28F	
			AT28HC256E-90LM/883	32L	
			AT28HC256E-90UM/883	28U	
120	80	0.3	AT28HC256E-12DM/883	28D6	
			AT28HC256E-12FM/883	28F	
			AT28HC256E-12LM/883	32L	
			AT28HC256E-12UM/883	28U	

Note: 1. No dual marking for this device.

27.1.3 AT28HC256F

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256F-90DM/883 5962-88634 04 XX	28D6	Military/883C Class B, Fully Compliant (-55° C to 125° C)
			AT28HC256F-90FM/883 5962-88634 04 ZX	28F	
			AT28HC256F-90LM/883 5962-88634 04 YX	32L	
			AT28HC256F-90UM/883 5962-88634 04 UX	28U	
120	80	0.3	AT28HC256F-12DM/883 5962-88634 02 XX	28D6	
			AT28HC256F-12FM/883 5962-88634 02 ZX	28F	
			AT28HC256F-12LM/883 5962-88634 02 YX	32L	
			AT28HC256F-12UM/883 5962-88634 02 UX	28U	

Package Type	
28D6	28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)
28F	28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (Flatpack)
32L	32-pad, Non-windowed, Ceramic Leadless Chip Carrier (LCC)
28U	28-pin, Ceramic Pin Grid Array (PGA)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

27.2 Industrial Green Package Option (Pb/Halide-free)

27.2.1 AT28HC256

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
70	80	0.3	AT28HC256-70JU	32J	Industrial (-40° C to 85° C)
			AT28HC256-70SU	28S	
			AT28HC256-70TU	28T	
90	80	0.3	AT28HC256-90JU	32J	
			AT28HC256-90SU	28S	
			AT28HC256-90TU	28T	
120	80	0.3	AT28HC256-12JU	32J	
			AT28HC256-12SU	28S	
			AT28HC256-12TU	28T	

27.2.2 AT28HC256E

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256E-90JU	32J	Industrial (-40° C to 85° C)
			AT28HC256E-90SU	28S	
			AT28HC256E-90TU	28T	
120	80	0.3	AT28HC256E-12JU	32J	
			AT28HC256E-12SU	28S	
			AT28HC256E-12TU	28T	

27.2.3 AT28HC256F

t_{ACC} (ns)	I_{CC} (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
90	80	0.3	AT28HC256F-90JU	32J	Industrial (-40° C to 85° C)
			AT28HC256F-90SU	28S	
			AT28HC256F-90TU	28T	

Package Type	
32J	32-lead, Plastic J-leaded Chip Carrier (PLCC)
28S	28-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC)
28T	28-lead, Plastic Thin Small Outline Package (TSOP)
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 10 ms
E	High Endurance Option: Endurance = 100K Write Cycles
F	Fast Write Option: Write Time = 3 ms

27.3 Ordering Information Note

Previous datasheets included the low power suffixes L, LE and LF on the AT28HC256 for 120 ns and 90 ns speeds. The low power parameters are now standard; therefore, the L, LE and LF suffixes are no longer required.

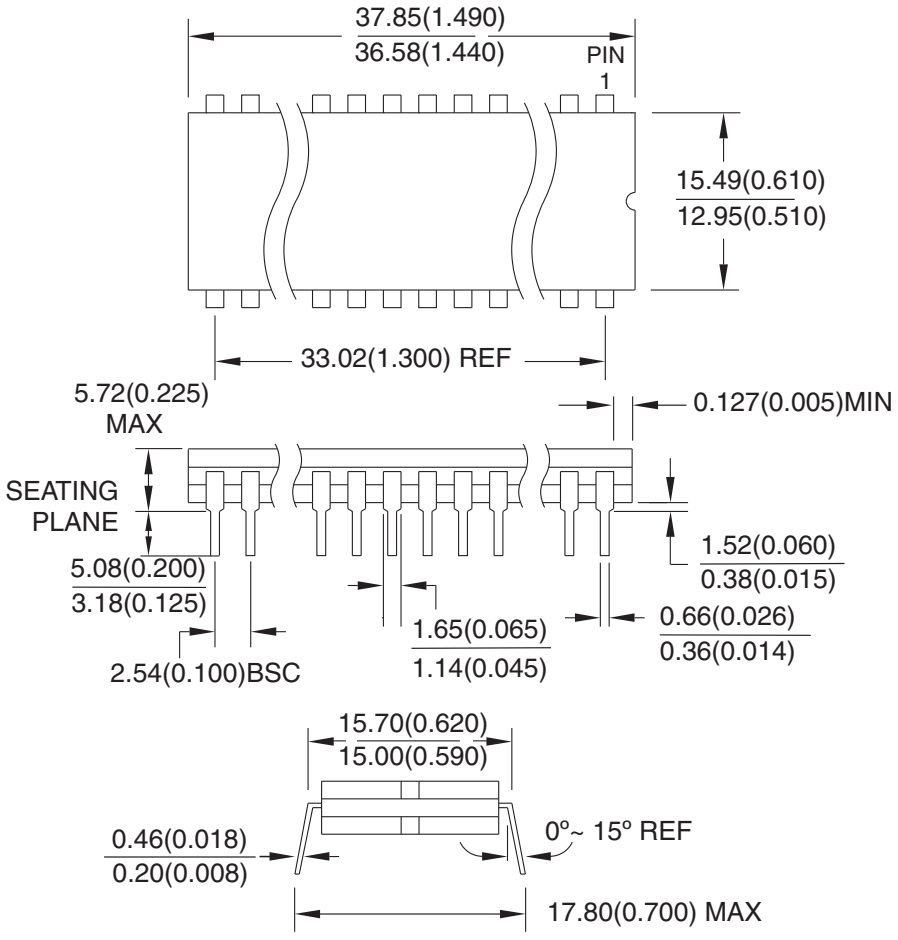
27.4 Die Products

Contact Atmel Sales for die sales options.

28. Packaging Information

28.1 28D6 – Cerdip

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 D-10 Config A (Glass Sealed)

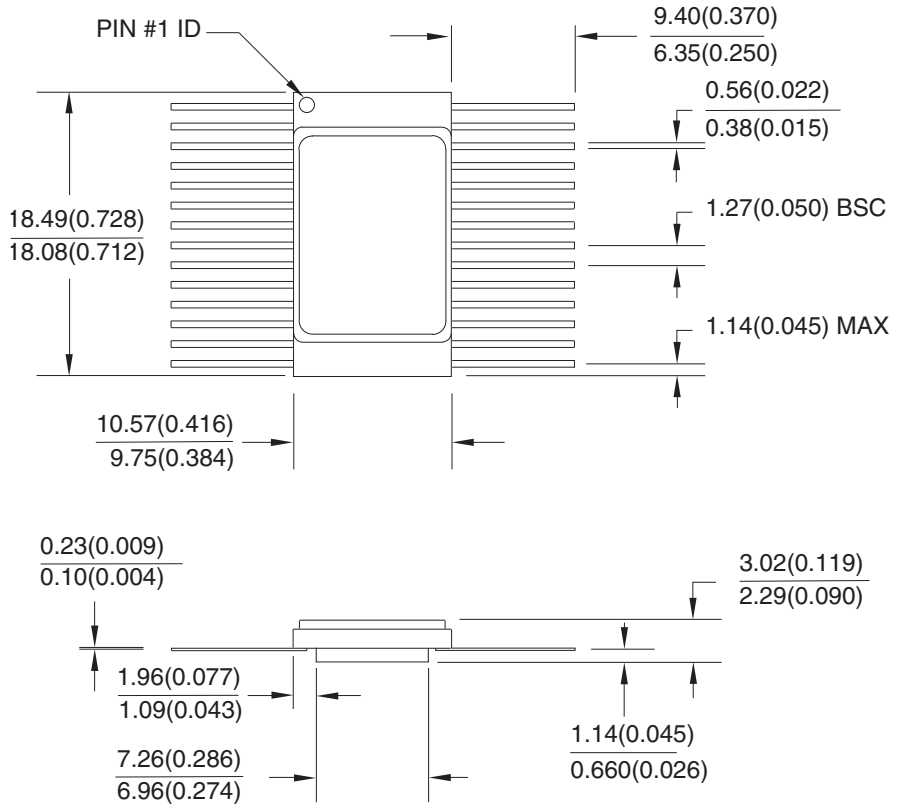


10/23/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28D6**, 28-lead, 0.600" Wide, Non-windowed, Ceramic Dual Inline Package (Cerdip)	28D6	B

28.2 28F – Flatpack

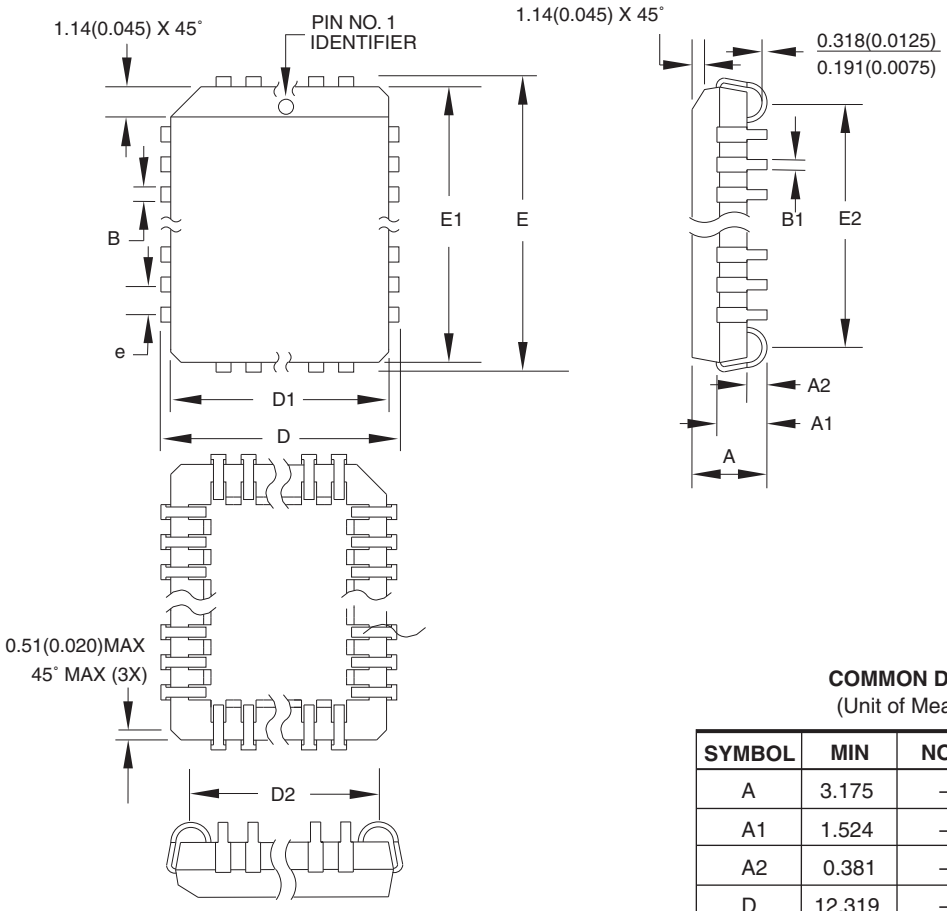
Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 F-12 Config B



10/21/03

2325 Orchard Parkway San Jose, CA 95131	TITLE **28F**, 28-lead, Non-windowed, Ceramic Bottom-brazed Flat Package (FlatPack)	DRAWING NO. 28F	REV. B

28.3 32J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	3.175	–	3.556	
A1	1.524	–	2.413	
A2	0.381	–	–	
D	12.319	–	12.573	
D1	11.354	–	11.506	Note 2
D2	9.906	–	10.922	
E	14.859	–	15.113	
E1	13.894	–	14.046	Note 2
E2	12.471	–	13.487	
B	0.660	–	0.813	
B1	0.330	–	0.533	
e	1.270 TYP			

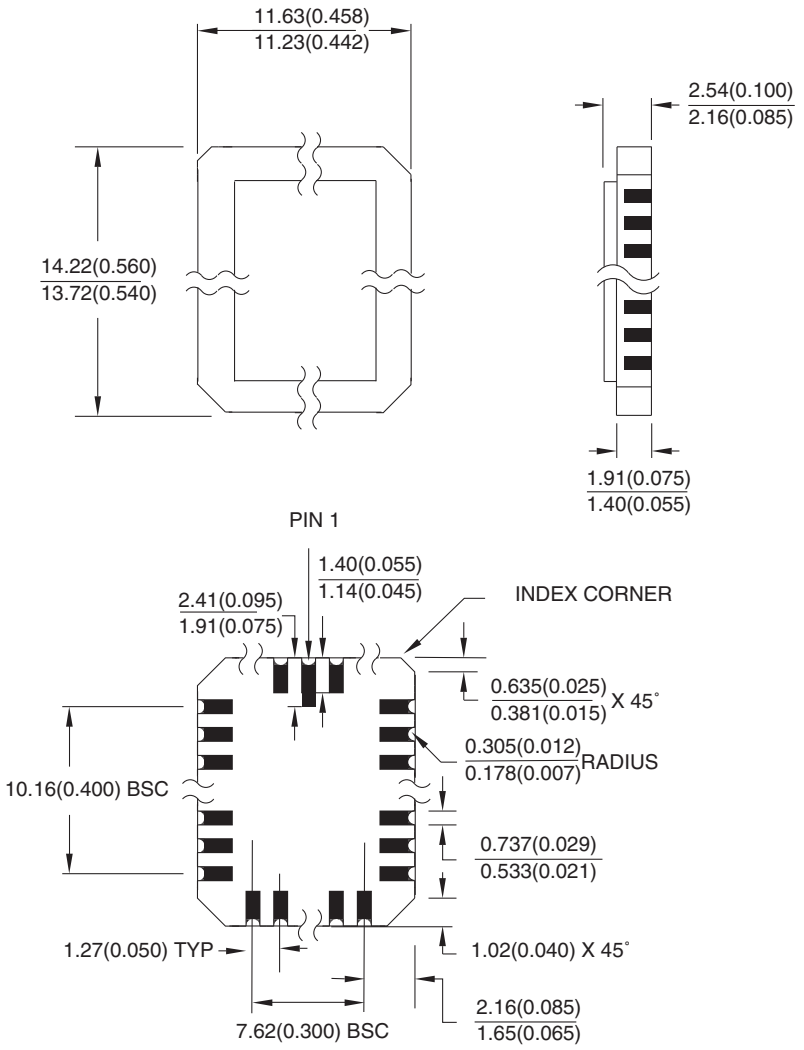
Notes:
1. This package conforms to JEDEC reference MS-016, Variation AE.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010"(0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32J**, 32-lead, Plastic J-leaded Chip Carrier (PLCC)	32J	B

28.4 32L – LCC

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.
MIL-STD 1835 C-12

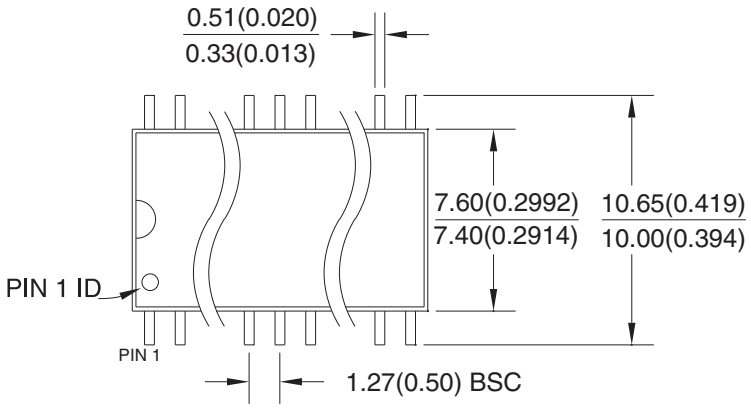


10/21/03

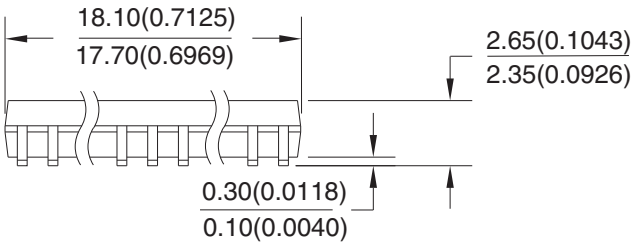
	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**32L**, 32-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC)	32L	B

28.5 28S – SOIC

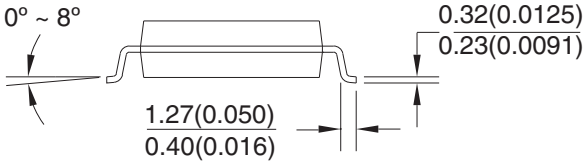
Dimensions in Millimeters and (Inches).
Controlling dimension: Millimeters.



TOP VIEW



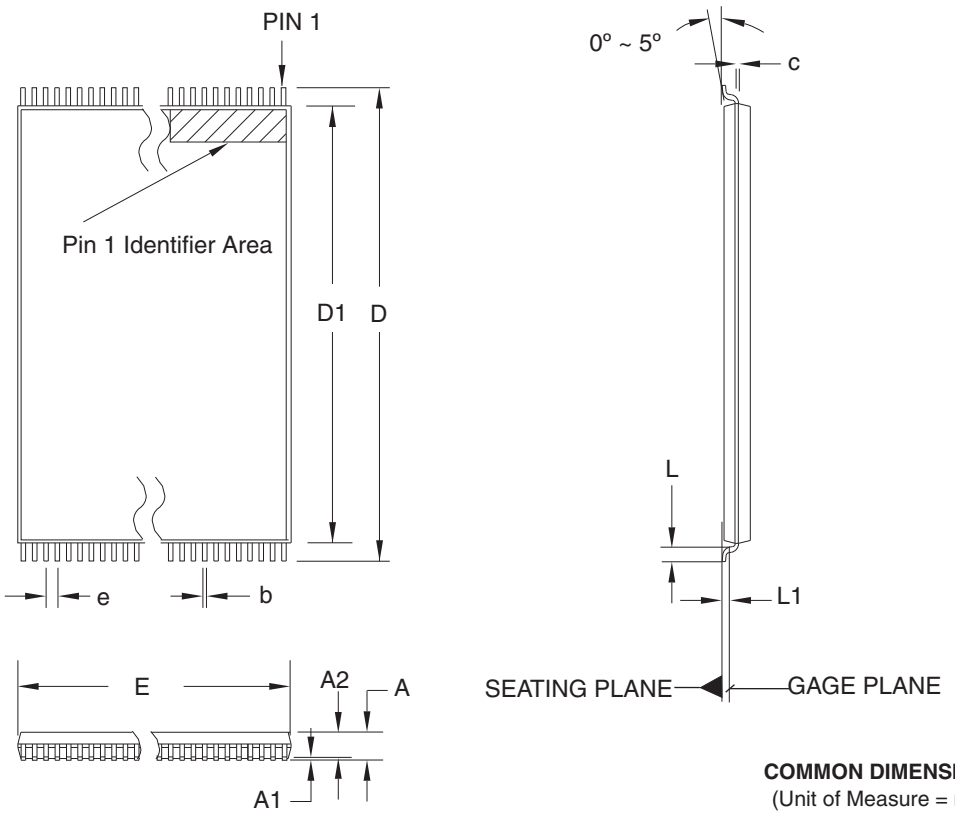
SIDE VIEWS



8/4/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28S**, 28-lead, 0.300" Body, Plastic Gull Wing Small Outline (SOIC) JEDEC Standard MS-013	28S	B

28.6 28T – TSOP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.90	1.00	1.05	
D	13.20	13.40	13.60	
D1	11.70	11.80	11.90	Note 2
E	7.90	8.00	8.10	Note 2
L	0.50	0.60	0.70	
L1	0.25 BASIC			
b	0.17	0.22	0.27	
c	0.10	–	0.21	
e	0.55 BASIC			

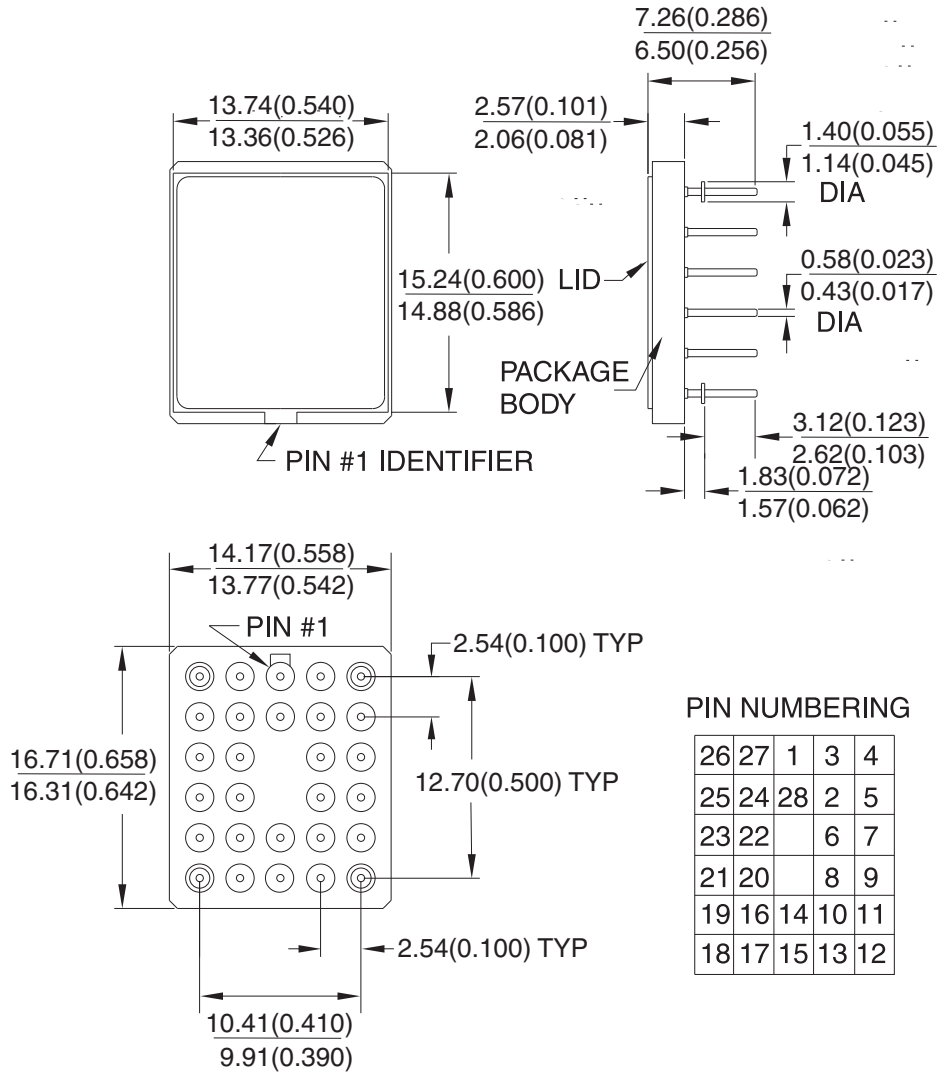
Notes:
1. This package conforms to JEDEC reference MO-183.
2. Dimensions D1 and E do not include mold protrusion. Allowable protrusion on E is 0.15 mm per side and on D1 is 0.25 mm per side.
3. Lead coplanarity is 0.10 mm maximum.

12/06/02

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28T**, 28-lead (8 x 13.4 mm) Plastic Thin Small Outline Package, Type I (TSOP)	28T	C

28.7 28U – PGA

Dimensions in Millimeters and (Inches).
Controlling dimension: Inches.



PIN NUMBERING

26	27	1	3	4
25	24	28	2	5
23	22		6	7
21	20		8	9
19	16	14	10	11
18	17	15	13	12

10/21/03

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**28U**, 28-pin, Ceramic Pin Grid Array (PGA)	28U	B

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