±16.5kV ESD Protected, 16Mbps, with Active Low Rx EN, RS-485/422 Receiver

ISL3282EMRTEP

The Intersil ISL3282EMRTEP is a ±16.5kV IEC61000 ESD protected, 3.0V to 5.5V powered, single receiver that meets both the RS-485 and RS-422 standards for balanced communication. This receiver has very low bus currents (+125µA/-100µA), so it presents a true “1/8 unit load” to the RS-485 bus. This allows up to 256 receivers on the network without violating the RS-485 specification’s 32 unit load maximum and without using repeaters.

Receiver inputs feature a “Full Fail-Safe” design, which ensures a logic high Rx output if Rx inputs are floating, shorted, or terminated but undriven.

The ISL3282EMRTEP includes an active low enable pin and is offered in the Military Temperature range (-55°C to +125°C).

A 26% smaller footprint is available with the TDFN package. This device also features a logic supply pin (V_L) that sets the V_{OH} level of the RO output (and the switching points of the RE/$\overline{RE}$ input) to be compatible with another supply voltage in mixed voltage systems.

Device Information

The specifications for an Enhanced Product (EP) device are defined in a Vendor Item Drawing (VID), which is controlled by the Defense Supply Center in Columbus (DSCC). “Hot-links” to the applicable VID and other supporting application information are provided on our website.

Applications

- Clock distribution
- High node count systems
- Space constrained systems
- Security camera networks
- Building environmental control/lighting systems
- Industrial/process control networks

Features

- Specifications per DSCC VID V62/10601-01XB
- Full military temperature electrical performance from -55°C to +125°C
- Controlled baseline with one wafer fabrication site and one assembly/test site
- Full homogeneous lot processing in wafer fab
- No combination of wafer fabrication lots in assembly
- Full traceability through assembly and test by date/trace code assignment
- Enhanced process change notification
- Enhanced obsolescence management
- Eliminates need for up-screening a COTS component
- ±16.5kV IEC61000 ESD protection on RS-485 inputs
- Class 3 ESD level on all other pins. . . . . .>5kV HBM
- Wide supply range . . . . . 3.0V to 5.5V
- Specified for +125°C operation
- Logic supply pin (V_L) eases operation in mixed supply systems
- Full fail-safe (open, short, terminated/undriven)
- True 1/8 unit load allows up to 256 devices on the bus
- High data rates. . . . . up to 16Mbps
- Low quiescent supply current. . . . . 500µA (maximum)
- Very low shutdown supply current . . . . . 20µA (maximum)
- -7V to +12V common-mode input voltage range
- Tri-statable Rx available (active low or high EN input)
- 5V tolerant logic inputs when $V_{CC} \leq 5V$

TABLE 1. SUMMARY OF FEATURES

PART NUMBER	FUNCTION	DATA RATE (Mbps)	# DEVICES ON BUS	RX ENABLE?	V_L PIN?	QUIESCENT I_{CC} (µA)	LOW POWER SHUTDOWN?	LEAD COUNT
ISL3282EMRTEP	1 Rx	16	256	ACTIVE LOW	YES	350	YES	8-TDFN

Ordering Information

PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE	PKG. DWG. #
ISL3282EMRTEP-TK	V62/10601-01XB	282	-55 to +125	1k	8 Ld TDFN	L8.2x3A

NOTES:

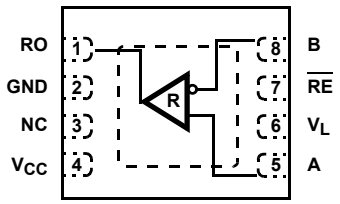
1. Please refer to TB347 for details on reel specifications.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL3282EMRTEP. For more information on MSL please see techbrief TB363.

Truth Table

RECEIVING		
INPUTS		OUTPUT
$\overline{RE}$	A - B	RO
0	≥ -0.05V	1
0	≤ -0.2V	0
0	Inputs Open/Shorted	1
1	X	High-Z*

Pin Configuration

ISL3282EMRTEP
(8 LD TDFN)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	FUNCTION
1	RO	Receiver output: If A - B ≥ -50mV, RO is high; If A - B ≤ -200mV, RO is low; RO = High if A and B are unconnected (floating) or shorted.
7	$\overline{RE}$	Receiver output enable. RO is enabled when $\overline{RE}$ is low; RO is high impedance when $\overline{RE}$ is high. If the Rx enable function is not used, connect $\overline{RE}$ directly to GND. $\overline{RE}$ is internally pulled high.
2	GND	Ground connection. This is also the potential of the TDFN thermal pad.
5	A	±16.5kV IEC61000 ESD Protected RS-485, RS-422 level, noninverting receiver input.
8	B	±16.5kV IEC61000 ESD Protected RS-485, RS-422 level, inverting receiver input.
4	V_{CC}	System power supply input (3.0V to 5.5V). On devices with a V_L pin, power-up V_{CC} first.
6	V_L	Logic-level supply, which sets the V_{IL}/V_{IH} levels for the $\overline{RE}$ pin, and sets the V_{OH} level of the RO output. Power-up this supply after V_{CC}, and keep $V_L \leq V_{CC}$.
3	NC	No Connection

Typical Operating Circuits

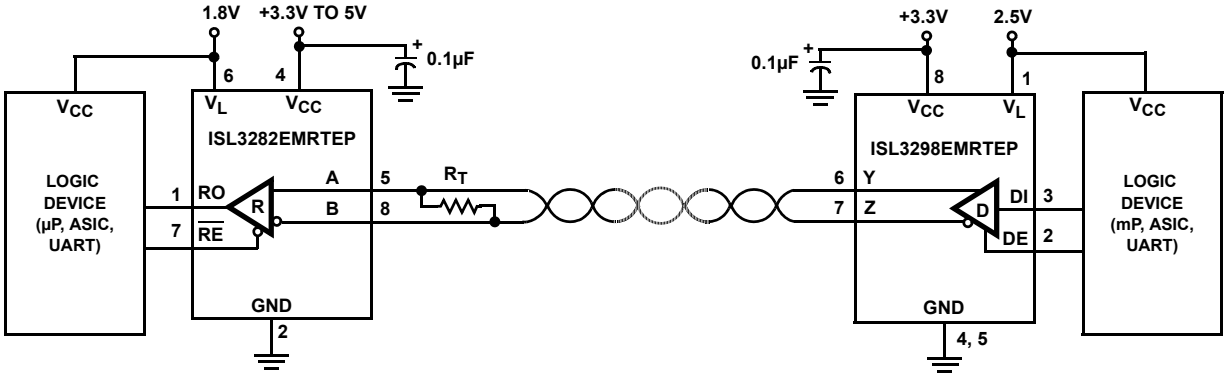


FIGURE 1. NETWORK WITH V_L PIN FOR INTERFACE TO LOWER VOLTAGE LOGIC DEVICES

Test Circuits and Waveforms

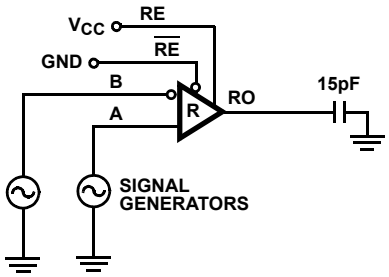


FIGURE 2A. TEST CIRCUIT

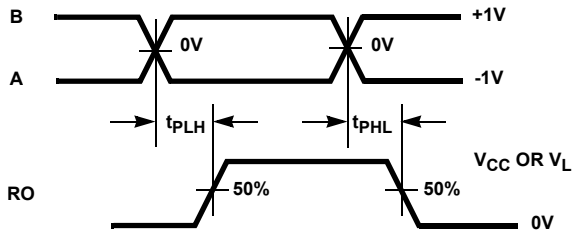
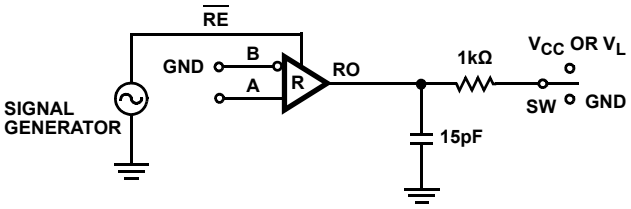


FIGURE 2B. MEASUREMENT POINTS

FIGURE 2. RECEIVER PROPAGATION DELAY AND DATA RATE



PARAMETER	A (V)	SW
t_{HZ}	+1.5	GND
t_{LZ}	-1.5	V_{CC} OR V_L
t_{ZH}	+1.5	GND
t_{ZL}	-1.5	V_{CC} OR V_L

FIGURE 3A. TEST CIRCUIT

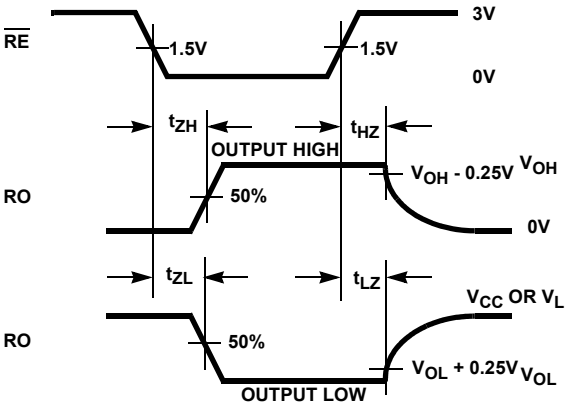


FIGURE 3B. MEASUREMENT POINTS

FIGURE 3. RECEIVER ENABLE AND DISABLE TIMES

Application Information

RS-485 and RS-422 are differential (balanced) data transmission standards for use in long haul or noisy environments. RS-422 is a subset of RS-485, so RS-485 transceivers are also RS-422 compliant. RS-422 is a point-to-multipoint (multidrop) standard, which allows only one driver and up to 10 (assuming one unit load devices) receivers on each bus. RS-485 is a true multipoint standard, which allows up to 32 one unit load devices (any combination of drivers and receivers) on each bus.

Another important advantage of RS-485 is the extended Common-Mode Range (CMR), which specifies that the driver outputs and receiver inputs withstand signals that range from +12V to -7V. RS-422 and RS-485 are intended for runs as long as 4000', so the wide CMR is necessary to handle ground potential differences, as well as voltages induced in the cable by external fields.

Receiver Features

This device utilizes a differential input receiver for maximum noise immunity and common-mode rejection. Input sensitivity is better than ±200mV, as required by the RS-422 and RS-485 specifications.

Receiver input resistance of 96kΩ surpasses the RS-422 specification of 4kΩ and is eight times the RS-485 "Unit Load (UL)" requirement of 12kΩ minimum. Thus, these products are known as "one-eighth UL" transceivers and there can be up to 256 of these devices on a network while still complying with the RS-485 loading specification.

Receiver inputs function with common-mode voltages as great as +9V/-7V outside the power supplies (i.e., +12V and -7V), making them ideal for long networks where induced voltages, and ground potential differences are realistic concerns.

The ISL3282EMRTEP includes a "full fail-safe" function that guarantees a high level receiver output if the receiver inputs are unconnected (floating), shorted together, or connected to a terminated, however, undriven bus. Fail-safe with shorted inputs is achieved by setting the Rx upper switching point to -50mV, thereby ensuring that the Rx sees 0V differential as a high input level.

The receiver can easily support a 16Mbps data rate, and its output is tri-statable via the active low $\overline{RE}$ input.

TABLE 2. V_{IH}, V_{IL} AND DATA RATE vs V_L FOR V_{CC} = 3.3V OR 5V

V_L (V)	V_{IH} (V)	V_{IL} (V)	DATA RATE (Mbps)
1.35	0.55	0.5	11
1.6	0.7	0.6	16
1.8	0.8	0.7	23
2.3	1	0.9	27
2.7	1.1	1	30
3.3	1.3	1.2	30
5.5 (i.e., V_{CC})	2	1.8	24

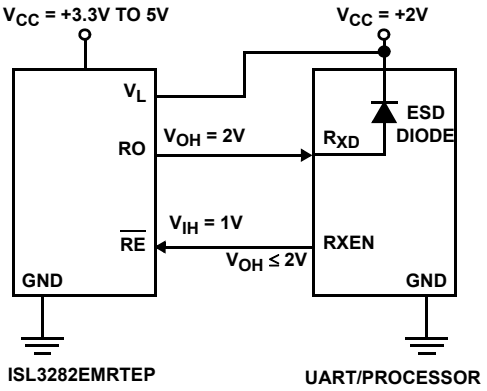


FIGURE 4. USING V_L PIN TO ADJUST LOGIC LEVELS

Wide Supply Range

The ISL3282EMRTEP is designed to operate with a wide range of supply voltages from 3.0V to 5.5V. This device meets the RS-422 and RS-485 specifications over this full range.

Logic Supply (V_L Pin)

Note: Power-up V_{CC} before powering up the V_L supply.

The ISL3282EMRTEP includes a V_L pin that powers the logic input ($\overline{RE}$) and/or the Rx output. These pins interface with "logic" devices such as UARTs, ASICs and microcontrollers. Today, most of these devices use power supplies significantly lower than 3.3V, thus, a 3.3V output level from a 3.3V powered RS-485 IC might seriously overdrive and damage the logic device input. Similarly, the logic device's low V_{OH} might not exceed the V_{IH} of a 3.3V or 5V powered $\overline{RE}$ input. Connecting the V_L pin to the power supply of the logic device (as shown in Figure 4) limits the ISL3282EMRTEP's Rx output V_{OH} to V_L (see Figures 7 through 11), and reduces the $\overline{RE}$ input switching point to a value compatible with the logic device's output levels. Tailoring the logic pin input switching point and output levels to the supply voltage of the UART, ASIC, or microcontroller eliminates the need for a level shifter/translator between the two ICs.

V_L can be anywhere from V_{CC} down to 1.35V, however, the input switching points may not provide enough noise margin when V_L < 1.6V. Table 2 indicates typical V_{IH}, V_{IL}, and data rate values for various V_L settings so the user can ascertain whether or not a particular V_L voltage meets his/her needs.

The quiescent, RO unloaded, V_L supply current (I_L) is typically less than 60µA for $V_L \leq 3.3V$, as shown in Figure 6 on page 6.

ESD Protection

All pins on the device include Class 3 (>4kV) Human Body Model (HBM) ESD protection structures, however, the RS-485 pins (receiver inputs) incorporate advanced structures allowing them to survive ESD events in excess of ±16.5kV HBM and ±16.5kV IEC61000. The RS-485 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Simply touching the port pins, or connecting a cable, can cause an ESD event that might destroy unprotected ICs. These new ESD structures protect the device whether or not it is powered up, and without degrading the RS-485 common-mode range of -7V to +12V. This built-in ESD

protection eliminates the need for board level protection structures (e.g., transient suppression diodes), and the associated, undesirable capacitive load they present.

IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment, rather than to an individual IC. Therefore, the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-485 pins in this case) and the IC is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is much more severe than the HBM test. The extra ESD protection built into this device's RS-485 pins allows the design of equipment meeting level 4 criteria without the need for additional board level protection on the RS-485 port.

AIR-GAP DISCHARGE TEST METHOD

For this test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on approach speed, humidity, temperature, etc., so it is difficult to obtain repeatable results. The A and B RS-485 pins withstand ±16.5kV air-gap discharges.

CONTACT DISCHARGE TEST METHOD

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized, thereby eliminating the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, however, equipment limits prevent testing devices at voltages higher than ±9kV. The ISL3282EMRTEP can survive ±9kV contact discharges on the RS-485 pins.

Data Rate, Cables, and Terminations

RS-485, RS-422 are intended for network lengths up to 4000', however, the maximum system data rate decreases as the transmission length increases. Networks operating at 16Mbps are limited to lengths less than 100', while a 250kbps network that uses slew rate limited transmitters can operate at that data rate over lengths of several thousand feet.

Twisted pair is the cable of choice for RS-485, RS-422 networks. Twisted pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals, which are effectively rejected by the differential receiver in these ICs.

To minimize reflections, proper termination is imperative for high data rate networks. Short networks using slew rate limited transmitters need not be terminated, however, terminations are recommended unless power dissipation is an overriding concern.

In point-to-point, or point-to-multipoint (single driver on bus) networks, the main cable should be terminated in its characteristic impedance (typically 120Ω) at the end farthest from the driver. In multireceiver applications, stubs connecting receivers to the main cable should be kept as short as possible. Multipoint (multidriver) systems require that the main cable be terminated in its characteristic impedance at both ends. Stubs connecting a transmitter or receiver to the main cable should be kept as short as possible.

Low Power Shutdown Mode

This BiCMOS receiver uses a fraction of the power required by its bipolar counterparts, and include a shutdown feature that reduces the already low quiescent I_{CC} to a 20µA trickle. They enter shutdown whenever the receiver is disabled ($\overline{RE} = V_{CC}$).

Typical Performance Curves C_L = 15pF, TA = +25°C; unless otherwise specified.

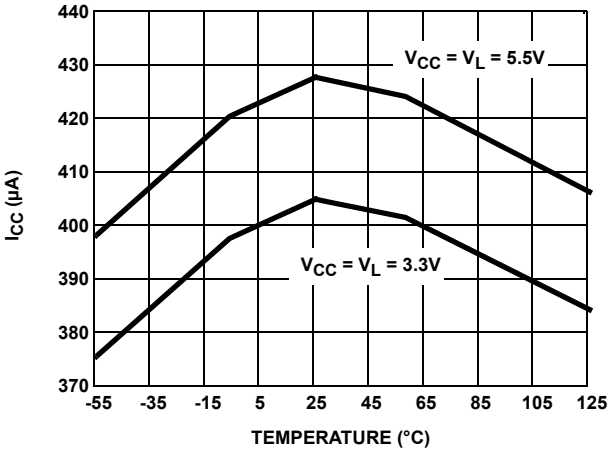


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE

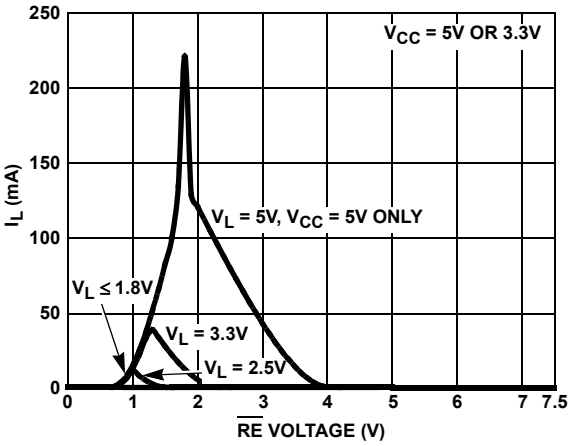


FIGURE 6. V_L SUPPLY CURRENT vs ENABLE PIN VOLTAGE

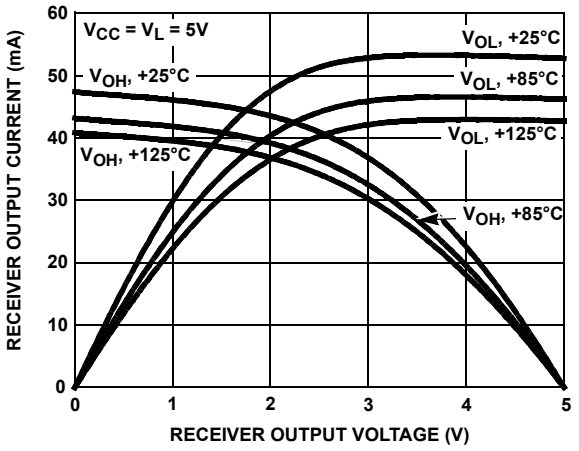


FIGURE 7. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

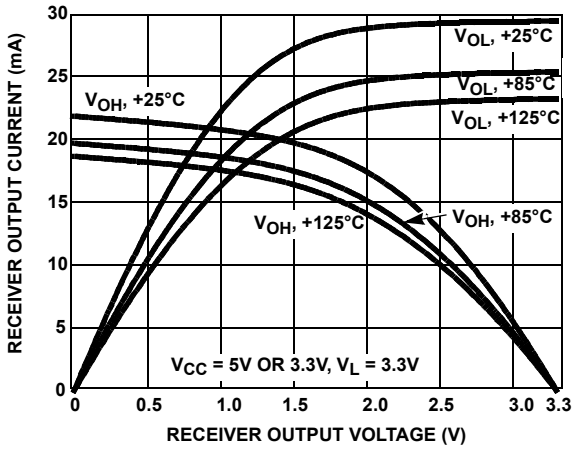


FIGURE 8. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

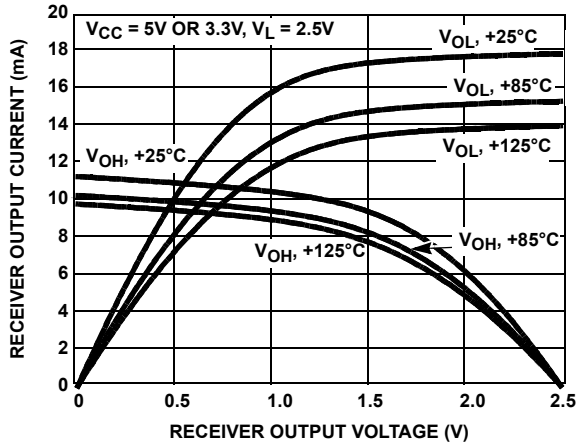


FIGURE 9. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

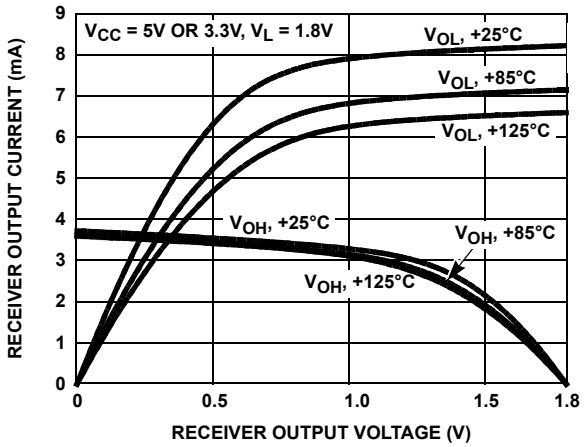


FIGURE 10. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

Typical Performance Curves C_L = 15pF, TA = +25°C; unless otherwise specified. (Continued)

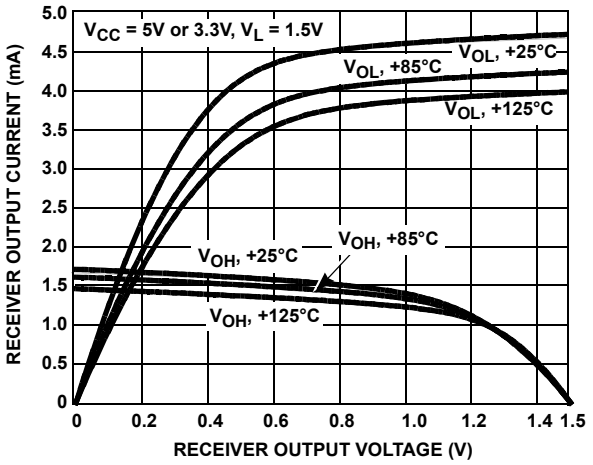


FIGURE 11. RECEIVER OUTPUT CURRENT vs RECEIVER OUTPUT VOLTAGE

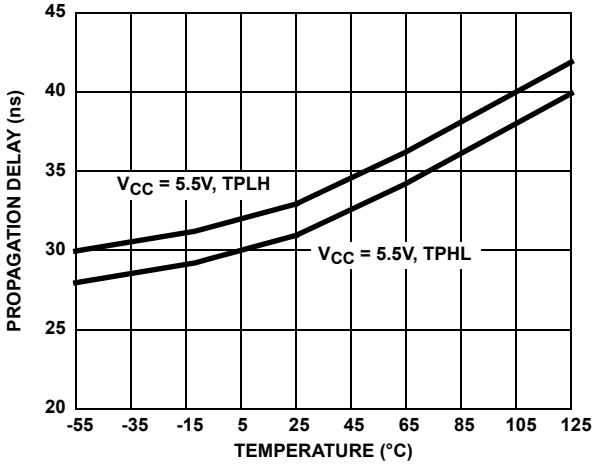


FIGURE 12. RECEIVER PROPAGATION DELAY vs TEMPERATURE

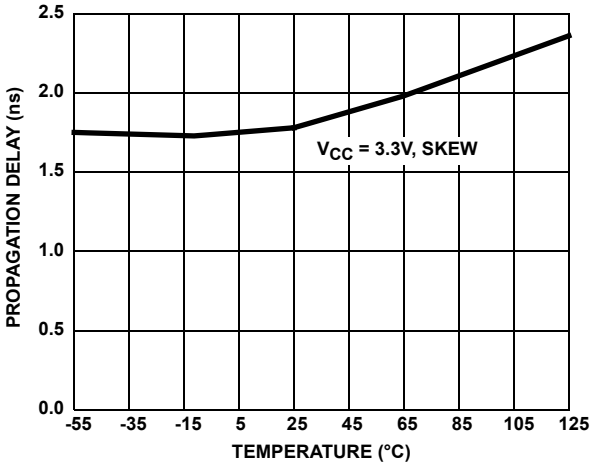


FIGURE 13. RECEIVER SKEW vs TEMPERATURE

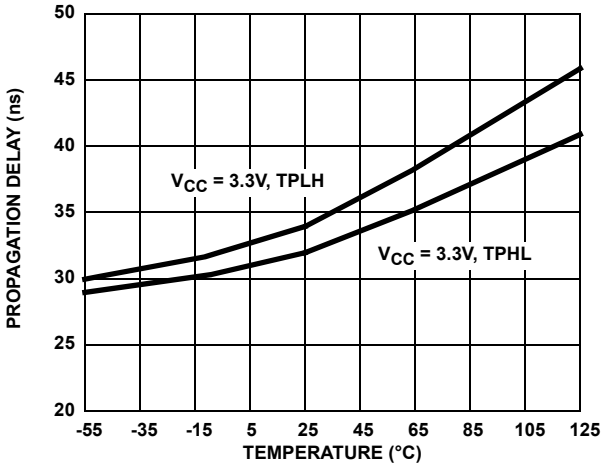


FIGURE 14. RECEIVER PROPAGATION DELAY vs TEMPERATURE

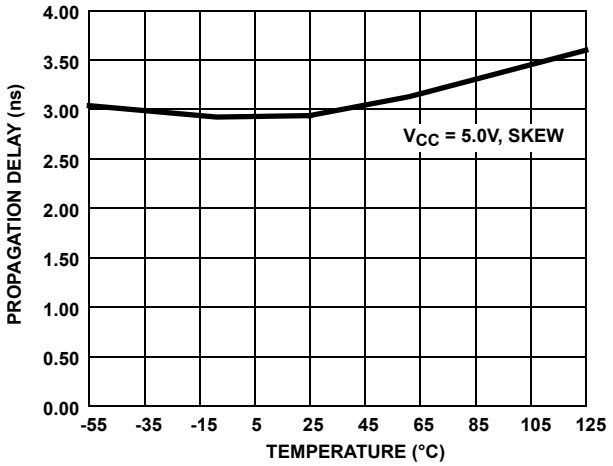


FIGURE 15. RECEIVER SKEW vs TEMPERATURE

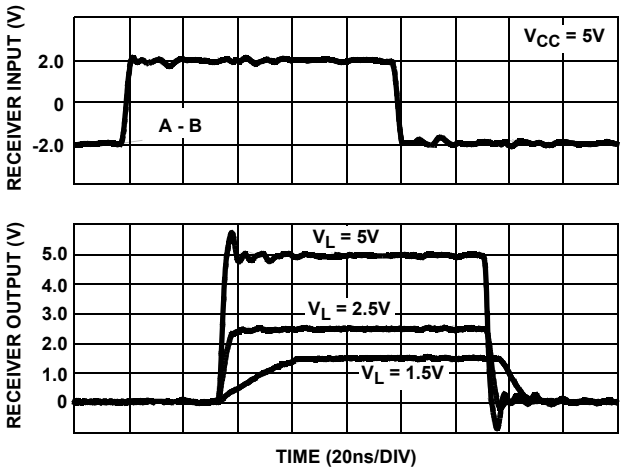


FIGURE 16. RECEIVER WAVEFORMS

Typical Performance Curves C_L = 15pF, TA = +25°C; unless otherwise specified. (Continued)

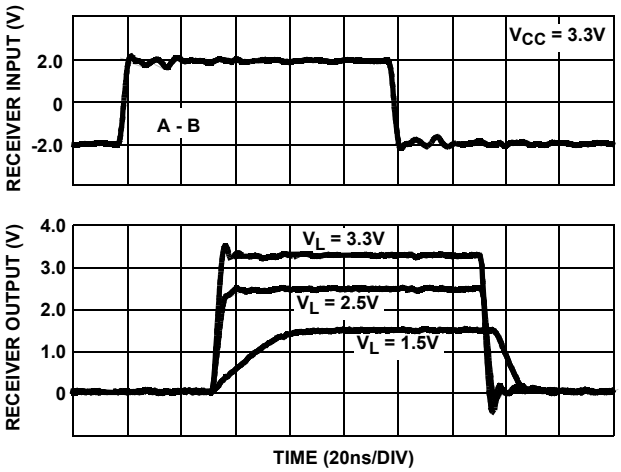


FIGURE 17. RECEIVER WAVEFORMS

Die Characteristics

SUBSTRATE AND TDFN THERMAL PAD POTENTIAL (POWERED UP):

GND

TRANSISTOR COUNT:

140

PROCESS:

Si Gate BiCMOS

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
June 17, 2016	FN7595.2	Updated title to fit 100 character limit. Removed Pb-Free bullet under Features section. Updated Ordering Information table by removing Pb-Free notes and obsolete parts. Added Tape and Reel Quantity and PKG DWG columns. Replaced Products section with About Intersil. Added the applicable POD.
January 27, 2011	FN7595.1	In Figure 5 on page 6, corrected units of y axis from mA to µA.
February 26, 2010	FN7595.0	Initial Release.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

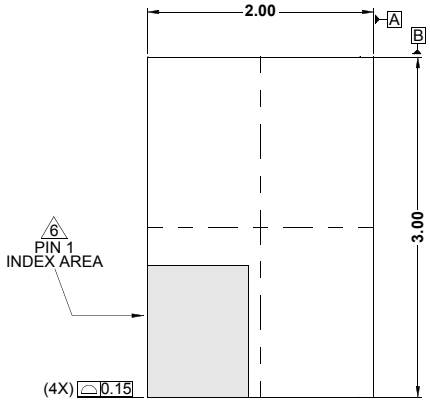
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

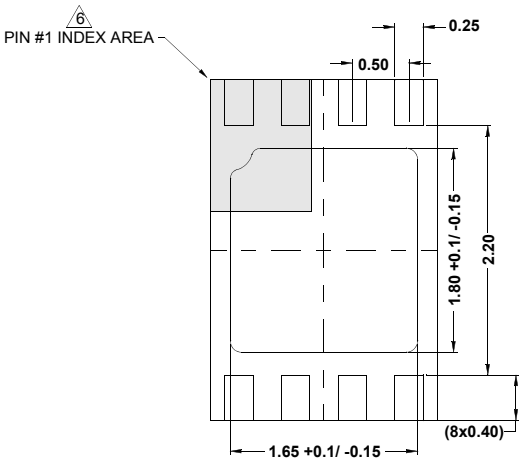
L8.2x3A

8 LEAD THIN DUAL FLAT NO-LEAD PLASTIC PACKAGE WITH E-PAD

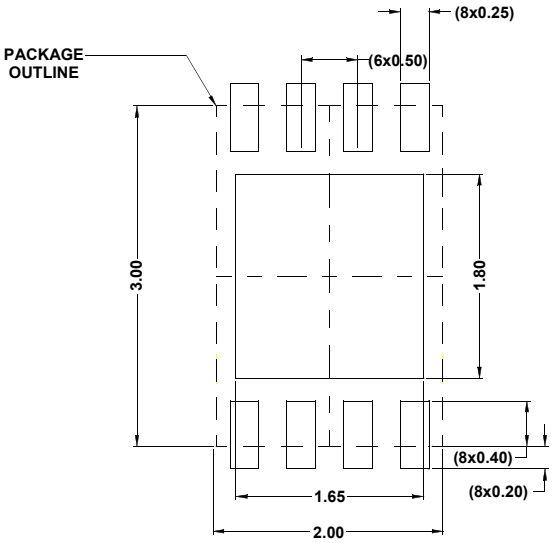
Rev 2, 05/15



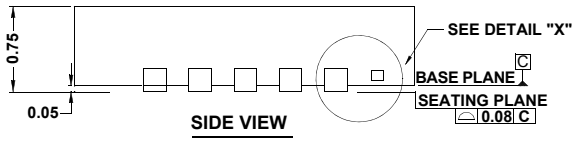
TOP VIEW



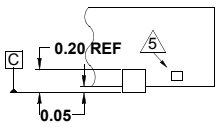
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.20mm and 0.32mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.

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