1. Introduction

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Introduction

Following the immensely successful first-generation Cyclone® device family, Altera® Cyclone II FPGAs extend the low-cost FPGA density range to 68,416 logic elements (LEs) and provide up to 622 usable I/O pins and up to 1.1 Mbits of embedded memory. Cyclone II FPGAs are manufactured on 300-mm wafers using TSMC's 90-nm low-k dielectric process to ensure rapid availability and low cost. By minimizing silicon area, Cyclone II devices can support complex digital systems on a single chip at a cost that rivals that of ASICs. Unlike other FPGA vendors who compromise power consumption and performance for low-cost, Altera's latest generation of low-cost FPGAs—Cyclone II FPGAs, offer 60% higher performance and half the power consumption of competing 90-nm FPGAs. The low cost and optimized feature set of Cyclone II FPGAs make them ideal solutions for a wide array of automotive, consumer, communications, video processing, test and measurement, and other end-market solutions. Reference designs, system diagrams, and IP, found at www.altera.com, are available to help you rapidly develop complete end-market solutions using Cyclone II FPGAs.

Low-Cost Embedded Processing Solutions

Cyclone II devices support the Nios II embedded processor which allows you to implement custom-fit embedded processing solutions. Cyclone II devices can also expand the peripheral set, memory, I/O, or performance of embedded processors. Single or multiple Nios II embedded processors can be designed into a Cyclone II device to provide additional co-processing power or even replace existing embedded processors in your system. Using Cyclone II and Nios II together allow for low-cost, high-performance embedded processing solutions, which allow you to extend your product's life cycle and improve time to market over standard product solutions.

Low-Cost DSP Solutions

Use Cyclone II FPGAs alone or as DSP co-processors to improve price-to-performance ratios for digital signal processing (DSP) applications. You can implement high-performance yet low-cost DSP systems with the following Cyclone II features and design support:

- Up to 150 18 × 18 multipliers
- Up to 1.1 Mbit of on-chip embedded memory
- High-speed interfaces to external memory

- DSP intellectual property (IP) cores
- DSP Builder interface to The Mathworks Simulink and Matlab design environment
- DSP Development Kit, Cyclone II Edition

Cyclone II devices include a powerful FPGA feature set optimized for low-cost applications including a wide range of density, memory, embedded multiplier, and packaging options. Cyclone II devices support a wide range of common external memory interfaces and I/O protocols required in low-cost applications. Parameterizable IP cores from Altera and partners make using Cyclone II interfaces and protocols fast and easy.

Features

The Cyclone II device family offers the following features:

- High-density architecture with 4,608 to 68,416 LEs
  - M4K embedded memory blocks
  - Up to 1.1 Mbits of RAM available without reducing available logic
  - 4,096 memory bits per block (4,608 bits per block including 512 parity bits)
  - Variable port configurations of ×1, ×2, ×4, ×8, ×9, ×16, ×18, ×32, and ×36
  - True dual-port (one read and one write, two reads, or two writes) operation for ×1, ×2, ×4, ×8, ×9, ×16, and ×18 modes
  - Byte enables for data input masking during writes
  - Up to 260-MHz operation
- Embedded multipliers
  - Up to 150 18- × 18-bit multipliers are each configurable as two independent 9- × 9-bit multipliers with up to 250-MHz performance
  - Optional input and output registers
- Advanced I/O support
  - High-speed differential I/O standard support, including LVDS, RSDS, mini-LVDS, LVPECL, differential HSTL, and differential SSTL
  - Single-ended I/O standard support, including 2.5-V and 1.8-V, SSTL class I and II, 1.8-V and 1.5-V HSTL class I and II, 3.3-V PCI and PCI-X 1.0, 3.3-, 2.5-, 1.8-, and 1.5-V LVCMOS, and 3.3-, 2.5-, and 1.8-V LVTTL
  - Peripheral Component Interconnect Special Interest Group (PCI SIG) *PCI Local Bus Specification, Revision 3.0* compliance for 3.3-V operation at 33 or 66 MHz for 32- or 64-bit interfaces
  - PCI Express with an external TI PHY and an Altera PCI Express ×1 Megacore® function

- 133-MHz PCI-X 1.0 specification compatibility
- High-speed external memory support, including DDR, DDR2, and SDR SDRAM, and QDRII SRAM supported by drop in Altera IP MegaCore functions for ease of use
- Three dedicated registers per I/O element (IOE): one input register, one output register, and one output-enable register
- Programmable bus-hold feature
- Programmable output drive strength feature
- Programmable delays from the pin to the IOE or logic array
- I/O bank grouping for unique VCCIO and/or VREF bank settings
- MultiVolt™ I/O standard support for 1.5-, 1.8-, 2.5-, and 3.3-interfaces
- Hot-socketing operation support
- Tri-state with weak pull-up on I/O pins before and during configuration
- Programmable open-drain outputs
- Series on-chip termination support

- Flexible clock management circuitry
  - Hierarchical clock network for up to 402.5-MHz performance
  - Up to four PLLs per device provide clock multiplication and division, phase shifting, programmable duty cycle, and external clock outputs, allowing system-level clock management and skew control
  - Up to 16 global clock lines in the global clock network that drive throughout the entire device

- Device configuration
  - Fast serial configuration allows configuration times less than 100 ms
  - Decompression feature allows for smaller programming file storage and faster configuration times
  - Supports multiple configuration modes: active serial, passive serial, and JTAG-based configuration
  - Supports configuration through low-cost serial configuration devices
  - Device configuration supports multiple voltages (either 3.3, 2.5, or 1.8 V)

- Intellectual property
  - Altera megafunction and Altera MegaCore function support, and Altera Megafunctions Partners Program (AMPP^{SM}) megafunction support, for a wide range of embedded processors, on-chip and off-chip interfaces, peripheral functions, DSP functions, and communications functions and

protocols. Visit the Altera IPMegaStore at www.altera.com to download IP MegaCore functions.

- Nios II Embedded Processor support

The Cyclone II family offers devices with the Fast-On feature, which offers a faster power-on-reset (POR) time. Devices that support the Fast-On feature are designated with an "A" in the device ordering code. For example, EP2C5A, EP2C8A, EP2C15A, and EP2C20A. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A are only available in the industrial speed grade. The EP2C15A is only available with the Fast-On feature and is available in both commercial and industrial grades. The Cyclone II "A" devices are identical in feature set and functionality to the non-A devices except for support of the faster POR time.

Cyclone II A devices are offered in automotive speed grade. For more information, refer to the Cyclone II section in the *Automotive-Grade Device Handbook*.

For more information on POR time specifications for Cyclone II A and non-A devices, refer to the *Hot Socketing & Power-On Reset* chapter in the *Cyclone II Device Handbook*.

Table 1–1 lists the Cyclone II device family features. Table 1–2 lists the Cyclone II device package offerings and maximum user I/O pins.

Table 1–1. Cyclone II FPGA Family Features (Part 1 of 2)

Feature	EP2C5 *(2)*	EP2C8 *(2)*	EP2C15 *(1)*	EP2C20 *(2)*	EP2C35	EP2C50	EP2C70
LEs	4,608	8,256	14,448	18,752	33,216	50,528	68,416
M4K RAM blocks (4 Kbits plus 512 parity bits	26	36	52	52	105	129	250
Total RAM bits	119,808	165,888	239,616	239,616	483,840	594,432	1,152,000
Embedded multipliers *(3)*	13	18	26	26	35	86	150
PLLs	2	2	4	4	4	4	4

Table 1–1. Cyclone II FPGA Family Features (Part 2 of 2)

Feature	EP2C5 (2)	EP2C8 (2)	EP2C15 (1)	EP2C20 (2)	EP2C35	EP2C50	EP2C70
Maximum user I/O pins	158	182	315	315	475	450	622

Notes to Table 1–1:

(1) The EP2C15A is only available with the Fast On feature, which offers a faster POR time. This device is available in both commercial and industrial grade.

(2) The EP2C5, EP2C8, and EP2C20 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. The EP2C8A and EP2C20A devices are only available in industrial grade.

(3) This is the total number of 18 × 18 multipliers. For the total number of 9 × 9 multipliers per device, multiply the total number of 18 × 18 multipliers by 2.

Table 1–2. Cyclone II Package Options & Maximum User I/O Pins *Notes (1) (2)*

Device	144-Pin TQFP *(3)*	208-Pin PQFP *(4)*	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(6) (8)*	89	142	—	158 *(5)*	—	—	—	—
EP2C8 *(6)*	85	138	—	182	—	—	—	—
EP2C8A *(6)*, *(7)*	—	—	—	182	—	—	—	—
EP2C15A *(6)*, *(7)*	—	—	—	152	315	—	—	—
EP2C20 *(6)*	—	—	142	152	315	—	—	—
EP2C20A *(6)*, *(7)*	—	—	—	152	315	—	—	—
EP2C35 *(6)*	—	—	—	—	322	322	475	—
EP2C50 *(6)*	—	—	—	—	294	294	450	—
EP2C70 *(6)*	—	—	—	—	—	—	422	622

Notes to Table 1–2:

(1) Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C20 device in the 484-pin FineLine BGA package and the EP2C35 and EP2C50 devices in the same package).

(2) The Quartus® II software I/O pin counts include four additional pins, `TDI`, `TDO`, `TMS`, and `TCK`, which are not available as general purpose I/O pins.

(3) TQFP: thin quad flat pack.

(4) PQFP: plastic quad flat pack.

(5) Vertical migration is supported between the EP2C5F256 and the EP2C8F256 devices. However, not all of the DQ and DQS groups are supported. Vertical migration between the EP2C5 and the EP2C15 in the F256 package is not supported.

(6) The I/O pin counts for the EP2C5, EP2C8, and EP2C15A devices include 8 dedicated clock pins that can be used for data inputs. The I/O counts for the EP2C20, EP2C35, EP2C50, and EP2C70 devices include 16 dedicated clock pins that can be used for data inputs.

(7) EP2C8A, EP2C15A, and EP2C20A have a Fast On feature that has a faster POR time. The EP2C15A is only available with the Fast On option.

(8) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook*.

Cyclone II devices support vertical migration within the same package (for example, you can migrate between the EP2C35, EPC50, and EP2C70 devices in the 672-pin FineLine BGA package). The exception to vertical migration support within the Cyclone II family is noted in Table 1–3.

Vertical migration means that you can migrate to devices whose dedicated pins, configuration pins, and power pins are the same for a given package across device densities.

Table 1–3. Total Number of Non-Migratable I/O Pins for Cyclone II Vertical Migration Paths

Vertical Migration Path	144-Pin TQFP	208-Pin PQFP	256-Pin FineLine BGA *(1)*	484-Pin FineLine BGA *(2)*	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA *(3)*
EP2C5 to EP2C8	4	4	1 *(4)*	—	—	—
EP2C8 to EP2C15	—	—	30	—	—	—
EP2C15 to EP2C20	—	—	0	0	—	—
EP2C20 to EP2C35		—	—	16	—	—
EP2C35 to EP2C50	—	—	—	28	28 *(5)*	28
EP2C50 to EP2C70	—	—	—	—	28	28

Notes to Table 1–3:

(1) Vertical migration between the EP2C5F256 to the EP2C15AF256 and the EP2C5F256 to the EP2C20F256 devices is not supported.
(2) When migrating from the EP2C20F484 device to the EP2C50F484 device, a total of 39 I/O pins are non-migratable.
(3) When migrating from the EP2C35F672 device to the EP2C70F672 device, a total of 56 I/O pins are non-migratable.
(4) In addition to the one non-migratable I/O pin, there are 34 DQ pins that are non-migratable.
(5) The pinouts of 484 FBGA and 484 UBGA are the same.

When moving from one density to a larger density, I/O pins are often lost because of the greater number of power and ground pins required to support the additional logic within the larger device. For I/O pin migration across densities, you must cross reference the available I/O pins using the device pin-outs for all planned densities of a given package type to identify which I/O pins are migratable.

To ensure that your board layout supports migratable densities within one package offering, enable the applicable vertical migration path within the Quartus II software (go to Assignments menu, then Device, then click the **Migration Devices** button). After compilation, check the information messages for a full list of I/O, DQ, LVDS, and other pins that are not available because of the selected migration path. Table 1–3 lists the Cyclone II device package offerings and shows the total number of non-migratable I/O pins when migrating from one density device to a larger density device.

Cyclone II devices are available in up to three speed grades: –6, –7, and –8, with –6 being the fastest. Table 1–4 shows the Cyclone II device speed-grade offerings.

Table 1–4. Cyclone II Device Speed Grades

Device	144-Pin TQFP	208-Pin PQFP	240-Pin PQFP	256-Pin FineLine BGA	484-Pin FineLine BGA	484-Pin Ultra FineLine BGA	672-Pin FineLine BGA	896-Pin FineLine BGA
EP2C5 *(1)*	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8	–6, –7, –8	–7, –8	—	–6, –7, –8	—	—	—	—
EP2C8A *(2)*	—	—	—	–8	—	—	—	—
EP2C15A	—	—	—	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20	—	—	–8	–6, –7, –8	–6, –7, –8	—	—	—
EP2C20A *(2)*	—	—	—	–8	–8	—	—	—
EP2C35	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C50	—	—	—	—	–6, –7, –8	–6, –7, –8	–6, –7, –8	—
EP2C70	—	—	—	—	—	—	–6, –7, –8	–6, –7, –8

Notes to Table 1–4:

(1) The EP2C5 optionally support the Fast On feature, which is designated with an "A" in the device ordering code. The EP2C5A is only available in the automotive speed grade. Refer to the Cyclone II section in the *Automotive-Grade Device Handbook* for detailed information.

(2) EP2C8A and EP2C20A are only available in industrial grade.

Referenced Documents

This chapter references the following documents:

- *Hot Socketing & Power-On Reset* chapter in *Cyclone II Device Handbook*
- *Automotive-Grade Device Handbook*

Document Revision History

Table 1–5 shows the revision history for this document.

Table 1–5. Document Revision History

Date & Document Version	Changes Made	Summary of Changes
February 2008 v3.2	• Added "Referenced Documents". • Updated "Features" section and Table 1–1, Table 1–2, and Table 1–4 with information about EP2C5A.	—
February 2007 v3.1	• Added document revision history. • Added new *Note (2)* to Table 1–2.	Note to explain difference between I/O pin count information provided in Table 1–2 and in the Quartus II software documentation.
November 2005 v2.1	• Updated Introduction and Features. • Updated Table 1–3.	—
July 2005 v2.0	• Updated technical content throughout. • Updated Table 1–2. • Added Tables 1–3 and 1–4.	—
November 2004 v1.1	• Updated Table 1–2. • Updated bullet list in the "Features" section.	—
June 2004 v1.0	Added document to the Cyclone II Device Handbook.	—

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