

# PEMD12; PUMD12

NPN/PNP resistor-equipped transistors;  
R1 = 47 k $\Omega$ , R2 = 47 k $\Omega$

Rev. 4 — 21 November 2011

Product data sheet

## 1. Product profile

### 1.1 General description

NPN/PNP double Resistor-Equipped Transistors (RET) in Surface-Mounted Device (SMD) plastic packages.

Table 1. Product overview

Type number	Package		PNP/PNP complement	NPN/NPN complement	Package configuration
	NXP	JEITA			
PEMD12	SOT666	-	PEMB2	PEMH2	ultra small and flat lead
PUMD12	SOT363	SC-88	PUMB2	PUMH2	very small

### 1.2 Features and benefits

- 100 mA output current capability
- Built-in bias resistors
- Simplifies circuit design
- Reduces component count
- Reduces pick and place costs
- AEC-Q101 qualified

### 1.3 Applications

- Low current peripheral driver
- Control of IC inputs
- Replaces general-purpose transistors in digital applications

### 1.4 Quick reference data

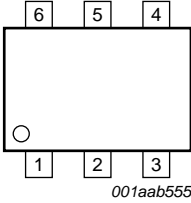
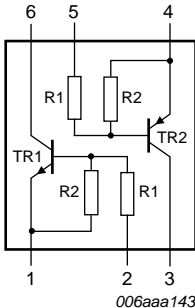
Table 2. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor (TR2) with negative polarity</b>						
V <sub>CEO</sub>	collector-emitter voltage	open base	-	-	50	V
I <sub>O</sub>	output current		-	-	100	mA
R1	bias resistor 1 (input)		33	47	61	k $\Omega$
R2/R1	bias resistor ratio		0.8	1	1.2	



## 2. Pinning information

Table 3. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	GND (emitter) TR1		
2	input (base) TR1		
3	output (collector) TR2		
4	GND (emitter) TR2		
5	input (base) TR2		
6	output (collector) TR1		

## 3. Ordering information

Table 4. Ordering information

Type number	Package		Version
	Name	Description	
PEMD12	-	plastic surface-mounted package; 6 leads	SOT666
PUMD12	SC-88	plastic surface-mounted package; 6 leads	SOT363

## 4. Marking

Table 5. Marking codes

Type number	Marking code <sup>[1]</sup>
PEMD12	D2
PUMD12	D*1

[1] \* = placeholder for manufacturing site code

## 5. Limiting values

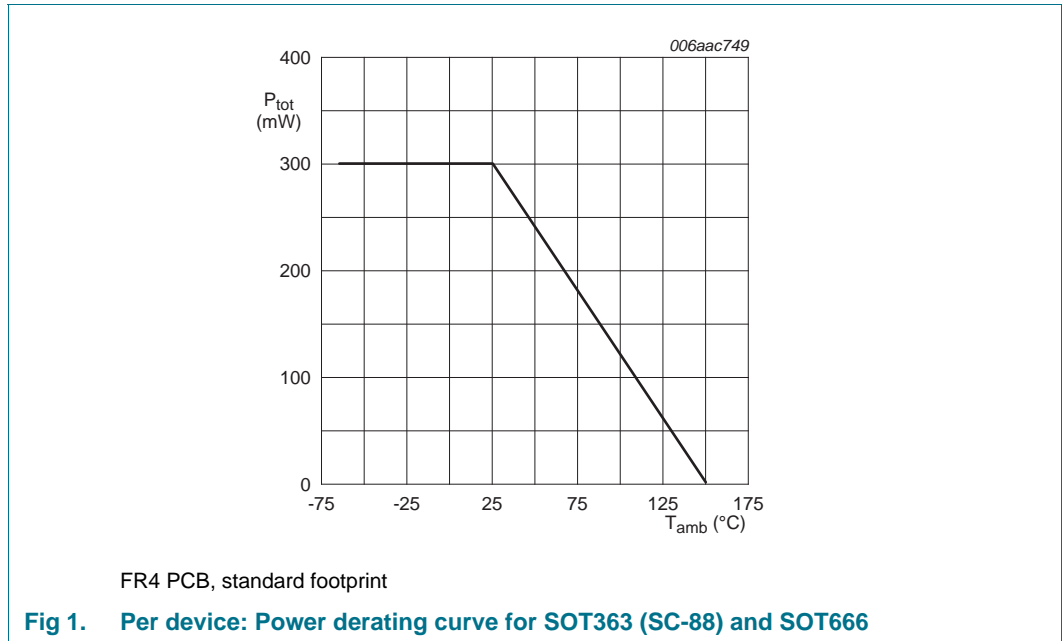
**Table 6. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor; for the PNP transistor (TR2) with negative polarity</b>						
$V_{CBO}$	collector-base voltage	open emitter	-	50	V	
$V_{CEO}$	collector-emitter voltage	open base	-	50	V	
$V_{EBO}$	emitter-base voltage	open collector	-	10	V	
$V_I$	input voltage TR1					
	positive		-	+40	V	
	negative		-	-10	V	
	input voltage TR2					
	positive		-	+10	V	
	negative		-	-40	V	
$I_O$	output current		-	100	mA	
$I_{CM}$	peak collector current	single pulse; $t_p \leq 1$ ms	-	100	mA	
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD12 (SOT666)		[1][2]	-	200	mW
	PUMD12 (SOT363)		[1]	-	200	mW
<b>Per device</b>						
$P_{tot}$	total power dissipation	$T_{amb} \leq 25$ °C				
	PEMD12 (SOT666)		[1][2]	-	300	mW
	PUMD12 (SOT363)		[1]	-	300	mW
$T_j$	junction temperature		-	150	°C	
$T_{amb}$	ambient temperature		-65	+150	°C	
$T_{stg}$	storage temperature		-65	+150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



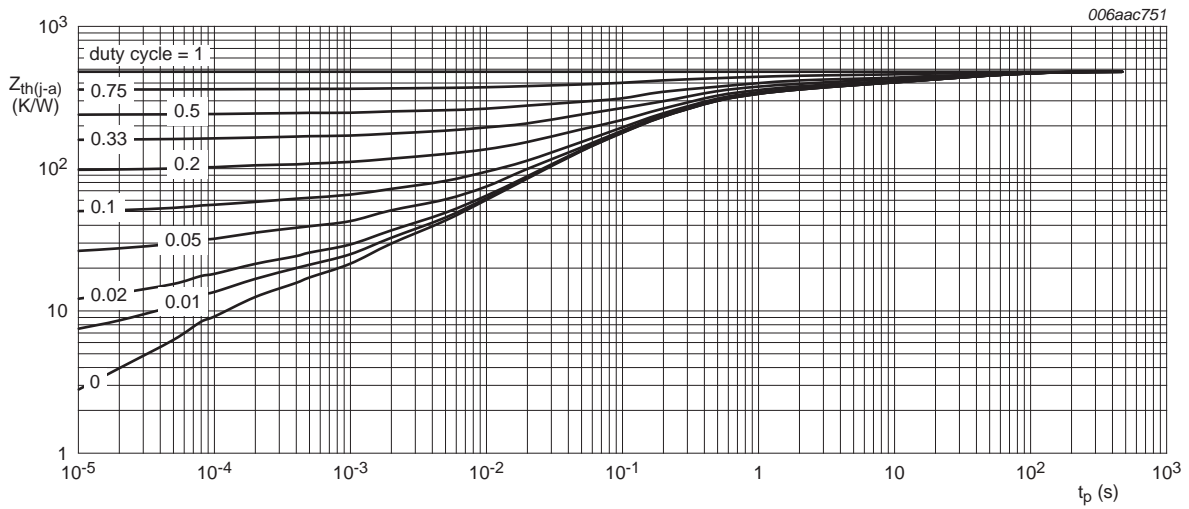
## 6. Thermal characteristics

**Table 7. Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
			[1][2]	-	625	K/W
			[1]	-	625	K/W
<b>Per device</b>						
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air				
			[1][2]	-	417	K/W
			[1]	-	417	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Reflow soldering is the only recommended soldering method.



FR4 PCB, standard footprint

**Fig 2. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PEMD12 (SOT666); typical values**



FR4 PCB, standard footprint

**Fig 3. Per transistor: Transient thermal impedance from junction to ambient as a function of pulse duration for PUMD12 (SOT363); typical values**

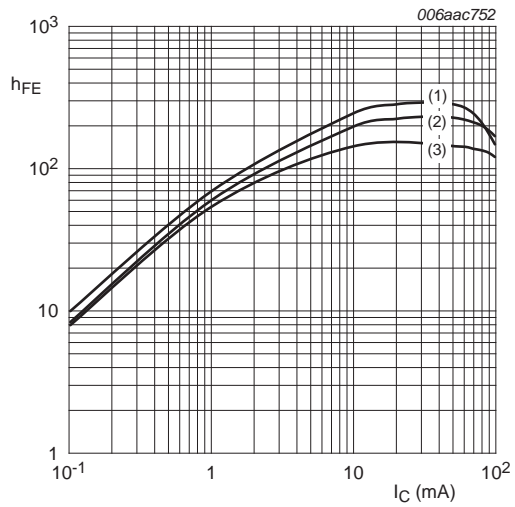
## 7. Characteristics

**Table 8. Characteristics**

$T_{amb} = 25\text{ °C}$  unless otherwise specified.

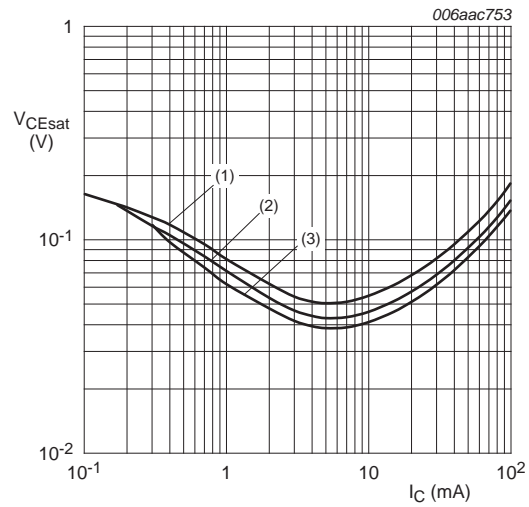
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor; for the PNP transistor (TR2) with negative polarity</b>						
$I_{CBO}$	collector-base cut-off current	$V_{CB} = 50\text{ V}; I_E = 0\text{ A}$	-	-	100	nA
$I_{CEO}$	collector-emitter cut-off current	$V_{CE} = 30\text{ V}; I_B = 0\text{ A}$	-	-	1	$\mu\text{A}$
		$V_{CE} = 30\text{ V}; I_B = 0\text{ A}; T_j = 150\text{ °C}$	-	-	5	$\mu\text{A}$
$I_{EBO}$	emitter-base cut-off current	$V_{EB} = 5\text{ V}; I_C = 0\text{ A}$	-	-	90	$\mu\text{A}$
$h_{FE}$	DC current gain	$V_{CE} = 5\text{ V}; I_C = 5\text{ mA}$	80	-	-	
$V_{CEsat}$	collector-emitter saturation voltage	$I_C = 10\text{ mA}; I_B = 0.5\text{ mA}$	-	-	150	mV
$V_{I(off)}$	off-state input voltage	$V_{CE} = 5\text{ V}; I_C = 100\text{ }\mu\text{A}$	-	1.2	0.8	V
$V_{I(on)}$	on-state input voltage	$V_{CE} = 0.3\text{ V}; I_C = 2\text{ mA}$	3	1.6	-	V
R1	bias resistor 1 (input)		33	47	61	kΩ
R2/R1	bias resistor ratio		0.8	1	1.2	
$C_c$	collector capacitance	$V_{CB} = 10\text{ V}; I_E = i_e = 0\text{ A}; f = 1\text{ MHz}$				
		TR1 (NPN)	-	-	2.5	pF
		TR2 (PNP)	-	-	3	pF
$f_T$	transition frequency	$V_{CE} = 5\text{ V}; I_C = 10\text{ mA}; f = 100\text{ MHz}$ <a href="#">[1]</a>				
		TR1 (NPN)	-	230	-	MHz
		TR2 (PNP)	-	180	-	MHz

[1] Characteristics of built-in transistor



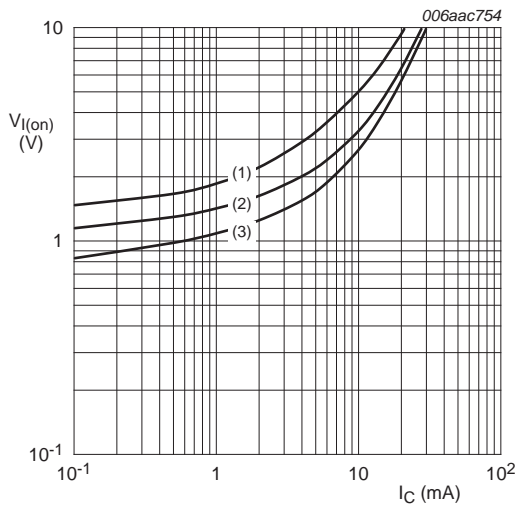
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig 4. TR1 (NPN): DC current gain as a function of collector current; typical values**



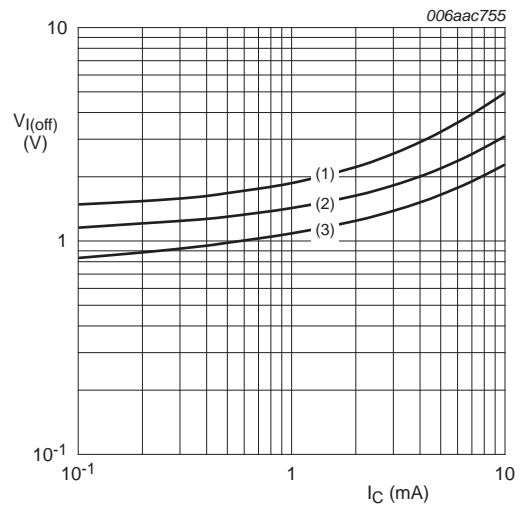
$I_C/I_B = 20$   
 (1)  $T_{amb} = 100\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = -40\text{ °C}$

**Fig 5. TR1 (NPN): Collector-emitter saturation voltage as a function of collector current; typical values**



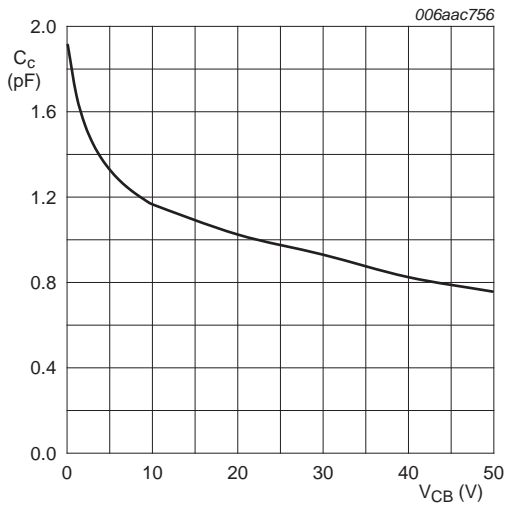
$V_{CE} = 0.3\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 6. TR1 (NPN): On-state input voltage as a function of collector current; typical values**



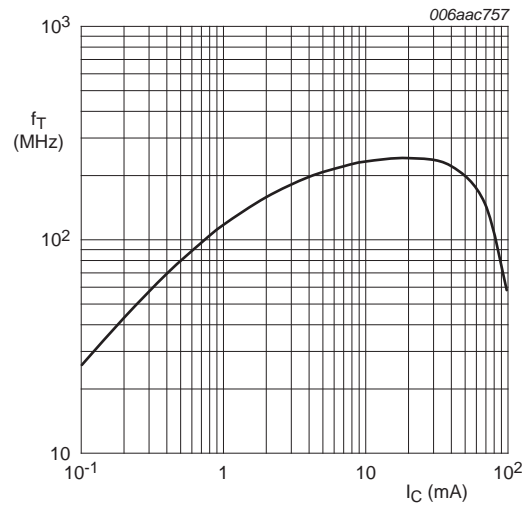
$V_{CE} = 5\text{ V}$   
 (1)  $T_{amb} = -40\text{ °C}$   
 (2)  $T_{amb} = 25\text{ °C}$   
 (3)  $T_{amb} = 100\text{ °C}$

**Fig 7. TR1 (NPN): Off-state input voltage as a function of collector current; typical values**



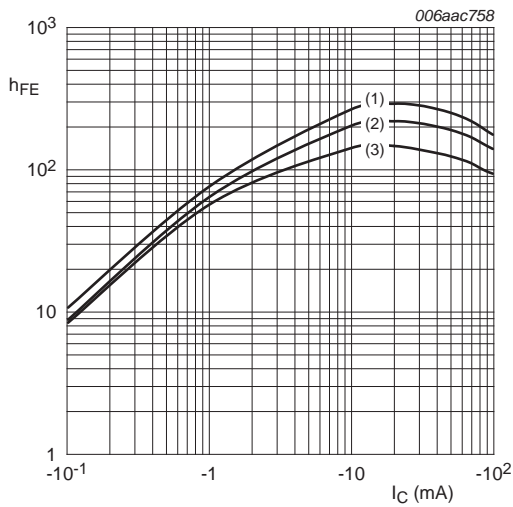
$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 8. TR1 (NPN): Collector capacitance as a function of collector-base voltage; typical values**



$V_{CE} = 5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

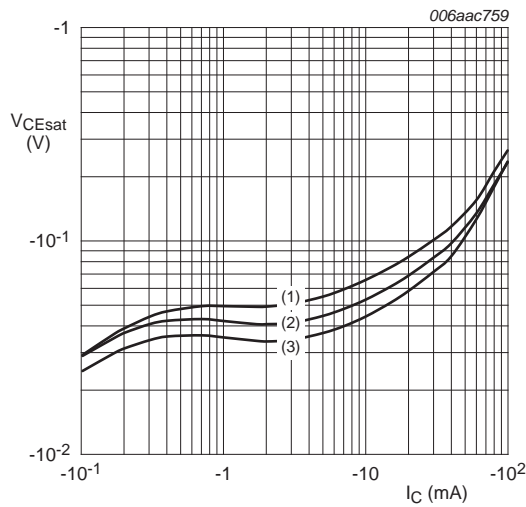
**Fig 9. TR1 (NPN): Transition frequency as a function of collector current; typical values of built-in transistor**



$V_{CE} = -5 \text{ V}$

- (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

**Fig 10. TR2 (PNP): DC current gain as a function of collector current; typical values**

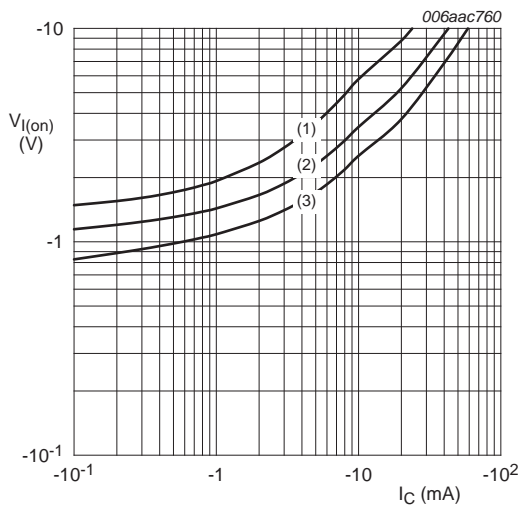


$I_C/I_B = 20$

- (1)  $T_{amb} = 100 \text{ }^\circ\text{C}$
- (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$
- (3)  $T_{amb} = -40 \text{ }^\circ\text{C}$

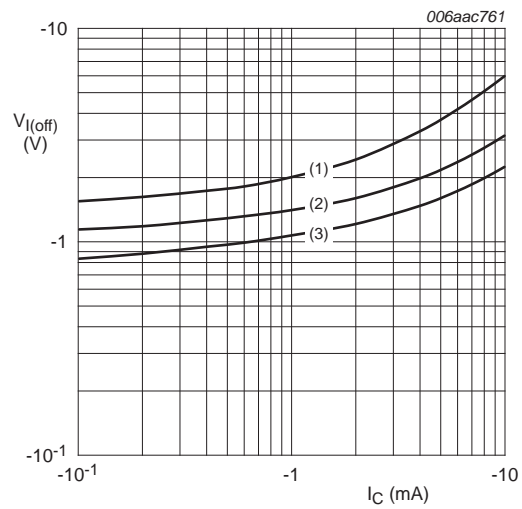
**Fig 11. TR2 (PNP): Collector-emitter saturation voltage as a function of collector current; typical values**





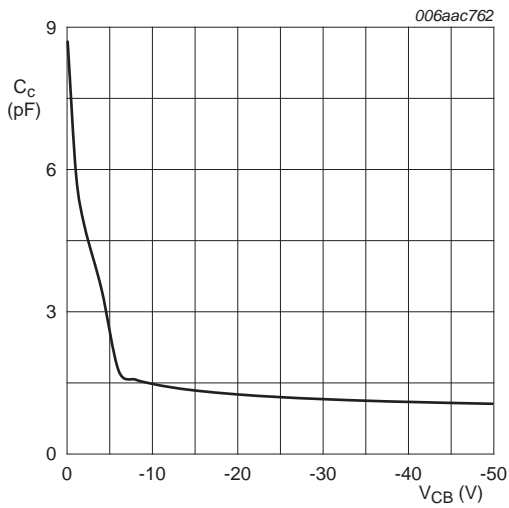
$V_{CE} = -0.3 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 12. TR2 (PNP): On-state input voltage as a function of collector current; typical values**



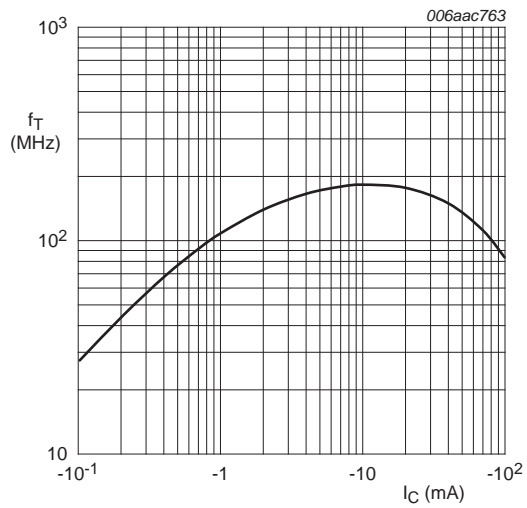
$V_{CE} = -5 \text{ V}$   
 (1)  $T_{amb} = -40 \text{ }^\circ\text{C}$   
 (2)  $T_{amb} = 25 \text{ }^\circ\text{C}$   
 (3)  $T_{amb} = 100 \text{ }^\circ\text{C}$

**Fig 13. TR2 (PNP): Off-state input voltage as a function of collector current; typical values**



$f = 1 \text{ MHz}; T_{amb} = 25 \text{ }^\circ\text{C}$

**Fig 14. TR2 (PNP): Collector capacitance as a function of collector-base voltage; typical values of built-in transistor**



$V_{CE} = -5 \text{ V}; T_{amb} = 25 \text{ }^\circ\text{C}$

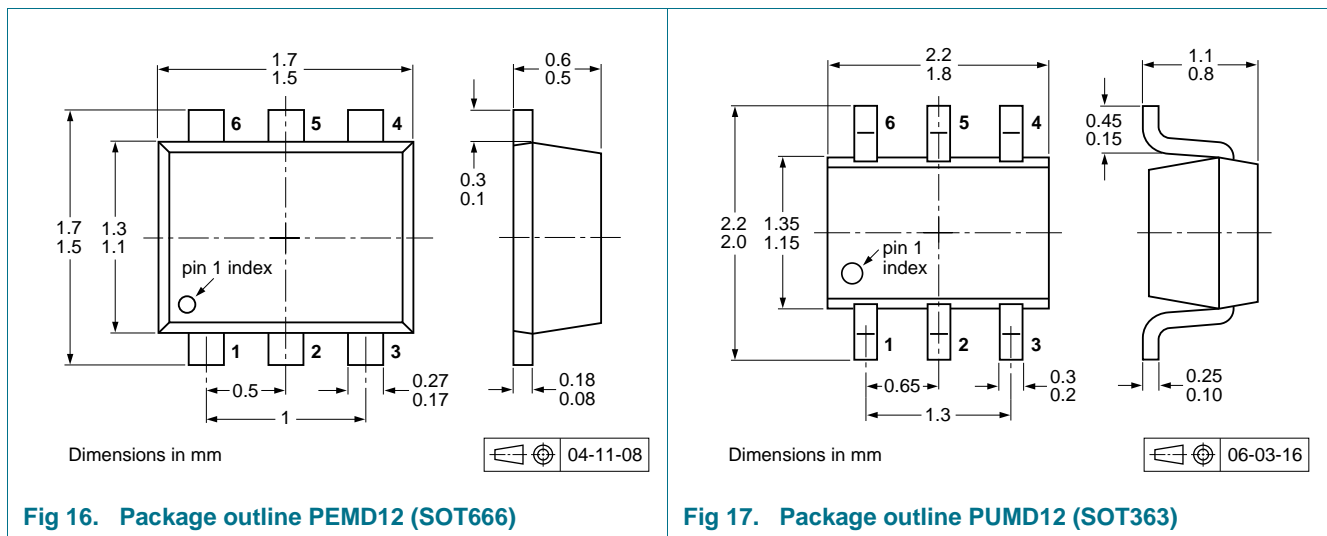
**Fig 15. TR2 (PNP): Transition frequency as a function of collector current; typical values of built-in transistor**

## 8. Test information

### 8.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q101 - Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 9. Package outline



## 10. Packing information

**Table 9. Packing methods**

The indicated -xxx are the last three digits of the 12NC ordering code.<sup>[1]</sup>

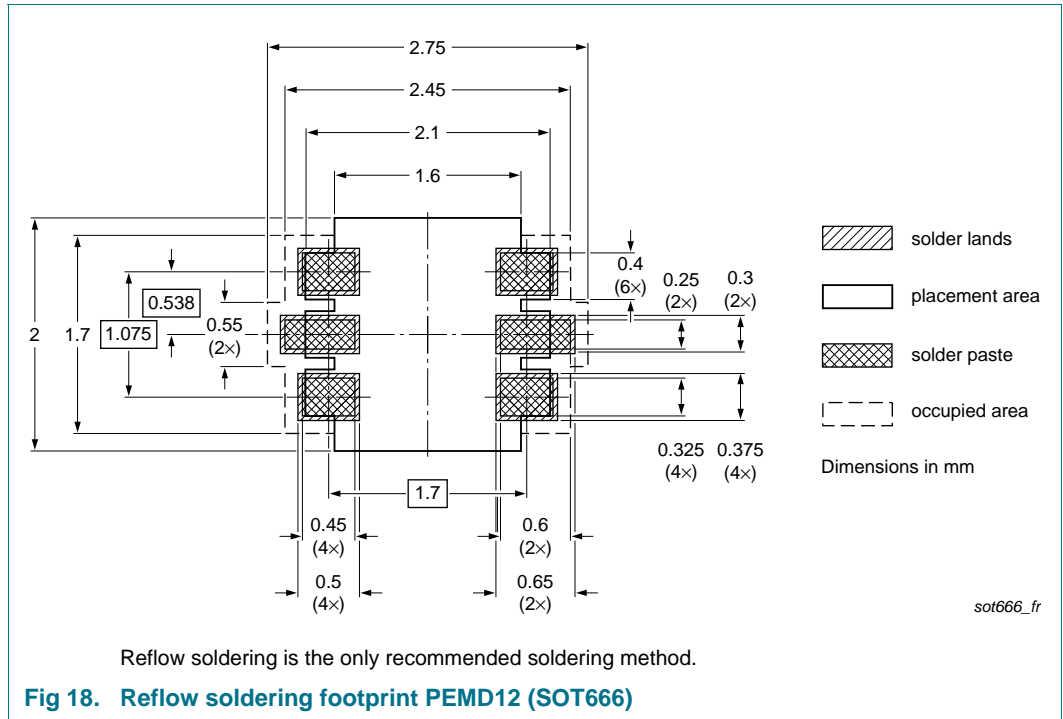
Type number	Package	Description	Packing quantity			
			3000	4000	8000	10000
PEMD12	SOT666	2 mm pitch, 8 mm tape and reel	-	-	-315	-
		4 mm pitch, 8 mm tape and reel	-	-115	-	-
PUMD12	SOT363	4 mm pitch, 8 mm tape and reel; T1 <sup>[2]</sup>	-115	-	-	-135
		4 mm pitch, 8 mm tape and reel; T2 <sup>[3]</sup>	-125	-	-	-165

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

## 11. Soldering



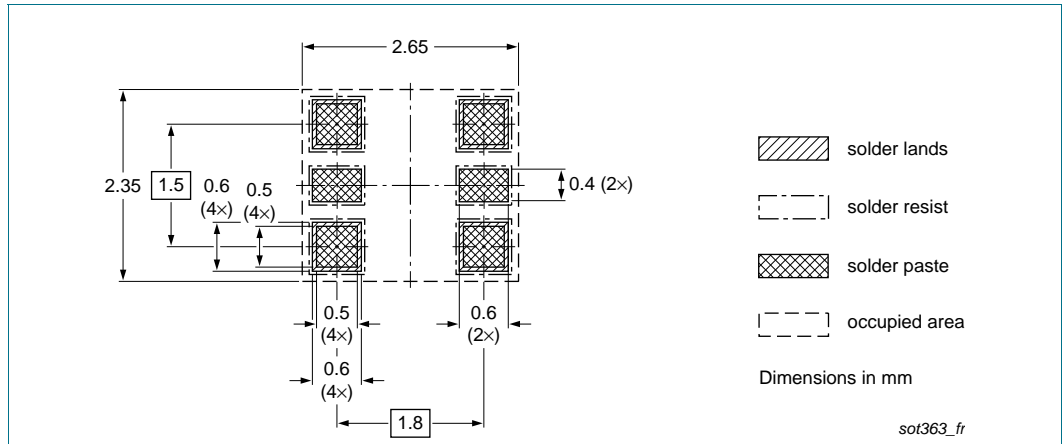


Fig 19. Reflow soldering footprint PUMD12 (SOT363)

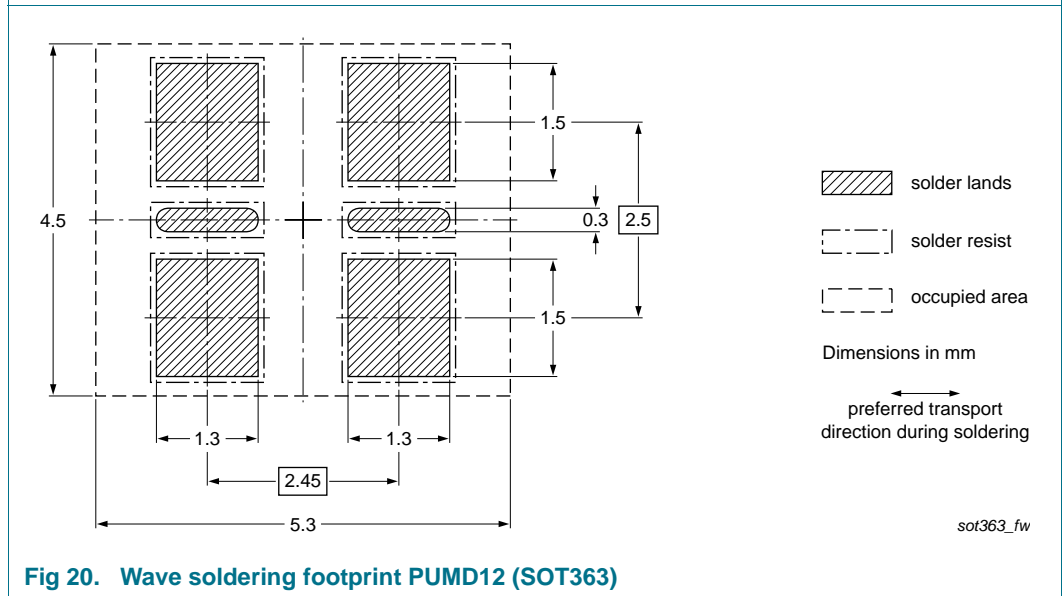


Fig 20. Wave soldering footprint PUMD12 (SOT363)

## 12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PEMD12_PUMD12 v.4	20111121	Product data sheet	-	PEMD12_PUMD12 v.3
Modifications:	<ul style="list-style-type: none"> <li>• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Section 1 "Product profile"</a>: updated</li> <li>• <a href="#">Section 4 "Marking"</a>: updated</li> <li>• <a href="#">Figure 1 to 15</a>: added</li> <li>• <a href="#">Section 6 "Thermal characteristics"</a>: updated</li> <li>• <a href="#">Table 8 "Characteristics"</a>: <math>V_{i(on)}</math> redefined to <math>V_{I(on)}</math> on-state input voltage, <math>V_{i(off)}</math> redefined to <math>V_{I(off)}</math> off-state input voltage, <math>I_{CEO}</math> updated, <math>f_T</math> added</li> <li>• <a href="#">Section 8 "Test information"</a>: added</li> <li>• <a href="#">Section 9 "Package outline"</a>: superseded by minimized package outline drawings</li> <li>• <a href="#">Section 10 "Packing information"</a>: added</li> <li>• <a href="#">Section 11 "Soldering"</a>: added</li> <li>• <a href="#">Section 13 "Legal information"</a>: updated</li> </ul>			
PEMD12_PUMD12 v.3	20031008	Product data sheet	-	PEMD12 v.2
PEMD12 v.2	20011107	Product specification	-	PEMD12 v.1
PEMD12 v.1	20010830	Preliminary specification	-	-
PUMD12 v.2	20010216	Product specification	-	PUMD12 v.1
PUMD12 v.1	19990426	Product specification	-	-

## 13. Legal information

### 13.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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Date of release: 21 November 2011

Document identifier: PEMD12\_PUMD12



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