User's Manual

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RZ/A1H Group

User's Manual: Hardware

Renesas Microcomputer
RZ/A Series

Renesas Electronics
www.renesas.com

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

1. Overview

1.1 Features of This LSI

This LSI is a single-chip microcontroller that includes an ARM Cortex™-A9 processor along with the integrated peripheral functions required to configure a system.

This LSI includes a 32-Kbyte L1 instruction cache, a 32-Kbyte L1 data cache, and a 128-Kbyte L2 cache. This LSI also includes on-chip peripheral functions necessary for system configuration, such as a 10-Mbyte large-capacity RAM (128 Kbytes are shared by the data-retention RAM), data-retention RAM, multi-function timer pulse unit 2, OS timer, realtime clock, serial communication interface with FIFO, serial communication interface, I2C bus interface, serial sound interface, media local bus, SCUX, CAN interface, IEBus™* controller, Renesas SPDIF interface, Renesas serial peripheral interface, SPI multi I/O bus controller, CD-ROM decoder, A/D converter, LIN/UART interface, Ethernet controller, EthernetAVB, NAND flash memory controller, USB 2.0 host/function, digital video decoder, video display controller 5, dynamic range compression, image renderer, image renderer for display, display out comparison unit, OpenVG-compliant Renesas graphics processor, JPEG codec unit, capture engine unit, pixel format converter, sound generator, SD host interface, MMC host interface, motor control PWM timer, interrupt controller modules, and general I/O ports.

The features of this LSI are listed in Table 1.1.

Note: * IEBus (Inter Equipment Bus) is a trademark of Renesas Electronics Corporation.

Table 1.1 RZ/A1H Features

Items	Specification
CPU	• ARM Cortex-A9 processor • Maximum operating frequency: 400 MHz • Instruction cache size: 32 Kbytes • Data cache size: 32 Kbytes • TLB entries: 128 entries • Jazelle architecture extension: Full implementation • Media processing engine with NEON technology
L2 cache memory	• ARM CoreLink™ Level 2 Cache Controller L2C-310 • Operating frequency: 133 MHz • Cache size: 128 Kbytes
Interrupt controller	• ARM PrimeCell® Generic Interrupt Controller (PL390) • External interrupt pins (NMI, IRQ7 to IRQ0, and TINT162 to TINT0) • On-chip peripheral interrupts: Priority level set for each module • 32 priority levels available
Bus state controller	• Address space divided into six areas (0 to 5), each a maximum of 64 Mbytes • The following features settable for each area independently —Bus size (8, 16, or 32 bits): Available sizes depend on the area. —Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas) —Idle wait cycle insertion (between the same area access cycles or different area access cycles) —Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. • Outputs a chip select signal ($\overline{CS0}$ to $\overline{CS5}$) according to the target area ($\overline{CS}$ assert or negate timing can be selected by software) • SDRAM refresh • Auto refresh or self refresh mode selectable • SDRAM burst access
Direct memory access controller	• Sixteen channels; external requests are available for one of them. • Can be activated by on-chip peripheral modules. • A specific DMA transfer interval can be specified to adjust the bus occupancy. • Link mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded.
Clock pulse generator	• Clock mode: Input clock can be selected from external input (EXTAL or USB_X1) or crystal resonator. • Input clock can be multiplied by 32 (max.) by the internal PLL circuit. • Peak values of EMI noise can be reduced by the on-chip SSCG circuit. • Five types of clocks generated: —CPU clock (Iφ): Maximum 400.00 MHz —Image processing clock (Gφ): Maximum 266.67 MHz —Internal bus clock (Bφ): Maximum 133.33 MHz —Peripheral clock 1 (P1φ): Maximum 66.67 MHz —Peripheral clock 0 (P0φ): Maximum 33.33 MHz
Watchdog timer	• On-chip one-channel watchdog timer • A counter overflow can reset the LSI.
Power-down modes	• Four power-down modes provided to reduce the power consumption in this LSI —Sleep mode —Software standby mode —Deep standby mode —Module standby mode

Items	Specification
Multi-function timer pulse unit 2	• Maximum 16 lines of pulse inputs/outputs based on five channels of 16-bit timers • 18 output compare and input capture registers • Input capture function • Pulse output modes • Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Complementary PWM output mode —Non-overlapping waveforms output for 3-phase inverter control —Automatic dead time setting —0% to 100% PWM duty value specifiable —A/D converter start request delaying function —Interrupt skipping at crest or trough • Reset-synchronized PWM mode Three-phase PWM waveforms in positive and negative phases can be output with a required duty value. • Phase counting mode Two-phase encoder pulse counting available
OS timer	• Two-channel 32-bit counters • Two operating modes: —Interval timer mode —Free-running comparison mode • DMA transfer request or interrupt request can be issued when a compare match occurs.
Realtime clock	• Internal clock, calendar function, alarm function • Interrupts can be generated at intervals of 1/64 s by the 32.768-kHz or 4-MHz on-chip crystal oscillator.
Serial communication interface with FIFO	• Eight channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channels 1, 5, and 7 in asynchronous mode)
Serial communication interface	• Two channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable. • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first/MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas serial peripheral interface	• Five channels • SPI operation • Master mode and slave mode selectable • Programmable bit length, clock polarity, and clock phase can be selected. • Consecutive transfers • MSB first/LSB first selectable • Maximum transfer rate: 33.33 Mbps
SPI multi I/O bus controller	• Two channels • Up to two serial flash memories with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • MSB first/LSB first selectable • Maximum transfer rate: 533.33 Mbps (with two serial flash memories connected)
I^2C bus interface	• Four channels • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection

Items	Specification
Serial sound interface	• Six-channel bidirectional serial transfer • Duplex communication (channels 0, 1, 3, and 5) • Support of various serial audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of eight-stage FIFO for transmission and reception • Support of TDM mode • Support of WS continue mode in which the SSIWS signal is not stopped. • Support of direct transfer to the SCUX module • A change of the sampling frequency can be detected.
Media local bus	• MediaLB (OS62400 manufactured by SMSC) for connection with the INIC incorporated. • Conforms with version 2.0 of the MediaLB standard. Data transfer at up to 50 Mbps is possible.
SCUX	• Sampling rate conversion —Asynchronous or synchronous sampling rate conversion is possible. —Sampling rate (synchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input [kHz]: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, or 96 is selectable. Output [kHz]: 8, 16, 24, 44.1, 48, or 96 is selectable. —Sampling rate (asynchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input/output [kHz]: 1 to 96 —Data format: 16 or 24 bits • Digital volume and mute functions —The digital volume can be set within the range from a multiple of 0 to 8 (−120 to 18 dB) —Volume ramping supports soft mute, fade-in, and fade-out. —The zero crossing mute function can apply muting at zero-crossing points. • Mixer —Data of two to four source systems can be mixed (added together) into one system. —The ratio to add the sources can be set. —Direct transfer to the serial sound interface module is supported.
CAN interface	• Five channels • ISO11898-1 compliant • Message buffer: —Up to 64 5-channel receive message buffers: shared among all channels. —16 transmit message buffers per channel
IEBus™ controller	• Conforms with the IEBus protocol (communication modes 1 and 2). • Transfer rates: approximately 17 kbps (in communication mode 1), approximately 26 kbps (in communication mode 2) • Maximum numbers of bytes for transfer: 32 bytes/frame (in communication mode 1), 128 bytes/frame (in communication mode 2) • Operating clock: 8 MHz Note: Input of peripheral clock 0 (P0φ) running at 33.33 MHz is required.
Renesas SPDIF interface	• Support of IEC60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Biphase mark encoding • Double buffered data • Parity encoded serial data • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data.

Items	Specification
CD-ROM decoder	• Support of five formats: Mode 0, mode 1, mode 2, mode 2 form 1, and mode 2 form 2 • Sync codes detection and protection • (Protection: When a sync code is not detected, it is automatically inserted.) • Descrambling • ECC correction —P, Q, PQ, and QP correction —PQ or QP correction can be repeated up to three times. • EDC check Performed before and after ECC • Mode and form are automatically detected. • Link sectors are automatically detected. • Buffering data control Buffering CD-ROM data including Sync code is transferred in specified format, after the data is descrambled, corrected by ECC, and checked by EDC.
LIN/UART interface	• Two channels • Conforms with revisions 1.3, 2.0, 2.1, and 2.2 of the LIN protocol and SAEJ 2062. • Master mode and slave mode selectable
Ethernet controller	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 10 and 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • E-DMAC (Direct Memory Access Controller for Ethernet controller) function
EthernetAVB	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • AVB-DMAC (DMAC dedicated to EthernetAVB) function AVB-DMAC conforms with the following 3 standards; IEEE802.1AS (Clock Synchronization Protocol), IEEE802.1Qav (Realtime Transfer Protocol) and IEEE802.1Qat (Bandwith Reservation Protocol)
NAND flash memory controller	• Direct-connected memory interface with NAND-type flash memory • Read/write in sectors • Two types of transfer modes: Command access mode and sector access mode (512-byte data + 16-byte management code) • Interrupt request and DMA transfer request • Supports flash memory requiring 5-byte addresses (2 Gbits and more)
USB 2.0 host/function module	• Two channels • Conforms to the Universal Serial Bus Specification Revision 2.0 • 480-Mbps, 12-Mbps, and 1.5-Mbps transfer rates provided (host mode) • 480-Mbps and 12-Mbps transfer rates provided (function mode) • On-chip 8-Kbyte RAM as communication buffers

Items	Specification
Digital video decoder	• Two channels • Video input Composite video input (CVBS) • A/D converter for video signal input VIN1 and VIN2 pin input selection Low-pass filter (LPF) Sync tip clamp Programmable gain amplifier (PGA) (0 to 6.021 dB) 10-bit precision pipelined A/D converter • Sync separation Noise reduction LPF, auto level control sync slicer, horizontal auto frequency control (AFC), vertical count-down, interlace detection, auto gain control (AGC)/peak limiter control • Y/C separation NTSC 2D, PAL 2D, and SECAM 1D supported. • Chroma-key decoding NTSC, PAL, and SECAM supported. Color killer, auto color control (ACC), TINT correction, R-Y axis correction • Digital clamp Pedestal clamp (Y), center clamp (Cb/Cr), noise detection • Adjustment of output gain Contrast: 0 to approximately 2 times Color (Cb/Cr independently): 0 to approximately 2 times
Video display controller 5	• Two channels • Video input interface: One channel can be selected from the followings. BT601, BT656 format (NTSC/PAL) input: Input clock: 27 MHz/54 MHz Digital pin input (channel 0): YCbCr422, YCbCr444, RGB888, RGB666, RGB565 Digital pin input size: Maximum input video image size to be set*: 1440 pixels × 1024 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the connected device. Examples of input video image size : WXGA (1280 × 768) XGA (1024 × 768) SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320) Composite video (CVBS) signal input decoded by the digital video decoder • Input video control Horizontal noise reduction (NR), brightness adjustment and contrast adjustment using matrix operation • Scaling control Vertical and horizontal scaling up or down of input video possible at a desired ratio (scaling up of graphics also possible) Scaling up ratio: 1 to 8; scaling down ratio: 1/8 to 1 Interpolation: Hold or linear selectable 2D IP conversion: 2D IP conversion through separately setting the initial phases for the top and bottom fields • Video recording Output pixel format: YCbCr444, YCbCr422, RGB888, RGB565 Output field rate: 1/1, 1/2, 1/4, 1/8 Rotation: Horizontal mirroring and 90/180/270 degree rotation for YCbCr422 and RGB565 Maximum video image size to be stored: ×1 size of input video image • Output video control Black stretch: Black area stretched according to Y signal state Enhancer capability: LTI (transient improvement) and sharpness (contour emphasis) for Y signal

Items	Specification
Video display controller 5	• Four graphics layers (two of them also for input video) Available input pixel formats 1 bit/pixel: CLUT1 4 bits/pixel: CLUT4 8 bits/pixel: CLUT8 16 bits/pixel: YCbCr422 (graphics layers 0 and 1), RGB565, ARGB1555, RGBA5551, ARGB4444 32 bits/pixel: ARGB8888, RGBA8888, RGB888, YCbCr444 (graphics layers 0 and 1) • Blending of two input video images Two input video images superimposed by alpha blending over a rectangular area can be output. • Superimposition Alpha blending in a rectangular area: Input video, layer 1, and layer 2 blended according to the transparency percentage α (fade-in and fade-out function available) Chroma key function: Mixing based on transparency percentage α using the specified RGB and CLUT value Pixel-base alpha blending: Alpha blending for each pixel based on transparency percentage α Generation of output video images Video images superimposed on graphics layers can be output to memory. • Panel output control Panel output correction: Brightness adjustment and contrast adjustment, gamma correction, panel dithering TCON: Various timing output for LCD panel driving provided by a total of seven vertical and horizontal panel driver signals Panel output pixel format: RGB888, RGB666, RGB565, serial RGB Output video image size: Maximum output video image size to be set*: 1999 pixels × 2035 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the display panel. Examples of output video image size: WXGA (1280 × 768) XGA (1024 × 768) SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320)
Dynamic range compression	• Two channels • Contrast adjustment of captured data Contrast expansion processing optimized per region of the image
Image renderer (IMR-LS2)	• Two channels • Refers to the video captured data as two-dimensional texture data and draws a shape by performing texture mapping for an arbitrary shape divided into triangular objects. • Display list system • Drawing functions Texture mapping, bilinear filtering, automatic coordinate generation (and relative coordinate input) • Instruction system Draw instruction: TRI for drawing a triangle Control instructions: TRAP, INT, NOP, SYNCM, SYNCW, WTL, and WTS • Drawing space Destination coordinates: 0 ≤ X ≤ 2,047, 0 ≤ Y ≤ 2,047 Source coordinates: 0 ≤ u ≤ 1,439, 0 ≤ v ≤ 1,023
Image renderer for display (IMR-LSD)	• Refers to the output video image data from the video display controller 5 (channel 0) as two-dimensional texture data and draws shapes by performing texture mapping for an arbitrary shape divided into triangular objects. • Display list system • Drawing functions Texture mapping, bilinear filtering, automatic coordinate generation (and relative coordinate input) • Instruction system Draw instruction: TRI for drawing a triangle Control instructions: TRAP, INT, NOP, SYNCM, SYNCW, WTL, and WTS • Drawing space Destination coordinates: 0 ≤ X ≤ 2,047, 0 ≤ Y ≤ 2,047 Source coordinates: 0 ≤ u ≤ 1,439, 0 ≤ v ≤ 1,023

Items	Specification
Display out comparison unit	• Two channels • Calculates the CRC code of an arbitrary graphics plane and compares it with the pre-calculated CRC code. • Specifies a rectangular area in an arbitrary graphics plane selected from among four graphics planes, one plane of the graphics data obtained after α blending, or one plane of the data read from the output video image generator of the video display controller 5. • Pixel format 32 bits/pixel: ARGB8888/RGB888/RGB666 16 bits/pixel: RGB565
OpenVG-compliant Renesas graphics processor	• OpenVG, which is an open 2D vector graphics API, can be processed. • Processes can be accelerated in OpenVG stage 2 to stage 8 using the dedicated hardware and programmable shader.
JPEG codec unit	• Compression and decompression method conforming to the JPEG baseline standard within the range described in this document. • Operational precision: Conforming to JPEG Part 2, ISO-IEC10918-2 • Pixel format: Compression: YCbCr422 Decompression: YCbCr444, YCbCr422, YCbCr411, YCbCr420 Output pixel format to the buffer: YCbCr422, ARGB8888, RGB565 • Four quantization tables provided • Four Huffman tables provided (two tables for AC coefficients and two tables for DC coefficients) • Markers supported: SOI, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI • Image data rate: Max. 133.33 Mbytes/s (at 66.67-MHz operation)
Capture engine unit	• Examples of input video image size : WXGA (1280 × 768) XGA (1024 × 768) SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320) Note: Depends on the AC characteristics of the connected device. • Input format: 8- or 16-bit YCbCr422 binary data • Memory output format: YCbCr422, YCbCr420 Note: The captured data cannot be displayed via the video display controller 5 because the Y data and CbCr data are split when written to memory.
Pixel format converter	• Two channels • Brightness adjustment, gain adjustment, and YCbCr and RGB mutual conversion. • Input pixel data: RGB888, RGB565, YCbCr422 • Output pixel data: ARGB8888, RGB565, YCbCr422
Sound generator	• Four channels • Capable of adjusting sound volume using 8-bit PWM output • Four types of operating clocks (P0φ/2, P0φ/4, P0φ/8, and P0φ/16) can be selected. • Frequency settings in the 31-Hz to 20-kHz range with precision of 1% or less • Automatic attenuator function can be selected.
SD host interface	• Two channels • SD memory I/O card interface (1-/4-bit SD bus) • Error check function: CRC7 (command), CRC16 (data) • Interrupt requests —Card access interrupt —SDIO access interrupt —Card detect interrupt • DMA transfer requests —SD_BUF write —SD_BUF read • Card detection function, write protect supported
MMC host interface	• Interface to multi-media card (MMC) • Data bus: 1-/4-/8-bit MMC mode • Interrupt requests: card detection, error/time-out, and normal operation • DMA transfer requests: CE_DATA write and CE_DATA read • Card detection function
General I/O ports	• 115 I/Os, 8 inputs with open-drain outputs, and 16 inputs • Input or output can be selected for each bit.

Items	Specification
A/D converter	• 12-/10-bit resolution • Eight input channels • Minimum conversion time: 5.0 µs for 10-bit precision, 20.0 µs for 12-bit precision • A/D conversion request by the external trigger or timer trigger
Motor control PWM timer	• Two 10-bit PWM channels, each with eight outputs
Debugging interface	• ARM CoreSight architecture • JTAG-standard pin assignment
On-chip RAM	• 10-Mbyte large capacity memory for video display/recording and work (128 Kbytes are used for data retention) • 128-Kbyte memory for data retention (16 Kbytes × 2, 32 Kbytes × 1, 64 Kbytes × 1)
Boot modes	• Five boot modes Boot mode 0: Booting from memory (bus width: 16 bits) connected to $\overline{\text{CS0}}$ area Boot mode 1: Booting from memory (bus width: 32 bits) connected to $\overline{\text{CS0}}$ area Boot mode 2: — Boot mode 3: Booting from a serial flash memory Boot mode 4: Booting from a NAND flash memory with SD controller Boot mode 5: Booting from a NAND flash memory with MMC controller
Power supply voltage	• Vcc: 1.10 to 1.26 V • PVcc: 3.0 to 3.6 V
Package	(T.B.D.)

1.2 Product Lineup

(T.B.D)

1.3 Block Diagram

See section 5, LSI Internal Bus.

1.4 Pin Assignment

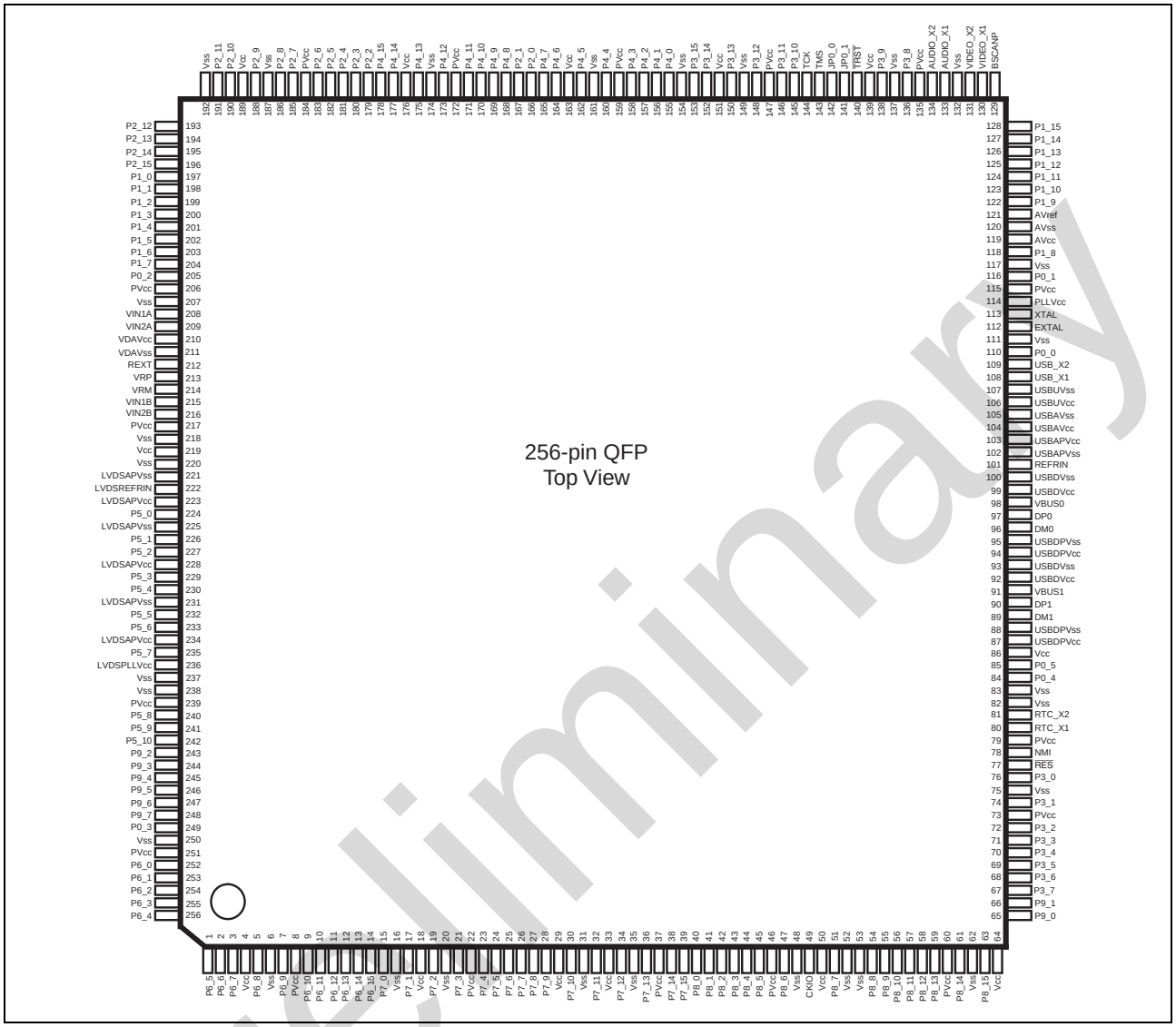
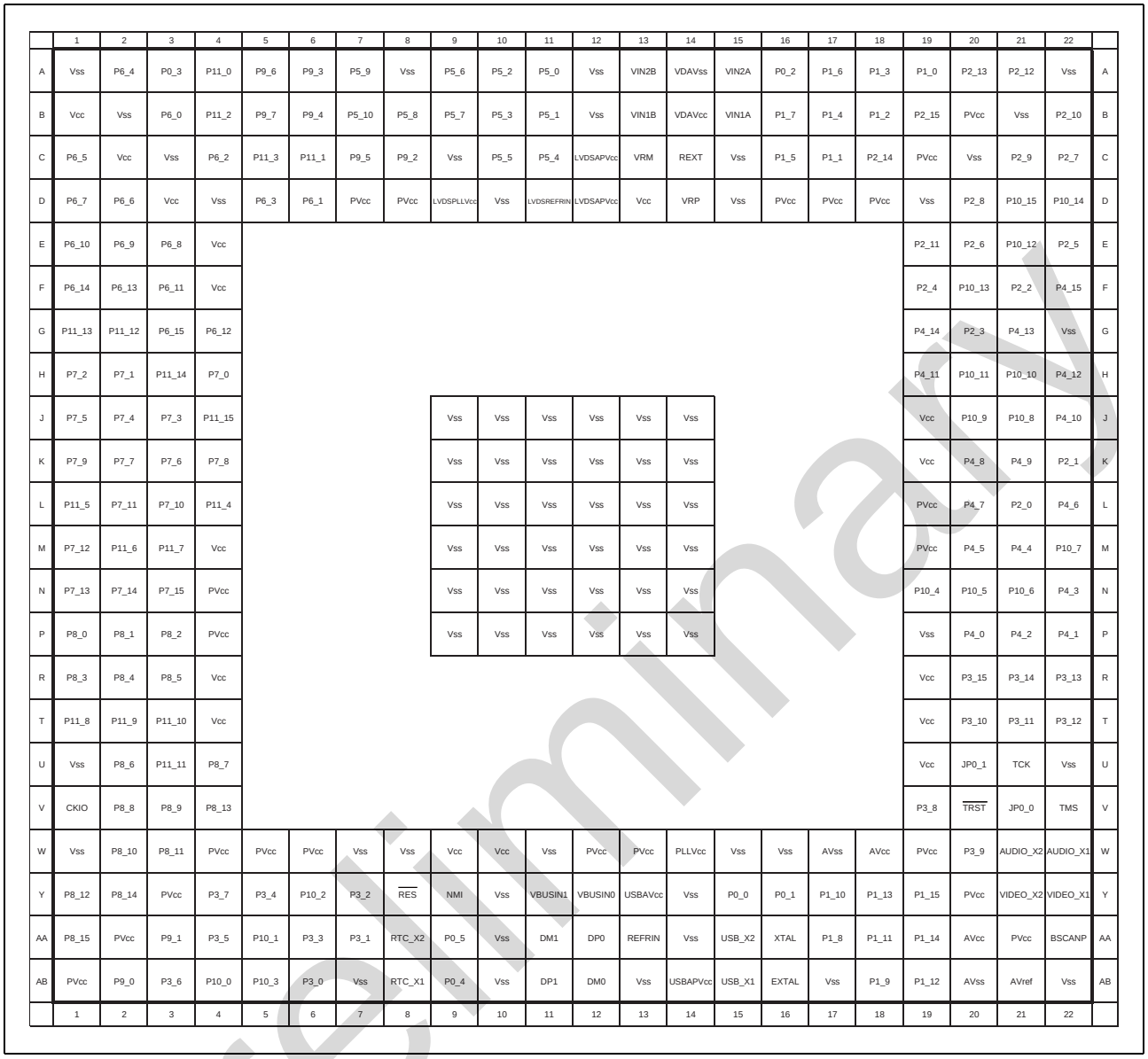


Figure 1.1 Pin Assignment (256-pin, QFP)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	
A	Vss	P6_4	P0_3	P11_0	P9_6	P9_3	P5_9	Vss	P5_6	P5_2	P5_0	Vss	VIN2B	VDAVss	VIN2A	P0_2	P1_6	P1_3	P1_0	P2_13	P2_12	Vss	A
B	Vcc	Vss	P6_0	P11_2	P9_7	P9_4	P5_10	P5_8	P5_7	P5_3	P5_1	Vss	VIN1B	VDAVcc	VIN1A	P1_7	P1_4	P1_2	P2_15	PVcc	Vss	P2_10	B
C	P6_5	Vcc	Vss	P6_2	P11_3	P11_1	P9_5	P9_2	Vss	P5_5	P5_4	LVDSAPVcc	VRM	REXT	Vss	P1_5	P1_1	P2_14	PVcc	Vss	P2_9	P2_7	C
D	P6_7	P6_6	Vcc	Vss	P6_3	P6_1	PVcc	PVcc	LVDSPLLVcc	Vss	LVDSREFRIN	LVDSAPVcc	Vcc	VRP	Vss	PVcc	PVcc	PVcc	Vss	P2_8	P10_15	P10_14	D
E	P6_10	P6_9	P6_8	Vcc															P2_11	P2_6	P10_12	P2_5	E
F	P6_14	P6_13	P6_11	Vcc															P2_4	P10_13	P2_2	P4_15	F
G	P11_13	P11_12	P6_15	P6_12															P4_14	P2_3	P4_13	Vss	G
H	P7_2	P7_1	P11_14	P7_0															P4_11	P10_11	P10_10	P4_12	H
J	P7_5	P7_4	P7_3	P11_15					Vss	Vss	Vss	Vss	Vss	Vss					Vcc	P10_9	P10_8	P4_10	J
K	P7_9	P7_7	P7_6	P7_8					Vss	Vss	Vss	Vss	Vss	Vss					Vcc	P4_8	P4_9	P2_1	K
L	P11_5	P7_11	P7_10	P11_4					Vss	Vss	Vss	Vss	Vss	Vss					PVcc	P4_7	P2_0	P4_6	L
M	P7_12	P11_6	P11_7	Vcc					Vss	Vss	Vss	Vss	Vss	Vss					PVcc	P4_5	P4_4	P10_7	M
N	P7_13	P7_14	P7_15	PVcc					Vss	Vss	Vss	Vss	Vss	Vss					P10_4	P10_5	P10_6	P4_3	N
P	P8_0	P8_1	P8_2	PVcc					Vss	Vss	Vss	Vss	Vss	Vss					Vss	P4_0	P4_2	P4_1	P
R	P8_3	P8_4	P8_5	Vcc															Vcc	P3_15	P3_14	P3_13	R
T	P11_8	P11_9	P11_10	Vcc															Vcc	P3_10	P3_11	P3_12	T
U	Vss	P8_6	P11_11	P8_7															Vcc	JP0_1	TCK	Vss	U
V	CKIO	P8_8	P8_9	P8_13															P3_8	$\overline{\text{TRST}}$	JP0_0	TMS	V
W	Vss	P8_10	P8_11	PVcc	PVcc	PVcc	Vss	Vss	Vcc	Vcc	Vss	PVcc	PVcc	PLLVcc	Vss	Vss	AVss	AVcc	PVcc	P3_9	AUDIO_X2	AUDIO_X1	W
Y	P8_12	P8_14	PVcc	P3_7	P3_4	P10_2	P3_2	$\overline{\text{RES}}$	NMI	Vss	VBUSIN1	VBUSIN0	USBAVcc	Vss	P0_0	P0_1	P1_10	P1_13	P1_15	PVcc	VIDEO_X2	VIDEO_X1	Y
AA	P8_15	PVcc	P9_1	P3_5	P10_1	P3_3	P3_1	RTC_X2	P0_5	Vss	DM1	DP0	REFRIN	Vss	USB_X2	XTAL	P1_8	P1_11	P1_14	AVcc	PVcc	BSCANP	AA
AB	PVcc	P9_0	P3_6	P10_0	P10_3	P3_0	Vss	RTC_X1	P0_4	Vss	DP1	DM0	Vss	USBAPVcc	USB_X1	EXTAL	Vss	P1_9	P1_12	AVss	AVref	Vss	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	

Figure 1.2 Pin Assignment (324-pin, BGA)

1.5 Pin Functions

Table 1.2 Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pins. All the Vcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	Vss	I	Ground	Ground pins. All the Vss pins must be connected to the system power supply (0 V). This LSI does not operate correctly if there is a pin left open.
	PVcc	I	Power supply for I/O circuits	Power supply for I/O pins. All the PVcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	PLLVcc	I	Power supply for PLL	Power supply for the on-chip PLL oscillator.
Clock	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
	CKIO	O	System clock output	Supplies the system clock to external devices.
	AUDIO_CLK	I	External clock for audio	Input pin of external clock for audio. A clock input to the divider is selected from an oscillation clock input on this pin or pins AUDIO_X1 and AUDIO_X2.
	AUDIO_X1	I	Crystal resonator/ external clock for audio	Pins connected to a crystal resonator for audio. An external clock can be input on pin AUDIO_X1. A clock input to the divider is selected from an oscillation clock input on these pins or the AUDIO_CLK pin.
	AUDIO_X2	O		
	AUDIO_XOUT	O	AUDIO_X1 clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal.
	AUDIO_XOUT2	O	AUDIO_X1 divided-by-two clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by two.
	AUDIO_XOUT3	O	AUDIO_X1 divided-by-three clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by three.
Operating mode control	MD_BOOT2, MD_BOOT1, MD_BOOT0	I	Mode set	Sets the operating mode. Do not change the signal levels on these pins while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLK	I	Clock mode set	Sets the clock operating mode. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLKS	I	SSCG clock mode set	Switches the SSCG circuit on or off. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	BSCANP	I	Boundary scan set	Boundary scan setting pin. This pin is set to the high level for a boundary scan and to the low level for normal operation.

Classification	Symbol	I/O	Name	Function
System control	$\overline{\text{RES}}$	I	Power-on reset	This LSI enters the power-on reset state when this signal goes low.
	$\overline{\text{WDTOVF}}$	O	Watchdog timer overflow	Outputs an overflow signal from the watchdog timer.
Interrupts	NMI	I	Non-maskable interrupt	Non-maskable interrupt request pin. It is handled as an FIQ exception. Fix it high when not in use.
	IRQ7 to IRQ0	I	Interrupt requests 7 to 0	Maskable interrupt request pins. Level-input or edge-input detection can be selected. When the edge-input detection is selected, the rising edge, falling edge, or both edges can also be selected.
Address bus	A25 to A0	O	Address bus	Outputs addresses.
Data bus	D31 to D0	I/O	Data bus	Bidirectional data bus.
Bus control	$\overline{\text{CS5}}$ to $\overline{\text{CS0}}$	O	Chip select 5 to 0	Chip-select signals for external memory or devices.
	$\overline{\text{RD}}$	O	Read	Indicates that data is read from an external device.
	RD/$\overline{\text{WR}}$	O	Read/write	Read/write signal.
	$\overline{\text{BS}}$	O	Bus start	Bus-cycle start signal.
	$\overline{\text{AH}}$	O	Address hold	Address hold timing signal for the device that uses the address/data-multiplexed bus.
	$\overline{\text{WAIT}}$	I	Wait	Inserts a wait cycle into the bus cycles during access to the external space.
	$\overline{\text{WE0}}$	O	Byte select	Indicates a write access to bits 7 to 0 of data of external memory or device.
	$\overline{\text{WE1}}$	O	Byte select	Indicates a write access to bits 15 to 8 of data of external memory or device.
	$\overline{\text{WE2}}$	O	Byte select	Indicates a write access to bits 23 to 16 of data of external memory or device.
	$\overline{\text{WE3}}$	O	Byte select	Indicates a write access to bits 31 to 24 of data of external memory or device.
	DQMLL	O	Byte select	Selects bits D7 to D0 when SDRAM is connected.
	DQMLU	O	Byte select	Selects bits D15 to D8 when SDRAM is connected.
	DQMUL	O	Byte select	Selects bits D23 to D16 when SDRAM is connected.
	DQMUU	O	Byte select	Selects bits D31 to D24 when SDRAM is connected.
	$\overline{\text{RAS}}$	O	RAS	Connected to the $\overline{\text{RAS}}$ pin when SDRAM is connected.
	$\overline{\text{CAS}}$	O	CAS	Connected to the $\overline{\text{CAS}}$ pin when SDRAM is connected.
	CKE	O	CK enable	Connected to the CKE pin when SDRAM is connected.
Direct memory access controller	DREQ0	I	DMA-transfer request	Input pin to receive external requests for DMA transfer.
	DACK0	O	DMA-transfer request accept	Output pin for signals indicating acceptance of external requests from external devices.
	TEND0	O	DMA-transfer end output	Output pin for DMA transfer end.

Classification	Symbol	I/O	Name	Function
Multi-function timer pulse unit 2	TCLKA, TCLKB, TCLKC, TCLKD	I	Timer clock input	External clock input pins for the timer.
	TIOC0A, TIOC0B, TIOC0C, TIOC0D	I/O	Input capture/ output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A, TIOC1B	I/O	Input capture/ output compare (channel 1)	The TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins.
	TIOC2A, TIOC2B	I/O	Input capture/ output compare (channel 2)	The TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A, TIOC3B, TIOC3C, TIOC3D	I/O	Input capture/ output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins.
	TIOC4A, TIOC4B, TIOC4C, TIOC4D	I/O	Input capture/ output compare (channel 4)	The TGRA_4 and TGRB_4 input capture input/output compare output/PWM output pins.
Realtime clock	RTC_X1	I	Crystal resonator for realtime clock/ external clock	Connected to 32.768-kHz crystal resonator. The RTC_X1 pin can also be used to input an external clock.
	RTC_X2	O		
	RTC_X3	I	Crystal resonator for realtime clock/ external clock	Connected to 4-MHz crystal resonator. The RTC_X3 pin can also be used to input an external clock.
	RTC_X4	O		
Serial communication interface with FIFO	TxD7 to TxD0	O	Transmit data	Data output pins.
	RxD7 to RxD0	I	Receive data	Data input pins.
	SCK7 to SCK0	I/O	Serial clock	Clock input/output pins.
	$\overline{\text{RTS7}}$, $\overline{\text{RTS5}}$, $\overline{\text{RTS1}}$	O	Transmit request	Modem control pins.
	$\overline{\text{CTS7}}$, $\overline{\text{CTS5}}$, $\overline{\text{CTS1}}$	I	Transmit enable	Modem control pins.
Serial communication interface	SCI_SCK1, SCI_SCK0	I/O	Serial clock	Clock input/output pins.
	SCI_TXD1, SCI_TXD0	O	Transmit data	Data output pins.
	SCI_RXD1, SCI_RXD0	I	Receive data	Data input pins.
	$\overline{\text{SCI\_CTS1}}$/$\overline{\text{RTS1}}$, SCI_CTS0/$\overline{\text{RTS0}}$	I/O	Transmit and receive start control	I/O pins for controlling the start of transmission and reception.
Renesas serial peripheral interface	MOSI4 to MOSI0	I/O	Data	Data I/O pins.
	MISO4 to MISO0	I/O	Data	Data I/O pins.
	RSPCK4 to RSPCK0	I/O	Clock	Clock I/O pins.
	SSL40 to SSL10	I/O	Slave select	Slave select I/O pins.

Classification	Symbol	I/O	Name	Function
SPI multi I/O bus controller	SPBCLK_1, SPBCLK_0	O	Clock	Clock output pins.
	SPBSSL_1, SPBSSL_0	O	Slave select	Slave select output pins.
	SPBMO0_0/SPBIO00_0, SPBMI0_0/SPBIO10_0, SPBIO20_0, SPBIO30_0, SPBMO1_0/SPBIO01_0, SPBMI1_0/SPBIO11_0, SPBIO21_0, SPBIO31_0	I/O	Data	Data I/O pins for channel 0.
	SPBMO0_1/SPBIO00_1, SPBMI0_1/SPBIO10_1, SPBIO20_1, SPBIO30_1, SPBMO1_1/SPBIO01_1, SPBMI1_1/SPBIO11_1, SPBIO21_1, SPBIO31_1	I/O	Data	Data I/O pins for channel 1.
I^2C bus interface	RIIC3SCL to RIIC0SCL	I/O	Serial clock pin	Serial clock I/O pins.
	RIIC3SDA to RIIC0SDA	I/O	Serial data pin	Serial data I/O pins.
Serial sound interface	SSITxD5, SSITxD3, SSITxD1, SSITxD0	O	Data output	Serial data output pin.
	SSIRxD5, SSIRxD3, SSIRxD1, SSIRxD0	I	Data input	Serial data input pin.
	SSIDATA4, SSIDATA2	I/O	Data I/O	Serial data I/O pins.
	SSISCK5 to SSISCK0	I/O	SSI clock I/O	I/O pins for serial clocks.
	SSIWS5 to SSIWS0	I/O	SSI clock LR I/O	I/O pins for word selection.
Media local bus	MLB_CLK	I	Clock input	MediaLB clock input pin.
	MLB_SIG	I/O	Signal information I/O	MediaLB signal information I/O pin.
	MLB_DAT	I/O	Data I/O	MediaLB data I/O pin.
CAN interface	CAN_CLK	I	Clock source for CAN communication	Clock source for CAN communication.
	CAN4TX to CAN0TX	O	CAN bus transmit data	Output pins for transmit data on the CAN bus.
	CAN4RX to CAN0RX	I	CAN bus receive data	Output pins for receive data on the CAN bus.
IEBus™ controller	IETxD	O	IEBus™ controller transmit data	Output pin for transmit data on IEBus™ controller.
	IERxD	I	IEBus™ controller receive data	Input pin for receive data on IEBus™ controller.
Renesas SPDIF interface	SPDIF_OUT	O	Output data	Transmit data output pin.
	SPDIF_IN	I	Input data	Receive data input pin.
LIN/UART interface	RLIN31TX, RLIN30TX	O	Output data	Transmit data output pins.
	RLIN31RX, RLIN30RX	I	Input data	Receive data input pins.

Classification	Symbol	I/O	Name	Function
Ethernet controller, EthernetAVB Note: Regarding the switching of pin functions between Ethernet controller and EthernetAVB, refer to section 54, Ports.	ET_TXCLK	I	Transmit clock	Clock pin for transmission.
	ET_TXEN	O	Transmit enable	Transmit data enable pin
	ET_TXD3 to ET_TXD0	O	Transmit data	MII transmit data pins.
	ET_COL	I	Collision detection	Collision detection pin.
	ET_TXER	O	Transmit error	Transmit error output pin.
	ET_RXCLK	I	Receive clock	Receive clock pin
	ET_RXDV	I	Receive enable	Receive data enable pin
	ET_RXD3 to ET_RXD0	I	Receive data	MII receive data pins.
	ET_RXER	I	Receive error	Receive error input pin.
	ET_CRS	I	Carrier detection	Carrier detection pin.
	ET_MDC	O	Management data clock	Clock pin for information transfer via MDIO.
	ET_MDIO	I/O	Management data I/O	Bidirectional pin for exchange of management data
EthernetAVB	AVB_CAPTURE	I	Timer capture	Capturing input pin for AVTP presentation timer
	AVB_COMP_MATCH	O	Timer compare pulse	Compare pulse output pin for AVTP presentation timer
	AVB_GPTP_EXTERN	I	gPTP timer external clock	External clock pin for gPTP timer
NAND flash memory controller	FALE	O	Flash memory address latch enable	Asserted for address output and negated for data I/O.
	$\overline{\text{FRE}}$	O	Flash memory read enable	Reads data at falling edge.
	$\overline{\text{FCE}}$	O	Flash memory chip enable	Enables the flash memory connected to this LSI.
	FCLE	O	Flash memory command latch enable	Asserted at command output.
	FRB	I	Flash memory ready/ busy	High level indicates ready state and low level indicates busy state.
	$\overline{\text{FWE}}$	O	Flash memory write enable	Flash memory latches commands, addresses, and data at falling edge.
	NAF7 to NAF0	I/O	Flash memory data	Data I/O pins.
USB 2.0 host/ function module	DP1, DP0	I/O	USB 2.0 host/function module D+ data	D+ data pins for USB 2.0 host/function module bus.
	DM1, DM0	I/O	USB 2.0 host/function module D– data	D– data pins for USB 2.0 host/function module bus.
	VBUS1, VBUS0	I	VBUS input	Connected to Vbus on USB 2.0 host/ function module bus.
	REFRIN	I	Reference input	Connected to USBAPVss via 5.6-kΩ ± 1% resistance.

Classification	Symbol	I/O	Name	Function
USB 2.0 host/ function module	USB_X1	I	Crystal resonator/ external clock for USB 2.0 host/function module	Connected to a crystal resonator for USB 2.0 host/function module. An external clock signal may also be input to the USB_X1 pin.
	USB_X2	O		
	USBAPVcc	I	Power supply for transceiver analog pins	Power supply for pins.
	USBAPVss	I	Ground for transceiver analog pins	Ground for pins.
	USBDPVcc	I	Power supply for transceiver digital pins	Power supply for pins.
	USBDPVss	I	Ground for transceiver digital pins	Ground for pins.
	USBAVcc	I	Power supply for transceiver analog core	Power supply for core.
	USBAVss	I	Ground for transceiver analog core	Ground for core.
	USBDVcc	I	Power supply for transceiver digital core	Power supply for core.
	USBDVss	I	Ground for transceiver digital core	Ground for core.
	USBUVcc	I	480-MHz power supply for USB 2.0 host/function module	Power supply for 480-MHz sections
	USBUVss	I	480-MHz ground for USB 2.0 host/function module	Ground for 480-MHz sections
Digital video decoder	VIN1A, VIN2A	I	Composite video signal (CVBS) input	Composite video signal (CVBS) channel 0 input pins.
	VIN1B, VIN2B	I	Composite video signal (CVBS) input	Composite video signal (CVBS) channel 1 input pins.
	VIDEO_X1	I	Crystal resonator/ external clock for digital video decoder	Connected to a crystal resonator for digital video decoder. An external clock signal may also be input to the VIDEO_X1 pin.
	VIDEO_X2	O		
	VRP	O	TOP reference voltage	TOP reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 0.1-µF capacitor.
	VRM	O	BOTTOM reference voltage	BOTTOM reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 0.1-µF capacitor.
	REXT	I	Reference voltage	Reference voltage pin for the A/D converter to input video signals. Connected to VDAVss via 22-kΩ ± 1% resistance.
	VDAVcc	I	Analog power supply	Power supply pin for the A/D converter to input video signals.
	VDAVss	I	Analog ground	Ground pin for the A/D converter to input video signals.

Classification	Symbol	I/O	Name	Function
Video display controller 5	LCD1_DATA23 to LCD1_DATA0, LCD0_DATA23 to LCD0_DATA0	O	Output data	Data output pins for panel.
	LCD1_TCON6 to LCD1_TCON0, LCD0_TCON6 to LCD0_TCON0	O	Panel timing adjustment output	Output pins for panel timing adjustment
	LCD_CLK1, LCD_CLK0	O	Panel clock	Panel clock output pins.
	LCD_EXTCLK1, LCD_EXTCLK0	I	Panel clock source	Panel clock source input pins.
	DV0_DATA23 to DV0_DATA0, DV1_DATA7 to DV1_DATA0	I	Input data	Data input pins for graphics data.
	DV1_VSYNC, DV0_VSYNC	I	VSYNC input	VSYNC input pins.
	DV1_HSYNC, DV0_HSYNC	I	HSYNC input	HSYNC input pins.
	DV1_CLK, DV0_CLK	I	Input clock	Clock input signal pins for graphics data.
LVDS output interface	TXCLKOUTP, TXCLKOUTM	O	Output clock	LVDS differential clock output pins.
	TXOUT2P to TXOUT0P, TXOUT2M to TXOUT0M	O	Output data	LVDS differential data output pins.
	LVDSREFRIN	I	Reference input	Connected to LVDSAPVss via 5.6-kΩ ± 1% resistance.
	LVDSAPVcc	I	LVDS analog power supply	Power supply for LVDS output.
	LVDSAPVss	I	LVDS analog ground	Ground for LVDS output.
	LVDSPLLVcc	I	LVDS PLL power supply	Power supply for LVDS PLL.
Capture engine unit	VIO_D15 to VIO_D0	I	Input data	Graphics data input pins.
	VIO_CLK	I	Input clock	Graphics data clock input pin.
	VIO_VD	I	VSYNC input	VSYNC input pin.
	VIO_HD	I	HSYNC input	HSYNC input pin.
	VIO_FLD	I	FIELD input	Input pin for field information
Sound generator	SGOUT3 to SGOUT0	O	Sound generator output	Sound generator output pins.
SD host interface	SD_CLK_0, SD_CLK_1	O	SD clock	Output pins for SD clock. Only SD_CLK_0 can be used in the RZ/A1H.
	SD_CMD_0, SD_CMD_1	I/O	SD command	SD command output and response input signals. Only SD_CMD_0 can be used in the RZ/A1H.
	SD_D3_0 to SD_D0_0, SD_D3_1 to SD_D0_1	I/O	SD data	SD data bus signals. Only SD_D3_0 to SD_D0_0 can be used in the RZ/A1H.
	SD_CD_0, SD_CD_1	I	SD card detection	SD card detection. Only SD_CD_0 can be used in the RZ/A1H.
	SD_WP_0, SD_WP_1	I	SD write protection	SD write protection signals. Only SD_WP_0 can be used in the RZ/A1H.
MMC host interface	MMC_CLK	O	MMC clock	Output pin for MMC clock.
	MMC_CMD	I/O	MMC command	MMC command output and response input signal.
	MMC_D7 to MMC_D0	I/O	MMC data	MMC data bus signals.
	MMC_CD	I	MMC card detection	MMC card detection.
Motor control PWM timer	PWM1H to PWM1A PWM2H to PWM2A	O	Timer output	PWM output pins.

Classification	Symbol	I/O	Name	Function
A/D converter	AN7 to AN0	I	Analog input pins	Analog input pins. Only AN5 to AN0 can be used in the RZ/A1H.
	$\overline{\text{ADTRG}}$	I	A/D conversion trigger input	External trigger input pin for starting A/D conversion.
	AVcc	I	Analog power supply	Power supply pin for A/D converter.
	AVss	I	Analog ground	Ground pin for A/D converter.
	AVref	I	Analog reference voltage	Reference voltage pin for A/D converter.
General I/O ports	P2_0 to P2_15, P3_0 to P3_15, P4_0 to P4_15, P5_0 to P5_10, P6_0 to P6_15, P7_0 to P7_15, P8_0 to P8_15, P9_0 to P9_15	I/O	General port	General I/O port pins.
	P1_0 to P1_7	I/O	General port	8 input port pins with open-drain output.
	JP0_0, JP0_1, P0_0 to P0_5, P1_8 to P1_15	I	General port	16 general input port pins.
Debugging interface	TCK/SWDCLK	I	Test clock	Test-clock input pin. Also used as the input clock pin for serial wire debugging
	TMS/SWDIO	I, I/O	Test mode select	Test-mode select signal input pin. Also used as the I/O data pin for serial wire debugging
	TDI	I	Test data input	Serial input pin for instructions and data.
	TDO	O	Test data output	Serial output pin for instructions and data.
	$\overline{\text{TRST}}$	I	Test reset	Initialization-signal input pin.
	TRACEDATA3 to TRACEDATA0	O	Data output	Trace data output pins.
	TRACECLK	O	Clock output	Trace clock output pin.
	TRACECTL	O	Enable output	Trace enable output pin.

1.6 List of Pins

Table 1.3 List of Pins (256-pin, QFP)

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
1	P6_5	I(s)/O	—	—	D5	I/O	LCD1_ DATA13	O	CAN2TX	O	—	—	SCK5	I(s)/O	—	—	SSL10	I(s)/O	DV0_ DATA21	O	(T.B.D)
2	P6_6	I(s)/O	—	—	D6	I/O	LCD1_ DATA14	O	—	—	LCD0_ TCON5	O	TxD5	O	—	—	MOSI1	I(s)/O	DV0_ DATA22	O	
3	P6_7	I(s)/O	—	—	D7	I/O	LCD1_ DATA15	O	—	—	LCD0_ TCON6	O	RxD5	I(s)	—	—	MISO1	I(s)/O	DV0_ DATA23	O	
4	Vcc																				
5	P6_8	I(s)/O	—	—	D8	I/O	DV0_ DATA12	I(s)	—	—	CAN_CLK	I(s)	SCK0	I(s)/O	LCD0_ DATA0	O	—	—	IRQ0	I(s)	
6	Vss																				
7	P6_9	I(s)/O	—	—	D9	I/O	DV0_ DATA13	I(s)	—	—	—	—	TxD0	O	LCD0_ DATA1	O	—	—	IRQ1	I(s)	
8	PVcc																				
9	P6_10	I(s)/O	—	—	D10	I/O	DV0_ DATA14	I(s)	—	—	LCD0_ TCON5	O	RxD0	I(s)	LCD0_ DATA2	O	—	—	IRQ2	I(s)	
10	P6_11	I(s)/O	—	—	D11	I/O	DV0_ DATA15	I(s)	—	—	LCD0_ TCON6	O	SCK1	I(s)/O	LCD0_ DATA3	O	—	—	IRQ3	I(s)	
11	P6_12	I(s)/O	—	—	D12	I/O	DV0_ DATA20	I(s)	—	—	—	—	TxD1	O	LCD0_ DATA4	O	—	—	IRQ4	I(s)	
12	P6_13	I(s)/O	—	—	D13	I/O	DV0_ DATA21	I(s)	—	—	SCK6	I(s)/O	RxD1	I(s)	LCD0_ DATA5	O	—	—	IRQ5	I(s)	
13	P6_14	I(s)/O	—	—	D14	I/O	DV0_ DATA22	I(s)	—	—	TxD6	O	—	—	LCD0_ DATA6	O	—	—	IRQ6	I(s)	
14	P6_15	I(s)/O	—	—	D15	I/O	DV0_ DATA23	I(s)	—	—	RxD6	I(s)	—	—	LCD0_ DATA7	O	—	—	IRQ7	I(s)	
15	P7_0	I(s)/O	MD_BOOT2	I(s)	$\overline{CS0}$	O	DV0_ DATA16	I(s)	ET_MDC	O	SCK4	I(s)/O	RLIN30TX	O	—	—	TIOC0A	I(s)/O	—	—	
16	Vss																				
17	P7_1	I(s)/O	—	—	$\overline{CS3}$	O	DV0_ DATA17	I(s)	ET_TXCLK	I(s)	TxD4	O	DV0_CLK	I(s)	SSISCK1	I(s)/O	TIOC0B	I(s)/O	—	—	
18	Vcc																				
19	P7_2	I(s)/O	—	—	$\overline{RAS}$	O	DV0_ DATA18	I(s)	ET_TXER	O	RxD4	I(s)	CAN2RX	I(s)	SSIWS1	I(s)/O	TIOC0C	I(s)/O	—	—	
20	Vss																				
21	P7_3	I(s)/O	—	—	$\overline{CAS}$	O	DV0_ DATA19	I(s)	ET_TXEN	O	SCK7	I(s)/O	CAN2TX	O	SSIRxD1	I(s)	TIOC0D	I(s)/O	—	—	
22	PVcc																				
23	P7_4	I(s)/O	—	—	CKE	O	DV0_ DATA20	I(s)	ET_TXD0	O	TxD7	O	—	—	SSITxD1	O	TIOC1A	I(s)/O	—	—	
24	P7_5	I(s)/O	—	—	RD/$\overline{WR}$	O	DV0_ DATA21	I(s)	ET_TXD1	O	RxD7	I(s)	—	—	SSISCK2	I(s)/O	TIOC1B	I(s)/O	—	—	
25	P7_6	I(s)/O	—	—	$\overline{WE0}$/ DQMLL	O	DV0_ DATA22	I(s)	ET_TXD2	O	$\overline{CTS7}$	I(s)/O	—	—	SSIWS2	I(s)/O	TIOC2A	I(s)/O	—	—	
26	P7_7	I(s)/O	—	—	$\overline{WE1}$/ DQMLU	O	DV0_ DATA23	I(s)	ET_TXD3	O	$\overline{RTS7}$	I(s)/O	—	—	SSIDATA2	I(s)/O	TIOC2B	I(s)/O	—	—	
27	P7_8	I(s)/O	—	—	$\overline{RD}$	O	SSISCK3	I(s)/O	AVB_GPTP_ EXTERN	I	CAN0RX	I(s)	—	—	—	—	TIOC3A	I(s)/O	IRQ1	I(s)	
28	P7_9	I(s)/O	—	—	A1	O	SSIWS3	I(s)/O	ET_RXD0	I(s)	CAN0TX	O	—	—	—	—	TIOC3B	I(s)/O	IRQ0	I(s)	
29	Vcc																				
30	P7_10	I(s)/O	—	—	A2	O	SSIRxD3	I(s)	ET_RXD1	I(s)	CAN1TX	O	—	—	—	—	TIOC3C	I(s)/O	IRQ2	I(s)	
31	Vss																				
32	P7_11	I(s)/O	—	—	A3	O	SSITxD3	O	ET_RXD2	I(s)	CAN1RX	I(s)	—	—	—	—	TIOC3D	I(s)/O	IRQ3	I(s)	
33	Vcc																				
34	P7_12	I(s)/O	—	—	A4	O	SSISCK4	I(s)/O	ET_RXD3	I(s)	—	—	—	—	—	—	TIOC4A	I(s)/O	IRQ4	I(s)	
35	Vss																				
36	P7_13	I(s)/O	—	—	A5	O	SSIWS4	I(s)/O	ET_MDIO	I(s)/O	—	—	—	—	—	—	TIOC4B	I(s)/O	IRQ5	I(s)	
37	PVcc																				
38	P7_14	I(s)/O	—	—	A6	O	SSIDATA4	I(s)/O	ET_CRS	I(s)	—	—	—	—	—	—	TIOC4C	I(s)/O	IRQ6	I(s)	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
39	P7_15	I(s)/O	—	—	A7	O	RSPCK0	I(s)/O	ET_RXCLK	I(s)	$\overline{\text{CTS5}}$	I(s)/O	SCI_TXD0	O	—	—	TIOC4D	I(s)/O	—	—	
40	P8_0	I(s)/O	—	—	A8	O	SSL00	I(s)/O	ET_RXER	I(s)	SCK5	I(s)/O	SCI_SCK0	I(s)/O	—	—	—	—	—	—	(T.B.D)
41	P8_1	I(s)/O	—	—	A9	O	MOSI0	I(s)/O	ET_RXDV	I(s)	TxD5	O	SCI_RXD0	I(s)	—	—	—	—	—	—	
42	P8_2	I(s)/O	—	—	A10	O	MISO0	I(s)/O	AVB_COMP_MATCH	O	RxD5	I(s)	IRQ0	I(s)	—	—	—	—	—	—	
43	P8_3	I(s)/O	—	—	A11	O	DV1_DATA0	I(s)	RSPCK2	I(s)/O	$\overline{\text{RTS5}}$	I(s)/O	—	—	IRQ1	I(s)	SCK2	I(s)/O	—	—	
44	P8_4	I(s)/O	—	—	A12	O	DV1_DATA1	I(s)	SSL20	I(s)/O	—	—			IERxD	I(s)	RxD2	I(s)	—	—	
45	P8_5	I(s)/O	—	—	A13	O	DV1_DATA2	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	—	—	—	—	
46	PVcc																				
47	P8_6	I(s)/O	—	—	A14	O	DV1_DATA3	I(s)	MISO2	I(s)/O	—	—	—	—	IETxD	O	TxD2	O	—	—	
48	Vss																				
49	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
50	Vcc																				
51	P8_7	I(s)/O	—	—	A15	O	DV1_DATA4	I(s)	AUDIO_XOUT	O	IRQ5	I(s)	ET_COL	I(s)	—	—	—	—	—	—	
52	Vss																				
53	Vss																				
54	P8_8	I(s)/O	—	—	A16	O	DV1_DATA5	I(s)	SPBIO00_1	I(s)/O	SPDIF_IN	I(s)	TIOC1A	I(s)/O	PWM1A	O	TxD3	O	SSISCK5	I(s)/O	
55	P8_9	I(s)/O	—	—	A17	O	DV1_DATA6	I(s)	SPBIO10_1	I(s)/O	SPDIF_OUT	O	TIOC1B	I(s)/O	PWM1B	O	RxD3	I(s)	SSIWS5	I(s)/O	
56	P8_10	I(s)/O	—	—	A18	O	DV1_DATA7	I(s)	SPBIO20_1	I(s)/O	TIOC3A	I(s)/O	CAN4TX	O	PWM1C	O	SGOUT_0	O	SSITxD5	O	
57	P8_11	I(s)/O	—	—	A19	O	—	—	SPBIO30_1	I(s)/O	TIOC3B	I(s)/O	RxD5	I(s)	PWM1D	O	SGOUT_1	O	DV0_CLK	I(s)	
58	P8_12	I(s)/O	—	—	A20	O	—	—	SPBCLK_1	O	TIOC3C	I(s)/O	SCK5	I(s)/O	PWM1E	O	SGOUT_2	O	SSISCK4	I(s)/O	
59	P8_13	I(s)/O	—	—	A21	O	—	—	SPBSSL_1	O	TIOC3D	I(s)/O	TxD5	O	PWM1F	O	SGOUT_3	O	SSIWS4	I(s)/O	
60	PVcc																				
61	P8_14	I(s)/O	—	—	A22	O	SPBIO01_0	I(s)/O	SPBIO00_1	I(s)/O	TIOC2A	I(s)/O	RSPCK2	I(s)/O	PWM1G	O	TxD4	O	SSIDATA4	I(s)/O	
62	Vss																				
63	P8_15	I(s)/O	—	—	A23	O	SPBIO11_0	I(s)/O	SPBIO10_1	I(s)/O	TIOC2B	I(s)/O	SSL20	I(s)/O	PWM1H	O	RxD4	I(s)	—	—	
64	Vcc																				
65	P9_0	I(s)/O	—	—	A24	O	SPBIO21_0	I(s)/O	CAN0TX	O	TCLKC	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	
66	P9_1	I(s)/O	—	—	A25	O	SPBIO31_0	I(s)/O	CAN0RX	I(s)	IRQ0	I(s)	MISO2	I(s)/O	—	—	—	—	—	—	
67	P3_7	I(s)/O	—	—	LCD0_TCON6	O	—	—	SSITxD1	O	LCD1_EXTCLK	I(s)	$\overline{\text{SCI_CTS0}}$/ $\overline{\text{RTS0}}$	I(s)/O	TIOC3D	I(s)/O	$\overline{\text{CS1}}$	O	$\overline{\text{WDTOVF}}$	O	
68	P3_6	I(s)/O	—	—	LCD0_TCON5	O	ET_RXDV	I(s)	SSIRxD1	I(s)	—	—	SCI_RXD0	I(s)	TIOC3C	I(s)/O	RxD3	I(s)	—	—	
69	P3_5	I(s)/O	—	—	LCD0_TCON4	O	ET_RXER	I(s)	SSIWS1	I(s)/O	AUDIO_XOUT3	O	SCI_TXD0	O	TIOC3B	I(s)/O	TxD3	O	—	—	
70	P3_4	I(s)/O	—	—	LCD0_TCON3	O	ET_RXCLK	I(s)	SSISCK1	I(s)/O	AUDIO_XOUT2	O	SCI_SCK0	I(s)/O	TIOC3A	I(s)/O	SCK3	I(s)/O	—	—	
71	P3_3	I(s)/O	—	—	LCD0_TCON2	O	ET_MDIO	I(s)/O	IRQ4	I(s)	$\overline{\text{BS}}$	O	$\overline{\text{SCI_CTS1}}$/ $\overline{\text{RTS1}}$	I(s)/O	DACK0	O	PWM2D	O	MISO3	I(s)/O	
72	P3_2	I(s)/O	—	—	LCD0_TCON1	O	ET_TXEN	O	—	—	RxD2	I(s)	SCI_RXD1	I(s)	TEND0	O	PWM2C	O	MOSI3	I(s)/O	
73	PVcc																				
74	P3_1	I(s)/O	—	—	LCD0_TCON0	O	ET_TXER	O	IRQ6	I(s)	TxD2	O	SCI_TXD1	O	AUDIO_CLK	I(s)	PWM2B	O	SSL30	I(s)/O	
75	Vss																				
76	P3_0	I(s)/O	—	—	LCD0_CLK	O	ET_TXCLK	I(s)	IRQ2	I(s)	SCK2	I(s)/O	SCI_SCK1	I(s)/O	TxD2	O	PWM2A	O	RSPCK3	I(s)/O	
77	$\overline{\text{RES}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
78	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
79	PVcc																				
80	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
81	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
82	Vss																				
83	Vss																				(T.B.D)
84	P0_4	I(s)	—	—	RTC_X3	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
85	P0_5	I(s)	—	—	RTC_X4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
86	Vcc																				
87	USBDPVcc																				
88	USBDPVss																				
89	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
90	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
91	VBUS1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
92	USBDVcc																				
93	USBDVss																				
94	USBDPVcc																				
95	USBDPVss																				
96	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
97	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
98	VBUS0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
99	USBDVcc																				
100	USBDVss																				
101	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
102	USBAPVss																				
103	USBAPVcc																				
104	USBAVcc																				
105	USBAVss																				
106	USBUVcc																				
107	USBUVss																				
108	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
109	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
110	P0_0	I(s)	MD_BOOT0	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
111	Vss																				
112	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
113	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
114	PLLVcc																				
115	PVcc																				
116	P0_1	I(s)	MD_BOOT1	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
117	Vss																				
118	P1_8	I(s)	—	—	AN0	I(a)	—	—	IRQ2	I(s)	DREQ0	I(s)	VIO_D14	I(s)	DV0_ DATA14	I(s)	—	—	—	—	
119	AVcc																				
120	AVss																				
121	AVref																				
122	P1_9	I(s)	—	—	AN1	I(a)	—	—	IRQ3	I(s)	—	—	VIO_D15	I(s)	DV0_ DATA15	I(s)	—	—	—	—	
123	P1_10	I(s)	—	—	AN2	I(a)	—	—	IRQ4	I(s)	TCLKB	I(s)	—	—	—	—	—	—	—	—	
124	P1_11	I(s)	—	—	AN3	I(a)	—	—	IRQ5	I(s)	TCLKD	I(s)	—	—	—	—	—	—	—	—	
125	P1_12	I(s)	—	—	AN4	I(a)	DV0_ VSYNC	I(s)	—	—	VIO_FLD	I(s)	—	—	—	—	—	—	—	—	
126	P1_13	I(s)	—	—	AN5	I(a)	DV0_ HSYNC	I(s)	—	—	$\overline{\text{WAIT}}$	I(s)	—	—	—	—	—	—	—	—	
127	P1_14	I(s)	—	—	AN6	I(a)	—	—	—	—	ET_COL	I(s)	—	—	—	—	—	—	—	—	
128	P1_15	I(s)	—	—	AN7	I(a)	—	—	—	—	AVB_ CAPTURE	I	—	—	—	—	—	—	—	—	
129	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
130	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
131	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
132	Vss																				
133	AUDIO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(T.B.D)
134	AUDIO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
135	PVcc																				
136	P3_8	I(s)/O	—	—	LCD0_ DATA0	O	—	—	NAF0	I(s)/O	—	—	TRACE DATA0	O	TIOC4A	I(s)/O	SD_CD_1	I(s)	MMC_CD	I(s)	
137	Vss																				
138	P3_9	I(s)/O	—	—	LCD0_ DATA1	O	—	—	NAF1	I(s)/O	—	—	TRACE DATA1	O	TIOC4B	I(s)/O	SD_WP_1	I(s)	IRQ6	I(s)	
139	Vcc																				
140	$\overline{\text{TRST}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
141	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
142	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
143	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
144	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
145	P3_10	I(s)/O	—	—	LCD0_ DATA2	O	—	—	NAF2	I(s)/O	—	—	TRACE DATA2	O	TIOC4C	I(s)/O	SD_D1_1	I(s)/O	MMC_D1	I(s)/O	
146	P3_11	I(s)/O	—	—	LCD0_ DATA3	O	—	—	NAF3	I(s)/O	—	—	TRACE DATA3	O	TIOC4D	I(s)/O	SD_D0_1	I(s)/O	MMC_D0	I(s)/O	
147	PVcc																				
148	P3_12	I(s)/O	—	—	LCD0_ DATA4	O	—	—	NAF4	I(s)/O	—	—	—	—	—	—	SD_CLK_1	O	MMC_CLK	O	
149	Vss																				
150	P3_13	I(s)/O	—	—	LCD0_ DATA5	O	—	—	NAF5	I(s)/O	AUDIO_ XOUT	O	—	—	—	—	SD_CMD_1	I(s)/O	MMC_CMD	I(s)/O	
151	Vcc																				
152	P3_14	I(s)/O	—	—	LCD0_ DATA6	O	—	—	NAF6	I(s)/O	—	—	TRACECLK	O	—	—	SD_D3_1	I(s)/O	MMC_D3	I(s)/O	
153	P3_15	I(s)/O	—	—	LCD0_ DATA7	O	—	—	NAF7	I(s)/O	—	—	TRACECTL	O	—	—	SD_D2_1	I(s)/O	MMC_D2	I(s)/O	
154	Vss																				
155	P4_0	I(s)/O	—	—	LCD0_ DATA8	O	TIOC0A	I(s)/O	$\overline{\text{FRE}}$	O	—	—	—	—	—	—	RSPCK4	I(s)/O	MMC_D4	I(s)/O	
156	P4_1	I(s)/O	—	—	LCD0_ DATA9	O	TIOC0B	I(s)/O	FCLE	O	—	—	SCK2	I(s)/O	—	—	SSL40	I(s)/O	MMC_D5	I(s)/O	
157	P4_2	I(s)/O	—	—	LCD0_ DATA10	O	TIOC0C	I(s)/O	FALE	O	CAN3RX	I(s)	TxD2	O	—	—	MOSI4	I(s)/O	MMC_D6	I(s)/O	
158	P4_3	I(s)/O	—	—	LCD0_ DATA11	O	TIOC0D	I(s)/O	FWE	O	CAN3TX	O	RxD2	I(s)	—	—	MISO4	I(s)/O	MMC_D7	I(s)/O	
159	PVcc																				
160	P4_4	I(s)/O	—	—	LCD0_ DATA12	O	RSPCK1	I(s)/O	TIOC4A	I(s)/O	PWM2E	O	SSISCK0	I(s)/O	—	—	DV0_ DATA12	I(s)	—	—	
161	Vss																				
162	P4_5	I(s)/O	—	—	LCD0_ DATA13	O	SSL10	I(s)/O	TIOC4B	I(s)/O	PWM2F	O	SSIWS0	I(s)/O	—	—	DV0_ DATA13	I(s)	—	—	
163	Vcc																				
164	P4_6	I(s)/O	—	—	LCD0_ DATA14	O	MOSI1	I(s)/O	TIOC4C	I(s)/O	PWM2G	O	SSIRxD0	I(s)	—	—	DV0_ DATA14	I(s)	—	—	
165	P4_7	I(s)/O	—	—	LCD0_ DATA15	O	MISO1	I(s)/O	TIOC4D	I(s)/O	PWM2H	O	SSITxD0	O	—	—	DV0_ DATA15	I(s)	—	—	
166	P2_0	I(s)/O	—	—	D16	I/O	ET_TXCLK	I(s)	DV0_DATA0	I(s)	SPBIO00_1	I(s)/O	MLB_CLK	I(s)	IRQ5	I(s)	VIO_D0	I(s)	LCD0_ DATA16	O	
167	P2_1	I(s)/O	—	—	D17	I/O	ET_TXER	O	DV0_DATA1	I(s)	SPBIO10_1	I(s)/O	MLB_DAT	I(s)/O	TIOC2A	I(s)/O	VIO_D1	I(s)	LCD0_ DATA17	O	
168	P4_8	I(s)/O	—	—	LCD0_ DATA16	O	LCD1_ TCON3	O	SD_CD_0	I(s)	MMC_CD	I(s)	SSISCK5	I(s)/O	CAN2TX	O	SCK0	I(s)/O	IRQ0	I(s)	
169	P4_9	I(s)/O	—	—	LCD0_ DATA17	O	LCD1_ TCON4	O	SD_WP_0	I(s)	—	—	SSIWS5	I(s)/O	CAN2RX	I(s)	TxD0	O	IRQ1	I(s)	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
170	P4_10	I(s)/O	—	—	LCD0_ DATA18	O	LCD1_ TCON5	O	SD_D1_0	I(s)/O	MMC_D1	I(s)/O	SSIRxD5	I(s)	—	—	RxD0	I(s)	IRQ2	I(s)	
171	P4_11	I(s)/O	—	—	LCD0_ DATA19	O	LCD1_ TCON6	O	SD_D0_0	I(s)/O	MMC_D0	I(s)/O	SSITxD5	O	CAN4TX	O	SCK1	I(s)/O	IRQ3	I(s)	
172	PVcc																				
173	P4_12	I(s)/O	—	—	LCD0_ DATA20	O	LCD1_CLK	O	SD_CLK_0	O	MMC_CLK	O	SPBIO01_1	I(s)/O	SSISCK3	I(s)/O	TxD1	O	IRQ4	I(s)	(T.B.D)
174	Vss																				
175	P4_13	I(s)/O	—	—	LCD0_ DATA21	O	LCD1_ TCON0	O	SD_CMD_0	I(s)/O	MMC_CMD	I(s)/O	SPBIO11_1	I(s)/O	SSIWS3	I(s)/O	RxD1	I(s)	IRQ5	I(s)	
176	Vcc																				
177	P4_14	I(s)/O	—	—	LCD0_ DATA22	O	LCD1_ TCON1	O	SD_D3_0	I(s)/O	MMC_D3	I(s)/O	SPBIO21_1	I(s)/O	SSIRxD3	I(s)	TxD2	O	IRQ6	I(s)	
178	P4_15	I(s)/O	—	—	LCD0_ DATA23	O	LCD1_ TCON2	O	SD_D2_0	I(s)/O	MMC_D2	I(s)/O	SPBIO31_1	I(s)/O	SSITxD3	O	RxD2	I(s)	IRQ7	I(s)	
179	P2_2	I(s)/O	—	—	D18	I/O	ET_TXEN	O	DV0_DATA2	I(s)	SPBIO20_1	I(s)/O	MLB_SIG	I(s)/O	TIOC2B	I(s)/O	VIO_D2	I(s)	LCD0_ DATA18	O	
180	P2_3	I(s)/O	—	—	D19	I/O	ET_CRS	I(s)	DV0_DATA3	I(s)	SPBIO30_1	I(s)/O	IERxD	I(s)	$\overline{\text{CTS1}}$	I(s)/O	VIO_D3	I(s)	LCD0_ DATA19	O	
181	P2_4	I(s)/O	—	—	D20	I/O	ET_TXD0	O	DV0_DATA4	I(s)	SSISCK5	I(s)/O	SPBCLK_1	O	SCK1	I(s)/O	VIO_D4	I(s)	LCD0_ DATA20	O	
182	P2_5	I(s)/O	—	—	D21	I/O	ET_TXD1	O	DV0_DATA5	I(s)	SSIWS5	I(s)/O	SPBSSL_1	O	TxD1	O	VIO_D5	I(s)	LCD0_ DATA21	O	
183	P2_6	I(s)/O	—	—	D22	I/O	ET_TXD2	O	DV0_DATA6	I(s)	SSIRxD5	I(s)	—	—	RxD1	I(s)	VIO_D6	I(s)	LCD0_ DATA22	O	
184	PVcc																				
185	P2_7	I(s)/O	—	—	D23	I/O	ET_TXD3	O	DV0_DATA7	I(s)	SSITxD5	O	IETxD	O	$\overline{\text{RTS1}}$	I(s)/O	VIO_D7	I(s)	LCD0_ DATA23	O	
186	P2_8	I(s)/O	—	—	D24	I/O	ET_RXD0	I(s)	DV0_DATA8	I(s)	SSISCK0	I(s)/O	LCD0_ TCON6	O	LCD1_ DATA8	O	VIO_D8	I(s)	RSPCK4	I(s)/O	
187	Vss																				
188	P2_9	I(s)/O	—	—	D25	I/O	ET_RXD1	I(s)	DV0_DATA9	I(s)	SSIWS0	I(s)/O	RLIN30RX	I(s)	LCD1_ DATA9	O	VIO_D9	I(s)	SSL40	I(s)/O	
189	Vcc																				
190	P2_10	I(s)/O	—	—	D26	I/O	ET_RXD2	I(s)	DV0_ DATA10	I(s)	SSIRxD0	I(s)	RLIN30TX	O	LCD1_ DATA10	O	VIO_D10	I(s)	MOSI4	I(s)/O	
191	P2_11	I(s)/O	—	—	D27	I/O	ET_RXD3	I(s)	DV0_ DATA11	I(s)	SSITxD0	O	TIOC1A	I(s)/O	LCD1_ DATA11	O	VIO_D11	I(s)	MISO4	I(s)/O	
192	Vss																				
193	P2_12	I(s)/O	—	—	D28	I/O	RSPCK0	I(s)/O	DV0_ DATA12	I(s)	SPBIO01_0	I(s)/O	CAN3RX	I(s)	IRQ6	I(s)	LCD1_ DATA12	O	TIOC1B	I(s)/O	
194	P2_13	I(s)/O	—	—	D29	I/O	SSL00	I(s)/O	DV0_ DATA13	I(s)	SPBIO11_0	I(s)/O	CAN3TX	O	SCK0	I(s)/O	LCD1_ DATA13	O	IRQ7	I(s)	
195	P2_14	I(s)/O	—	—	D30	I/O	MOSI0	I(s)/O	DV0_ DATA14	I(s)	SPBIO21_0	I(s)/O	CAN4RX	I(s)	TxD0	O	LCD1_ DATA14	O	IRQ0	I(s)	
196	P2_15	I(s)/O	—	—	D31	I/O	MISO0	I(s)/O	DV0_ DATA15	I(s)	SPBIO31_0	I(s)/O	CAN_CLK	I(s)	RxD0	I(s)	LCD1_ DATA15	O	IRQ1	I(s)	
197	P1_0	I(s)/ O(o)	—	—	RIIC0SCL	I(s)/ O(o)	DV0_ DATA16	I(s)	TCLKA	I(s)	IRQ0	I(s)	VIO_VD	I(s)	DV0_ VSYNC	I(s)	—	—	—	—	
198	P1_1	I(s)/ O(o)	—	—	RIIC0SDA	I(s)/ O(o)	DV0_ DATA17	I(s)	TCLKC	I(s)	IRQ1	I(s)	VIO_HD	I(s)	DV0_ HSYNC	I(s)	—	—	—	—	
199	P1_2	I(s)/ O(o)	—	—	RIIC1SCL	I(s)/ O(o)	DV0_ DATA18	I(s)	FRB	I(s)	IRQ2	I(s)	—	—	—	—	LCD1_ EXTCLK	I(s)	—	—	
200	P1_3	I(s)/ O(o)	—	—	RIIC1SDA	I(s)/ O(o)	DV0_ DATA19	I(s)	ET_COL	I(s)	IRQ3	I(s)	$\overline{\text{ADTRG}}$	I(s)	—	—	—	—	—	—	
201	P1_4	I(s)/ O(o)	—	—	RIIC2SCL	I(s)/ O(o)	DV0_CLK	I(s)	CAN1RX	I(s)	IRQ4	I(s)	—	—	—	—	CAN_CLK	I(s)	—	—	
202	P1_5	I(s)/ O(o)	—	—	RIIC2SDA	I(s)/ O(o)	DV1_CLK	I(s)	CAN4RX	I(s)	IRQ5	I(s)	VIO_CLK	I(s)	—	—	LCD1_ EXTCLK	I(s)	—	—	
203	P1_6	I(s)/ O(o)	—	—	RIIC3SCL	I(s)/ O(o)	DV1_ VSYNC	I(s)	IERxD	I(s)	IRQ6	I(s)	VIO_D12	I(s)	DV0_ DATA12	I(s)	—	—	—	—	
204	P1_7	I(s)/ O(o)	—	—	RIIC3SDA	I(s)/ O(o)	DV1_ HSYNC	I(s)	RLIN30RX	I(s)	IRQ7	I(s)	VIO_D13	I(s)	DV0_ DATA13	I(s)	—	—	—	—	
205	P0_2	I(s)	MD_CLK	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
206	PVcc																				
207	Vss																				
208	VIN1A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
209	VIN2A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
210	VDAVcc																				
211	VDAVss																				(T.B.D)
212	REXT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
213	VRP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
214	VRM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
215	VIN1B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
216	VIN2B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
217	PVcc																				
218	Vss																				
219	Vcc																				
220	Vss																				
221	LVDSAPVss																				
222	LVDSREFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
223	LVDSAPVcc																				
224	P5_0	I(s)/O	—	—	TXCLKOUTP	O	LCD1_DATA0	O	LCD0_DATA16	O	DV1_DATA0	I(s)	TxD4	O	TIOC0A	I(s)/O	—	—	RSPCK3	I(s)/O	
225	LVDSAPVss																				
226	P5_1	I(s)/O	—	—	TXCLKOUTM	O	LCD1_DATA1	O	LCD0_DATA17	O	DV1_DATA1	I(s)	RxD4	I(s)	TIOC0B	I(s)/O	—	—	SSL30	I(s)/O	
227	P5_2	I(s)/O	—	—	TXOUT2P	O	LCD1_DATA2	O	LCD0_DATA18	O	DV1_DATA2	I(s)	SCK3	I(s)/O	TIOC1B	I(s)/O	—	—	MOSI3	I(s)/O	
228	LVDSAPVcc																				
229	P5_3	I(s)/O	—	—	TXOUT2M	O	LCD1_DATA3	O	LCD0_DATA19	O	DV1_DATA3	I(s)	TxD3	O	TIOC3C	I(s)/O	—	—	MISO3	I(s)/O	
230	P5_4	I(s)/O	—	—	TXOUT1P	O	LCD1_DATA4	O	LCD0_DATA20	O	DV1_DATA4	I(s)	RxD3	I(s)	TIOC3D	I(s)/O	—	—	DV0_DATA12	I(s)	
231	LVDSAPVss																				
232	P5_5	I(s)/O	—	—	TXOUT1M	O	LCD1_DATA5	O	LCD0_DATA21	O	DV1_DATA5	I(s)	AUDIO_XOUT	O	TIOC0C	I(s)/O	$\overline{FCE}$	O	DV0_DATA13	I(s)	
233	P5_6	I(s)/O	—	—	TXOUT0P	O	LCD1_DATA6	O	LCD0_DATA22	O	DV1_DATA6	I(s)	TxD6	O	IRQ6	I(s)	SPDIF_IN	I(s)	DV0_DATA14	I(s)	
234	LVDSAPVcc																				
235	P5_7	I(s)/O	—	—	TXOUT0M	O	LCD1_DATA7	O	LCD0_DATA23	O	DV1_DATA7	I(s)	RxD6	I(s)	TIOC0D	I(s)/O	SPDIF_OUT	O	DV0_DATA15	I(s)	
236	LVDSPLLVcc																				
237	Vss																				
238	Vss																				
239	PVcc																				
240	P5_8	I(s)/O	—	—	LCD0_EXTCLK	I(s)	IRQ0	I(s)	DV1_CLK	I(s)	—	—	DV0_CLK	I(s)	$\overline{CS2}$	O	—	—	—	—	
241	P5_9	I(s)/O	—	—	$\overline{WE2}$/DQMUL	O	ET_MDC	O	DV0_VSYNC	I(s)	IRQ2	I(s)	CAN1RX	I(s)	IERxD	I(s)	LCD1_DATA16	O	—	—	
242	P5_10	I(s)/O	—	—	$\overline{WE3}$/DQMUU/$\overline{AH}$	O	—	—	DV0_HSYNC	I(s)	—	—	CAN1TX	O	IETxD	O	LCD1_DATA17	O	—	—	
243	P9_2	I(s)/O	—	—	LCD1_DATA18	O	SPBCLK_0	O	RLIN30TX	O	SCK1	I(s)/O	A0	O	—	—	—	—	—	—	
244	P9_3	I(s)/O	—	—	LCD1_DATA19	O	SPBSSL_0	O	—	—	TxD1	O	—	—	—	—	—	—	—	—	
245	P9_4	I(s)/O	—	—	LCD1_DATA20	O	SPBIO00_0	I(s)/O	—	—	RxD1	I(s)	—	—	—	—	—	—	—	—	
246	P9_5	I(s)/O	—	—	LCD1_DATA21	O	SPBIO10_0	I(s)/O	SSISCK2	I(s)/O	$\overline{CTS1}$	I(s)/O	$\overline{CS4}$	O	—	—	—	—	—	—	
247	P9_6	I(s)/O	—	—	LCD1_DATA22	O	SPBIO20_0	I(s)/O	SSIWS2	I(s)/O	$\overline{RTS1}$	I(s)/O	$\overline{CS5}$	O	—	—	—	—	—	—	

No.	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram Figure 1.3
	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	
248	P9_7	I(s)/O	—	—	LCD1_ DATA23	O	SPBIO30_0	I(s)/O	SSIDATA2	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	—	—	
249	P0_3	I(s)	MD_CLKS	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
250	Vss																				
251	PVcc																				
252	P6_0	I(s)/O	—	—	D0	I/O	LCD1_ DATA8	O	RLIN30RX	I(s)	DV0_CLK	I(s)	TIOC1A	I(s)/O	IRQ5	I(s)	RxD3	I(s)	DV0_ DATA16	I(s)	(T.B.D)
253	P6_1	I(s)/O	—	—	D1	I/O	LCD1_ DATA9	O	RLIN30TX	O	IRQ4	I(s)	TIOC1B	I(s)/O	SSIDATA4	I(s)/O	TxD3	O	DV0_ DATA17	I(s)	
254	P6_2	I(s)/O	—	—	D2	I/O	LCD1_ DATA10	O	RLIN31RX	I(s)	IRQ7	I(s)	TCLKA	I(s)	TIOC2A	I(s)/O	RxD2	I(s)	DV0_ DATA18	I(s)	
255	P6_3	I(s)/O	—	—	D3	I/O	LCD1_ DATA11	O	RLIN31TX	O	IRQ2	I(s)	$\overline{\text{CTS5}}$	I(s)/O	TIOC2B	I(s)/O	TxD2	O	DV0_ DATA19	I(s)	
256	P6_4	I(s)/O	—	—	D4	I/O	LCD1_ DATA12	O	CAN2RX	I(s)	IRQ3	I(s)	$\overline{\text{RTS5}}$	I(s)/O	—	—	RSPCK1	I(s)/O	DV0_ DATA20	I(s)	

[Legend]
(s):Schmitt
(a):Analog
(o):Open drain

Table 1.4 List of Pins (324-pin, BGA)

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
1	A1	Vss																			
2	A2	P6_4	I(s)/O	—	—	D4	I/O	LCD1_ DATA12	O	CAN2RX	I(s)	IRQ3	I(s)	$\overline{\text{RTS5}}$	I(s)/O	—	—	RSPCK1	I(s)/O	DV0_ DATA20	I(s)
3	A3	P0_3	I(s)	MD_ CLKS	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
4	A4	P11_0	I(s)/O	—	—	DV0_ DATA12	I(s)	TIOC4A	I(s)/O	—	—	SCK6	I(s)/O	LCD0_ DATA7	O	VIO_D12	I(s)	—	—	—	—
5	A5	P9_6	I(s)/O	—	—	LCD1_ DATA22	O	SPBIO 20_0	I(s)/O	SSIWS2	I(s)/O	$\overline{\text{RTS1}}$	I(s)/O	$\overline{\text{CS5}}$	O	—	—	—	—	—	—
6	A6	P9_3	I(s)/O	—	—	LCD1_ DATA19	O	SPBSSL _0	O	—	—	TxD1	O	—	—	—	—	—	—	—	—
7	A7	P5_9	I(s)/O	—	—	$\overline{\text{WE2}}$/ DQMUL	O	ET_ MDC	O	DV0_ VSYNC	I(s)	IRQ2	I(s)	CAN1RX	I(s)	IERxD	I(s)	LCD1_ DATA16	O	—	—
8	A8	Vss																			
9	A9	P5_6	I(s)/O	—	—	TXOUT 0P	O	LCD1_ DATA6	O	LCD0_ DATA22	O	DV1_ DATA6	I(s)	TxD6	O	IRQ6	I(s)	SPDIF_ IN	I(s)	DV0_ DATA14	I(s)
10	A10	P5_2	I(s)/O	—	—	TXOUT 2P	O	LCD1_ DATA2	O	LCD0_ DATA18	O	DV1_ DATA2	I(s)	SCK3	I(s)/O	TIOC1B	I(s)/O	—	—	MOSI3	I(s)/O
11	A11	P5_0	I(s)/O	—	—	TXCLK OUTP	O	LCD1_ DATA0	O	LCD0_ DATA16	O	DV1_ DATA0	I(s)	TxD4	O	TIOC0A	I(s)/O	—	—	RSPCK3	I(s)/O
12	A12	Vss																			
13	A13	VIN2B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	A14	VDAVss																			
15	A15	VIN2A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	A16	P0_2	I(s)	MD_CLK	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
17	A17	P1_6	I(s)/O(o)	—	—	RIIC3 SCL	I(s)/O(o)	DV1_ VSYNC	I(s)	IERxD	I(s)	IRQ6	I(s)	VIO_D12	I(s)	DV0_ DATA12	I(s)	—	—	—	—
18	A18	P1_3	I(s)/O(o)	—	—	RIIC1 SDA	I(s)/O(o)	DV0_ DATA19	I(s)	ET_ COL	I(s)	IRQ3	I(s)	$\overline{\text{ADTRG}}$	I(s)	—	—	—	—	—	—
19	A19	P1_0	I(s)/O(o)	—	—	RIIC0 SCL	I(s)/O(o)	DV0_ DATA16	I(s)	TCLKA	I(s)	IRQ0	I(s)	VIO_VD	I(s)	DV0_ VSYNC	I(s)	—	—	—	—
20	A20	P2_13	I(s)/O	—	—	D29	I/O	SSL00	I(s)/O	DV0_ DATA13	I(s)	SPBIO 11_0	I(s)/O	CAN3TX	O	SCK0	I(s)/O	LCD1_ DATA13	O	IRQ7	I(s)
21	A21	P2_12	I(s)/O	—	—	D28	I/O	RSPCK0	I(s)/O	DV0_ DATA12	I(s)	SPBIO 01_0	I(s)/O	CAN3RX	I(s)	IRQ6	I(s)	LCD1_ DATA12	O	TIOC1B	I(s)/O
22	A22	Vss																			
23	B1	Vcc																			
24	B2	Vss																			
25	B3	P6_0	I(s)/O	—	—	D0	I/O	LCD1_ DATA8	O	RLIN30 RX	I(s)	DV0_ CLK	I(s)	TIOC1A	I(s)/O	IRQ5	I(s)	RxD3	I(s)	DV0_ DATA16	I(s)
26	B4	P11_2	I(s)/O	—	—	DV0_ DATA14	I(s)	TIOC4C	I(s)/O	—	—	RxD6	I(s)	LCD0_ DATA5	O	VIO_D14	I(s)	—	—	—	—
27	B5	P9_7	I(s)/O	—	—	LCD1_ DATA23	O	SPBIO 30_0	I(s)/O	SSI DATA2	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	—	—
28	B6	P9_4	I(s)/O	—	—	LCD1_ DATA20	O	SPBIO 00_0	I(s)/O	—	—	RxD1	I(s)	—	—	—	—	—	—	—	—
29	B7	P5_10	I(s)/O	—	—	$\overline{\text{WE3}}$/ DQMUU/ AH	O	—	—	DV0_ HSYNC	I(s)	—	—	CAN1TX	O	IETxD	O	LCD1_ DATA17	O	—	—
30	B8	P5_8	I(s)/O	—	—	LCD0_ EXTCLK	I(s)	IRQ0	I(s)	DV1_ CLK	I(s)	—	—	DV0_ CLK	I(s)	$\overline{\text{CS2}}$	O	—	—	—	—
31	B9	P5_7	I(s)/O	—	—	TXOUT 0M	O	LCD1_ DATA7	O	LCD0_ DATA23	O	DV1_ DATA7	I(s)	RxD6	I(s)	TIOC0D	I(s)/O	SPDIF_ OUT	O	DV0_ DATA15	I(s)
32	B10	P5_3	I(s)/O	—	—	TXOUT 2M	O	LCD1_ DATA3	O	LCD0_ DATA19	O	DV1_ DATA3	I(s)	TxD3	O	TIOC3C	I(s)/O	—	—	MISO3	I(s)/O
33	B11	P5_1	I(s)/O	—	—	TXCLK OUTM	O	LCD1_ DATA1	O	LCD0_ DATA17	O	DV1_ DATA1	I(s)	RxD4	I(s)	TIOC0B	I(s)/O	—	—	SSL30	I(s)/O
34	B12	Vss																			

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
35	B13	VIN1B	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
36	B14	VDAVcc																			
37	B15	VIN1A	I(a)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
38	B16	P1_7	I(s)/O(o)	—	—	RIIC3 SDA	I(s)/O(o)	DV1_ HSYNC	I(s)	RLIN30 RX	I(s)	IRQ7	I(s)	VIO_D13	I(s)	DV0_ DATA13	I(s)	—	—	—	—
39	B17	P1_4	I(s)/O(o)	—	—	RIIC2 SCL	I(s)/O(o)	DV0_ CLK	I(s)	CAN1RX	I(s)	IRQ4	I(s)	—	—	—	—	CAN_ CLK	I(s)	—	—
40	B18	P1_2	I(s)/O(o)	—	—	RIIC1 SCL	I(s)/O(o)	DV0_ DATA18	I(s)	FRB	I(s)	IRQ2	I(s)	—	—	—	—	LCD1_ EXTCLK	I(s)	—	—
41	B19	P2_15	I(s)/O	—	—	D31	I/O	MISO0	I(s)/O	DV0_ DATA15	I(s)	SPBIO 31_0	I(s)/O	CAN_ CLK	I(s)	RxD0	I(s)	LCD1_ DATA15	O	IRQ1	I(s)
42	B20	PVcc																			
43	B21	Vss																			
44	B22	P2_10	I(s)/O	—	—	D26	I/O	ET_ RXD2	I(s)	DV0_ DATA10	I(s)	SSIRxD0	I(s)	RLIN30 TX	O	LCD1_ DATA10	O	VIO_D10	I(s)	MOSI4	I(s)/O
45	C1	P6_5	I(s)/O	—	—	D5	I/O	LCD1_ DATA13	O	CAN2TX	O	—	—	SCK5	I(s)/O	—	—	SSL10	I(s)/O	DV0_ DATA21	O
46	C2	Vcc																			
47	C3	Vss																			
48	C4	P6_2	I(s)/O	—	—	D2	I/O	LCD1_ DATA10	O	RLIN31 RX	I(s)	IRQ7	I(s)	TCLKA	I(s)	TIOC2A	I(s)/O	RxD2	I(s)	DV0_ DATA18	I(s)
49	C5	P11_3	I(s)/O	—	—	DV0_ DATA15	I(s)	TIOC4D	I(s)/O	—	—	—	—	LCD0_ DATA4	O	VIO_D15	I(s)	—	—	—	—
50	C6	P11_1	I(s)/O	—	—	DV0_ DATA13	I(s)	TIOC4B	I(s)/O	—	—	TxD6	O	LCD0_ DATA6	O	VIO_D13	I(s)	—	—	—	—
51	C7	P9_5	I(s)/O	—	—	LCD1_ DATA21	O	SPBIO 10_0	I(s)/O	SSISCK 2	I(s)/O	$\overline{\text{CTS1}}$	I(s)/O	$\overline{\text{CS4}}$	O	—	—	—	—	—	—
52	C8	P9_2	I(s)/O	—	—	LCD1_ DATA18	O	SPBCLK _0	O	RLIN30 TX	O	SCK1	I(s)/O	A0	O	—	—	—	—	—	—
53	C9	Vss																			
54	C10	P5_5	I(s)/O	—	—	TXOUT 1M	O	LCD1_ DATA5	O	LCD0_ DATA21	O	DV1_ DATA5	I(s)	AUDIO_ XOUT	O	TIOC0C	I(s)/O	$\overline{\text{FCE}}$	O	DV0_ DATA13	I(s)
55	C11	P5_4	I(s)/O	—	—	TXOUT 1P	O	LCD1_ DATA4	O	LCD0_ DATA20	O	DV1_ DATA4	I(s)	RxD3	I(s)	TIOC3D	I(s)/O	—	—	DV0_ DATA12	I(s)
56	C12	LVDS APVcc																			
57	C13	VRM	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58	C14	REXT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
59	C15	Vss																			
60	C16	P1_5	I(s)/O(o)	—	—	RIIC2 SDA	I(s)/O(o)	DV1_ CLK	I(s)	CAN4RX	I(s)	IRQ5	I(s)	VIO_ CLK	I(s)	—	—	LCD1_ EXTCLK	I(s)	—	—
61	C17	P1_1	I(s)/O(o)	—	—	RIIC0 SDA	I(s)/O(o)	DV0_ DATA17	I(s)	TCLKC	I(s)	IRQ1	I(s)	VIO_HD	I(s)	DV0_ HSYNC	I(s)	—	—	—	—
62	C18	P2_14	I(s)/O	—	—	D30	I/O	MOSI0	I(s)/O	DV0_ DATA14	I(s)	SPBIO 21_0	I(s)/O	CAN4RX	I(s)	TxD0	O	LCD1_ DATA14	O	IRQ0	I(s)
63	C19	PVcc																			
64	C20	Vss																			
65	C21	P2_9	I(s)/O	—	—	D25	I/O	ET_ RXD1	I(s)	DV0_ DATA9	I(s)	SSIWS0	I(s)/O	RLIN30 RX	I(s)	LCD1_ DATA9	O	VIO_D9	I(s)	SSL40	I(s)/O
66	C22	P2_7	I(s)/O	—	—	D23	I/O	ET_ TXD3	O	DV0_ DATA7	I(s)	SSITxD5	O	IETxD	O	$\overline{\text{RTS1}}$	I(s)/O	VIO_D7	I(s)	LCD0_ DATA23	O
67	D1	P6_7	I(s)/O	—	—	D7	I/O	LCD1_ DATA15	O	—	—	LCD0_ TCON6	O	RxD5	I(s)	—	—	MISO1	I(s)/O	DV0_ DATA23	O
68	D2	P6_6	I(s)/O	—	—	D6	I/O	LCD1_ DATA14	O	—	—	LCD0_ TCON5	O	TxD5	O	—	—	MOSI1	I(s)/O	DV0_ DATA22	O
69	D3	Vcc																			
70	D4	Vss																			

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
71	D5	P6_3	I(s)/O	—	—	D3	I/O	LCD1_ DATA11	O	RLIN31 TX	O	IRQ2	I(s)	$\overline{\text{CTS5}}$	I(s)/O	TIOC2B	I(s)/O	TxD2	O	DV0_ DATA19	I(s)
72	D6	P6_1	I(s)/O	—	—	D1	I/O	LCD1_ DATA9	O	RLIN30 TX	O	IRQ4	I(s)	TIOC1B	I(s)/O	SSI DATA4	I(s)/O	TxD3	O	DV0_ DATA17	I(s)
73	D7	PVcc																			
74	D8	PVcc																			
75	D9	LVDS PLLVcc																			
76	D10	Vss																			
77	D11	LVDS REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
78	D12	LVDS APVcc																			
79	D13	Vcc																			
80	D14	VRP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
81	D15	Vss																			
82	D16	PVcc																			
83	D17	PVcc																			
84	D18	PVcc																			
85	D19	Vss																			
86	D20	P2_8	I(s)/O	—	—	D24	I/O	ET_ RXD0	I(s)	DV0_ DATA8	I(s)	SSISCK 0	I(s)/O	LCD0_ TCON6	O	LCD1_ DATA8	O	VIO_D8	I(s)	RSPCK4	I(s)/O
87	D21	P10_15	I(s)/O	—	—	DV0_ DATA11	I(s)	SSITxD1	O	—	—	MISO0	I(s)/O	LCD0_ DATA8	O	VIO_D11	I(s)	—	—	—	—
88	D22	P10_14	I(s)/O	—	—	DV0_ DATA10	I(s)	SSIRxD1	I(s)	—	—	MOSI0	I(s)/O	LCD0_ DATA9	O	VIO_D10	I(s)	—	—	—	—
89	E1	P6_10	I(s)/O	—	—	D10	I/O	DV0_ DATA14	I(s)	—	—	LCD0_ TCON5	O	RxD0	I(s)	LCD0_ DATA2	O	—	—	IRQ2	I(s)
90	E2	P6_9	I(s)/O	—	—	D9	I/O	DV0_ DATA13	I(s)	—	—	—	—	TxD0	O	LCD0_ DATA1	O	—	—	IRQ1	I(s)
91	E3	P6_8	I(s)/O	—	—	D8	I/O	DV0_ DATA12	I(s)	—	—	CAN_ CLK	I(s)	SCK0	I(s)/O	LCD0_ DATA0	O	—	—	IRQ0	I(s)
92	E4	Vcc																			
93	E19	P2_11	I(s)/O	—	—	D27	I/O	ET_ RXD3	I(s)	DV0_ DATA11	I(s)	SSITxD0	O	TIOC1A	I(s)/O	LCD1_ DATA11	O	VIO_D11	I(s)	MISO4	I(s)/O
94	E20	P2_6	I(s)/O	—	—	D22	I/O	ET_ TXD2	O	DV0_ DATA6	I(s)	SSIRxD5	I(s)	—	—	RxD1	I(s)	VIO_D6	I(s)	LCD0_ DATA22	O
95	E21	P10_12	I(s)/O	—	—	DV0_ DATA8	I(s)	SSISCK 1	I(s)/O	—	—	RSPCK0	I(s)/O	LCD0_ DATA11	O	VIO_D8	I(s)	—	—	—	—
96	E22	P2_5	I(s)/O	—	—	D21	I/O	ET_ TXD1	O	DV0_ DATA5	I(s)	SSIWS5	I(s)/O	SPBSSL _1	O	TxD1	O	VIO_D5	I(s)	LCD0_ DATA21	O
97	F1	P6_14	I(s)/O	—	—	D14	I/O	DV0_ DATA22	I(s)	—	—	TxD6	O	—	—	LCD0_ DATA6	O	—	—	IRQ6	I(s)
98	F2	P6_13	I(s)/O	—	—	D13	I/O	DV0_ DATA21	I(s)	—	—	SCK6	I(s)/O	RxD1	I(s)	LCD0_ DATA5	O	—	—	IRQ5	I(s)
99	F3	P6_11	I(s)/O	—	—	D11	I/O	DV0_ DATA15	I(s)	—	—	LCD0_ TCON6	O	SCK1	I(s)/O	LCD0_ DATA3	O	—	—	IRQ3	I(s)
100	F4	Vcc																			
101	F19	P2_4	I(s)/O	—	—	D20	I/O	ET_ TXD0	O	DV0_ DATA4	I(s)	SSISCK 5	I(s)/O	SPBCLK _1	O	SCK1	I(s)/O	VIO_D4	I(s)	LCD0_ DATA20	O
102	F20	P10_13	I(s)/O	—	—	DV0_ DATA9	I(s)	SSIWS1	I(s)/O	—	—	SSL00	I(s)/O	LCD0_ DATA10	O	VIO_D9	I(s)	—	—	—	—
103	F21	P2_2	I(s)/O	—	—	D18	I/O	ET_ TXEN	O	DV0_ DATA2	I(s)	SPBIO 20_1	I(s)/O	MLB_ SIG	I(s)/O	TIOC2B	I(s)/O	VIO_D2	I(s)	LCD0_ DATA18	O
104	F22	P4_15	I(s)/O	—	—	LCD0_ DATA23	O	LCD1_ TCON2	O	SD_ D2_0	I(s)/O	MMC_ D2	I(s)/O	SPBIO 31_1	I(s)/O	SSITxD3	O	RxD2	I(s)	IRQ7	I(s)
105	G1	P11_13	I(s)/O	—	—	CAN1TX	O	SSL10	I(s)/O	LCD0_ TCON4	O	MMC_ D5	I(s)/O	LCD0_ TCON1	O	—	—	—	—	—	—

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
106	G2	P11_12	I(s)/O	—	—	CAN1RX	I(s)	RSPCK1	I(s)/O	IRQ3	I(s)	MMC_ D4	I(s)/O	LCD0_ TCON2	O	—	—	—	—	—	—
107	G3	P6_15	I(s)/O	—	—	D15	I/O	DV0_ DATA23	I(s)	—	—	RxD6	I(s)	—	—	LCD0_ DATA7	O	—	—	IRQ7	I(s)
108	G4	P6_12	I(s)/O	—	—	D12	I/O	DV0_ DATA20	I(s)	—	—	—	—	TxD1	O	LCD0_ DATA4	O	—	—	IRQ4	I(s)
109	G19	P4_14	I(s)/O	—	—	LCD0_ DATA22	O	LCD1_ TCON1	O	SD_ D3_0	I(s)/O	MMC_ D3	I(s)/O	SPBIO 21_1	I(s)/O	SSIRxD3	I(s)	TxD2	O	IRQ6	I(s)
110	G20	P2_3	I(s)/O	—	—	D19	I/O	ET_ CRS	I(s)	DV0_ DATA3	I(s)	SPBIO 30_1	I(s)/O	IERxD	I(s)	$\overline{\text{CTS1}}$	I(s)/O	VIO_D3	I(s)	LCD0_ DATA19	O
111	G21	P4_13	I(s)/O	—	—	LCD0_ DATA21	O	LCD1_ TCON0	O	SD_ CMD_0	I(s)/O	MMC_ CMD	I(s)/O	SPBIO 11_1	I(s)/O	SSIWS3	I(s)/O	RxD1	I(s)	IRQ5	I(s)
112	G22	Vss																			
113	H1	P7_2	I(s)/O	—	—	$\overline{\text{RAS}}$	O	DV0_ DATA18	I(s)	ET_ TXER	O	RxD4	I(s)	CAN2RX	I(s)	SSIWS1	I(s)/O	TIOC0C	I(s)/O	—	—
114	H2	P7_1	I(s)/O	—	—	$\overline{\text{CS3}}$	O	DV0_ DATA17	I(s)	ET_ TXCLK	I(s)	TxD4	O	DV0_ CLK	I(s)	SSISCK 1	I(s)/O	TIOC0B	I(s)/O	—	—
115	H3	P11_14	I(s)/O	—	—	SPDIF_ IN	I(s)	MOSI1	I(s)/O	LCD0_ TCON5	O	MMC_ D6	I(s)/O	LCD0_ TCON0	O	—	—	—	—	—	—
116	H4	P7_0	I(s)/O	MD_ BOOT2	I(s)	$\overline{\text{CS0}}$	O	DV0_ DATA16	I(s)	ET_ MDC	O	SCK4	I(s)/O	RLIN30 TX	O	—	—	TIOC0A	I(s)/O	—	—
117	H19	P4_11	I(s)/O	—	—	LCD0_ DATA19	O	LCD1_ TCON6	O	SD_ D0_0	I(s)/O	MMC_ D0	I(s)/O	SSITxD5	O	CAN4TX	O	SCK1	I(s)/O	IRQ3	I(s)
118	H20	P10_11	I(s)/O	—	—	DV0_ DATA7	I(s)	TIOC2B	I(s)/O	—	—	ET_ RXD3	I(s)	LCD0_ DATA12	O	VIO_D7	I(s)	—	—	—	—
119	H21	P10_10	I(s)/O	—	—	DV0_ DATA6	I(s)	TIOC2A	I(s)/O	—	—	ET_ RXD2	I(s)	LCD0_ DATA13	O	VIO_D6	I(s)	—	—	—	—
120	H22	P4_12	I(s)/O	—	—	LCD0_ DATA20	O	LCD1_ CLK	O	SD_ CLK_0	O	MMC_ CLK	O	SPBIO 10_1	I(s)/O	SSISCK 3	I(s)/O	TxD1	O	IRQ4	I(s)
121	J1	P7_5	I(s)/O	—	—	RD/$\overline{\text{WR}}$	O	DV0_ DATA21	I(s)	ET_ TXD1	O	RxD7	I(s)	—	—	SSISCK 2	I(s)/O	TIOC1B	I(s)/O	—	—
122	J2	P7_4	I(s)/O	—	—	CKE	O	DV0_ DATA20	I(s)	ET_ TXD0	O	TxD7	O	—	—	SSITxD1	O	TIOC1A	I(s)/O	—	—
123	J3	P7_3	I(s)/O	—	—	$\overline{\text{CAS}}$	O	DV0_ DATA19	I(s)	ET_ TXEN	O	SCK7	I(s)/O	CAN2TX	O	SSIRxD1	I(s)	TIOC0D	I(s)/O	—	—
124	J4	P11_15	I(s)/O	—	—	SPDIF_ OUT	O	MISO1	I(s)/O	IRQ1	I(s)	MMC_ D7	I(s)/O	LCD0_ CLK	O	—	—	—	—	—	—
125	J9	Vss																			
126	J10	Vss																			
127	J11	Vss																			
128	J12	Vss																			
129	J13	Vss																			
130	J14	Vss																			
131	J19	Vcc																			
132	J20	P10_9	I(s)/O	—	—	DV0_ DATA5	I(s)	TIOC1B	I(s)/O	—	—	ET_ RXD1	I(s)	LCD0_ DATA14	O	VIO_D5	I(s)	—	—	—	—
133	J21	P10_8	I(s)/O	—	—	DV0_ DATA4	I(s)	TIOC1A	I(s)/O	—	—	ET_ RXD0	I(s)	LCD0_ DATA15	O	VIO_D4	I(s)	—	—	—	—
134	J22	P4_10	I(s)/O	—	—	LCD0_ DATA18	O	LCD1_ TCON5	O	SD_ D1_0	I(s)/O	MMC_ D1	I(s)/O	SSIRxD5	I(s)	—	—	RxD0	I(s)	IRQ2	I(s)
135	K1	P7_9	I(s)/O	—	—	A1	O	SSIWS3	I(s)/O	ET_ RXD0	I(s)	CAN0TX	O	—	—	—	—	TIOC3B	I(s)/O	IRQ0	I(s)
136	K2	P7_7	I(s)/O	—	—	$\overline{\text{WE1}}$/ DQMLU	O	DV0_ DATA23	I(s)	ET_ TXD3	O	$\overline{\text{RTS7}}$	I(s)/O	—	—	SSI DATA2	I(s)/O	TIOC2B	I(s)/O	—	—
137	K3	P7_6	I(s)/O	—	—	$\overline{\text{WE0}}$/ DQMLL	O	DV0_ DATA22	I(s)	ET_ TXD2	O	$\overline{\text{CTS7}}$	I(s)/O	—	—	SSIWS2	I(s)/O	TIOC2A	I(s)/O	—	—
138	K4	P7_8	I(s)/O	—	—	$\overline{\text{RD}}$	O	SSISCK 3	I(s)/O	AVB_ COMP_ MATCH	O	CAN0RX	I(s)	—	—	—	—	TIOC3A	I(s)/O	IRQ1	I(s)
139	K9	Vss																			

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
140	K10	Vss																			
141	K11	Vss																			
142	K12	Vss																			
143	K13	Vss																			
144	K14	Vss																			
145	K19	Vcc																			
146	K20	P4_8	I(s)/O	—	—	LCD0_ DATA16	O	LCD1_ TCON3	O	SD_ CD_0	I(s)	MMC_ CD	I(s)	SSISCK 5	I(s)/O	CAN2TX	O	SCK0	I(s)/O	IRQ0	I(s)
147	K21	P4_9	I(s)/O	—	—	LCD0_ DATA17	O	LCD1_ TCON4	O	SD_ WP_0	I(s)	—	—	SSIWS5	I(s)/O	CAN2RX	I(s)	TxD0	O	IRQ1	I(s)
148	K22	P2_1	I(s)/O	—	—	D17	I/O	ET_ TXER	O	DV0_ DATA1	I(s)	SPBIO 10_1	I(s)/O	MLB_ DAT	I(s)/O	TIOC2A	I(s)/O	VIO_D1	I(s)	LCD0_ DATA17	O
149	L1	P11_5	I(s)/O	—	—	DV0_ DATA17	I(s)	SD_ WP_0	I(s)	SSIWS4	I(s)/O	—	—	LCD0_ DATA2	O	—	—	—	—	—	—
150	L2	P7_11	I(s)/O	—	—	A3	O	SSITxD3	O	ET_ RXD2	I(s)	CAN1RX	I(s)	—	—	—	—	TIOC3D	I(s)/O	IRQ3	I(s)
151	L3	P7_10	I(s)/O	—	—	A2	O	SSIRxD3	I(s)	ET_ RXD1	I(s)	CAN1TX	O	—	—	—	—	TIOC3C	I(s)/O	IRQ2	I(s)
152	L4	P11_4	I(s)/O	—	—	DV0_ DATA16	I(s)	SD_ CD_0	I(s)	SSISCK 4	I(s)/O	MMC_ CD	I(s)	LCD0_ DATA3	O	—	—	—	—	—	—
153	L9	Vss																			
154	L10	Vss																			
155	L11	Vss																			
156	L12	Vss																			
157	L13	Vss																			
158	L14	Vss																			
159	L19	PVcc																			
160	L20	P4_7	I(s)/O	—	—	LCD0_ DATA15	O	MISO1	I(s)/O	TIOC4D	I(s)/O	PWM2H	O	SSITxD0	O	—	—	DV0_ DATA15	I(s)	—	—
161	L21	P2_0	I(s)/O	—	—	D16	I/O	ET_ TXCLK	I(s)	DV0_ DATA0	I(s)	SPBIO 00_1	I(s)/O	MLB_ CLK	I(s)	IRQ5	I(s)	VIO_D0	I(s)	LCD0_ DATA16	O
162	L22	P4_6	I(s)/O	—	—	LCD0_ DATA14	O	MOSI1	I(s)/O	TIOC4C	I(s)/O	PWM2G	O	SSIRxD0	I(s)	—	—	DV0_ DATA14	I(s)	—	—
163	M1	P7_12	I(s)/O	—	—	A4	O	SSISCK 4	I(s)/O	ET_ RXD3	I(s)	—	—	—	—	—	—	TIOC4A	I(s)/O	IRQ4	I(s)
164	M2	P11_6	I(s)/O	—	—	DV0_ DATA18	I(s)	SD_ D1_0	I(s)/O	SSI DATA4	I(s)/O	MMC_ D1	I(s)/O	LCD0_ DATA1	O	—	—	—	—	—	—
165	M3	P11_7	I(s)/O	—	—	DV0_ DATA19	I(s)	SD_ D0_0	I(s)/O	$\overline{\text{CTS5}}$	I(s)/O	MMC_ D0	I(s)/O	LCD0_ DATA0	O	—	—	—	—	—	—
166	M4	Vcc																			
167	M9	Vss																			
168	M10	Vss																			
169	M11	Vss																			
170	M12	Vss																			
171	M13	Vss																			
172	M14	Vss																			
173	M19	PVcc																			
174	M20	P4_5	I(s)/O	—	—	LCD0_ DATA13	O	SSL10	I(s)/O	TIOC4B	I(s)/O	PWM2F	O	SSIWS 0	I(s)/O	—	—	DV0_ DATA13	I(s)	—	—
175	M21	P4_4	I(s)/O	—	—	LCD0_ DATA12	O	RSPCK1	I(s)/O	TIOC4A	I(s)/O	PWM2E	O	SSISCK 0	I(s)/O	—	—	DV0_ DATA12	I(s)	—	—
176	M22	P10_7	I(s)/O	—	—	DV0_ DATA3	I(s)	TIOC0D	I(s)/O	PWM2H	O	ET_ TXD3	O	LCD0_ DATA16	O	VIO_D3	I(s)	—	—	—	—
177	N1	P7_13	I(s)/O	—	—	A5	O	SSIWS4	I(s)/O	ET_ MDIO	I(s)/O	—	—	—	—	—	—	TIOC4B	I(s)/O	IRQ5	I(s)
178	N2	P7_14	I(s)/O	—	—	A6	O	SSI DATA4	I(s)/O	ET_ CRS	I(s)	—	—	—	—	—	—	TIOC4C	I(s)/O	IRQ6	I(s)

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
179	N3	P7_15	I(s)/O	—	—	A7	O	RSPCK0	I(s)/O	ET_ RXCLK	I(s)	$\overline{\text{CTS5}}$	I(s)/O	SCI_ TXD0	O	—	—	TIOC4D	I(s)/O	—	—
180	N4	PVcc																			
181	N9	Vss																			
182	N10	Vss																			
183	N11	Vss																			
184	N12	Vss																			
185	N13	Vss																			
186	N14	Vss																			
187	N19	P10_4	I(s)/O	—	—	DV0_ DATA0	I(s)	TIOC0A	I(s)/O	PWM2E	O	ET_ TXD0	O	LCD0_ DATA19	O	VIO_D0	I(s)	—	—	—	—
188	N20	P10_5	I(s)/O	—	—	DV0_ DATA1	I(s)	TIOC0B	I(s)/O	PWM2F	O	ET_ TXD1	O	LCD0_ DATA18	O	VIO_D1	I(s)	—	—	—	—
189	N21	P10_6	I(s)/O	—	—	DV0_ DATA2	I(s)	TIOC0C	I(s)/O	PWM2G	O	ET_ TXD2	O	LCD0_ DATA17	O	VIO_D2	I(s)	—	—	—	—
190	N22	P4_3	I(s)/O	—	—	LCD0_ DATA11	O	TIOC0D	I(s)/O	$\overline{\text{FWE}}$	O	CAN3TX	O	RxD2	I(s)	—	—	MISO4	I(s)/O	MMC_ D7	I(s)/O
191	P1	P8_0	I(s)/O	—	—	A8	O	SSL00	I(s)/O	ET_ RXER	I(s)	SCK5	I(s)/O	SCI_ SCK0	I(s)/O	—	—	—	—	—	—
192	P2	P8_1	I(s)/O	—	—	A9	O	MOSI0	I(s)/O	ET_ RXDV	I(s)	TxD5	O	SCI_ RXD0	I(s)	—	—	—	—	—	—
193	P3	P8_2	I(s)/O	—	—	A10	O	MISO0	I(s)/O	AVB_ GPTP_ EXTERN	I(s)	RxD5	I(s)	IRQ0	I(s)	—	—	—	—	—	—
194	P4	PVcc																			
195	P9	Vss																			
196	P10	Vss																			
197	P11	Vss																			
198	P12	Vss																			
199	P13	Vss																			
200	P14	Vss																			
201	P19	Vss																			
202	P20	P4_0	I(s)/O	—	—	LCD0_ DATA8	O	TIOC0A	I(s)/O	$\overline{\text{FRE}}$	O	—	—	—	—	—	—	RSPCK4	I(s)/O	MMC_ D4	I(s)/O
203	P21	P4_2	I(s)/O	—	—	LCD0_ DATA10	O	TIOC0C	I(s)/O	FALE	O	CAN3RX	I(s)	TxD2	O	—	—	MOSI4	I(s)/O	MMC_ D6	I(s)/O
204	P22	P4_1	I(s)/O	—	—	LCD0_ DATA9	O	TIOC0B	I(s)/O	FCLE	O	—	—	SCK2	I(s)/O	—	—	SSL40	I(s)/O	MMC_ D5	I(s)/O
205	R1	P8_3	I(s)/O	—	—	A11	O	DV1_ DATA0	I(s)	RSPCK2	I(s)/O	$\overline{\text{RTS5}}$	I(s)/O	—	—	IRQ1	I(s)	SCK2	I(s)/O	—	—
206	R2	P8_4	I(s)/O	—	—	A12	O	DV1_ DATA1	I(s)	SSL20	I(s)/O	—	—	—	—	IERxD	I(s)	RxD2	I(s)	—	—
207	R3	P8_5	I(s)/O	—	—	A13	O	DV1_ DATA2	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—	—	—	—	—
208	R4	Vcc																			
209	R19	Vcc																			
210	R20	P3_15	I(s)/O	—	—	LCD0_ DATA7	O	—	—	NAF7	I(s)/O	—	—	TRACE CTL	O	—	—	SD_ D2_1	I(s)/O	MMC_ D2	I(s)/O
211	R21	P3_14	I(s)/O	—	—	LCD0_ DATA6	O	—	—	NAF6	I(s)/O	—	—	TRACE CLK	O	—	—	SD_ D3_1	I(s)/O	MMC_ D3	I(s)/O
212	R22	P3_13	I(s)/O	—	—	LCD0_ DATA5	O	—	—	NAF5	I(s)/O	AUDIO_ XOUT	O	—	—	—	—	SD_ CMD_1	I(s)/O	MMC_ CMD	I(s)/O
213	T1	P11_8	I(s)/O	—	—	DV0_ DATA20	I(s)	SD_ CLK_0	O	$\overline{\text{RTS5}}$	I(s)/O	MMC_ CLK	O	LCD0_ TCON6	O	—	—	—	—	—	—
214	T2	P11_9	I(s)/O	—	—	DV0_ DATA21	I(s)	SD_ CMD_0	I(s)/O	SCK5	I(s)/O	MMC_ CMD	I(s)/O	LCD0_ TCON5	O	—	—	—	—	—	—
215	T3	P11_10	I(s)/O	—	—	DV0_ DATA22	I(s)	SD_ D3_0	I(s)/O	TxD5	O	MMC_ D3	I(s)/O	LCD0_ TCON4	O	—	—	—	—	—	—

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		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
216	T4	Vcc																			
217	T19	Vcc																			
218	T20	P3_10	I(s)/O	—	—	LCD0_ DATA2	O	—	—	NAF2	I(s)/O	—	—	TRACE DATA2	O	TIOC4C	I(s)/O	SD_ D1_1	I(s)/O	MMC_ D1	I(s)/O
219	T21	P3_11	I(s)/O	—	—	LCD0_ DATA3	O	—	—	NAF3	I(s)/O	—	—	TRACE DATA3	O	TIOC4D	I(s)/O	SD_ D0_1	I(s)/O	MMC_ D0	I(s)/O
220	T22	P3_12	I(s)/O	—	—	LCD0_ DATA4	O	—	—	NAF4	I(s)/O	—	—	—	—	—	—	SD_ CLK_1	O	MMC_ CLK	O
221	U1	Vss																			
222	U2	P8_6	I(s)/O	—	—	A14	O	DV1_ DATA3	I(s)	MISO2	I(s)/O	—	—	—	—	IETxD	O	TxD2	O	—	—
223	U3	P11_11	I(s)/O	—	—	DV0_ DATA23	I(s)	SD_ D2_0	I(s)/O	RxD5	I(s)	MMC_ D2	I(s)/O	LCD0_ TCON3	O	—	—	—	—	—	—
224	U4	P8_7	I(s)/O	—	—	A15	O	DV1_ DATA4	I(s)	AUDIO_ XOUT	O	IRQ5	I(s)	ET_ COL	I(s)	—	—	—	—	—	—
225	U19	Vcc																			
226	U20	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—
227	U21	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
228	U22	Vss																			
229	V1	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
230	V2	P8_8	I(s)/O	—	—	A16	O	DV1_ DATA5	I(s)	SPBIO 00_1	I(s)/O	SPDIF_ IN	I(s)	TIOC1A	I(s)/O	PWM1A	O	TxD3	O	SSISCK 5	I(s)/O
231	V3	P8_9	I(s)/O	—	—	A17	O	DV1_ DATA6	I(s)	SPBIO 10_1	I(s)/O	SPDIF_ OUT	O	TIOC1B	I(s)/O	PWM1B	O	RxD3	I(s)	SSIWS5	I(s)/O
232	V4	P8_13	I(s)/O	—	—	A21	O	—	—	SPBSSL _1	O	TIOC3D	I(s)/O	TxD5	O	PWM1F	O	SGOUT_ 3	O	SSIWS4	I(s)/O
233	V19	P3_8	I(s)/O	—	—	LCD0_ DATA0	O	—	—	NAF0	I(s)/O	—	—	TRACE DATA0	O	TIOC4A	I(s)/O	SD_ CD_1	I(s)	MMC_ CD	I(s)
234	V20	$\overline{\text{TRST}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
235	V21	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—
236	V22	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
237	W1	Vss																			
238	W2	P8_10	I(s)/O	—	—	A18	O	DV1_ DATA7	I(s)	SPBIO 20_1	I(s)/O	TIOC3A	I(s)/O	CAN4TX	O	PWM1C	O	SGOUT_ 0	O	SSITxD5	O
239	W3	P8_11	I(s)/O	—	—	A19	O	—	—	SPBIO 30_1	I(s)/O	TIOC3B	I(s)/O	RxD5	I(s)	PWM1D	O	SGOUT_ 1	O	DV0_ CLK	I(s)
240	W4	PVcc																			
241	W5	PVcc																			
242	W6	PVcc																			
243	W7	Vss																			
244	W8	Vss																			
245	W9	Vcc																			
246	W10	Vcc																			
247	W11	Vss																			
248	W12	PVcc																			
249	W13	PVcc																			
250	W14	PLLVcc																			
251	W15	Vss																			
252	W16	Vss																			
253	W17	AVss																			
254	W18	AVcc																			
255	W19	PVcc																			
256	W20	P3_9	I(s)/O	—	—	LCD0_ DATA1	O	—	—	NAF1	I(s)/O	—	—	TRACE DATA1	O	TIOC4B	I(s)/O	SD_ WP_1	I(s)	IRQ6	I(s)

No.	Ball number	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8	
		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
257	W21	AUDIO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
258	W22	AUDIO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
259	Y1	P8_12	I(s)/O	—	—	A20	O	—	—	SPBCLK_1	O	TIOC3C	I(s)/O	SCK5	I(s)/O	PWM1E	O	SGOUT_2	O	SSISCK4	I(s)/O
260	Y2	P8_14	I(s)/O	—	—	A22	O	SPBIO01_0	I(s)/O	SPBIO00_1	I(s)/O	TIOC2A	I(s)/O	RSPCK2	I(s)/O	PWM1G	O	TxD4	O	SSIDATA4	I(s)/O
261	Y3	PVcc																			
262	Y4	P3_7	I(s)/O	—	—	LCD0_TCON6	O	—	—	SSITxD1	O	LCD1_EXTCLK	I(s)	$\overline{\text{SCI\_CTS0/}}$ $\overline{\text{RTS0}}$	I(s)/O	TIOC3D	I(s)/O	$\overline{\text{CS1}}$	O	$\overline{\text{WDT OVF}}$	O
263	Y5	P3_4	I(s)/O	—	—	LCD0_TCON3	O	ET_RXCLK	I(s)	SSISCK1	I(s)/O	AUDIO_XOUT2	O	SCI_SCK0	I(s)/O	TIOC3A	I(s)/O	SCK3	I(s)/O	—	—
264	Y6	P10_2	I(s)/O	—	—	DV0_HSYNC	I(s)	TCLKC	I(s)	PWM2C	O	ET_TXEN	O	LCD0_DATA21	O	VIO_HD	I(s)	—	—	—	—
265	Y7	P3_2	I(s)/O	—	—	LCD0_TCON1	O	ET_TXEN	O	—	—	RxD2	I(s)	SCI_RXD1	I(s)	TEND0	O	PWM2C	O	MOSI3	I(s)/O
266	Y8	$\overline{\text{RES}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
267	Y9	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
268	Y10	Vss																			
269	Y11	VBUSIN1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
270	Y12	VBUSIN0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
271	Y13	USB AVcc																			
272	Y14	Vss																			
273	Y15	P0_0	I(s)	MD_BOOT0	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
274	Y16	P0_1	I(s)	MD_BOOT1	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
275	Y17	P1_10	I(s)	—	—	AN2	I(a)	—	—	IRQ4	I(s)	TCLKB	I(s)	—	—	—	—	—	—	—	—
276	Y18	P1_13	I(s)	—	—	AN5	I(a)	DV0_HSYNC	I(s)	—	—	$\overline{\text{WAIT}}$	I(s)	—	—	—	—	—	—	—	—
277	Y19	P1_15	I(s)	—	—	AN7	I(a)	—	—	—	—	AVB_CAPTURE	I(s)	—	—	—	—	—	—	—	—
278	Y20	PVcc																			
279	Y21	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
280	Y22	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
281	AA1	P8_15	I(s)/O	—	—	A23	O	SPBIO11_0	I(s)/O	SPBIO10_1	I(s)/O	TIOC2B	I(s)/O	SSL20	I(s)/O	PWM1H	O	RxD4	I(s)	—	—
282	AA2	PVcc																			
283	AA3	P9_1	I(s)/O	—	—	A25	O	SPBIO31_0	I(s)/O	CAN0RX	I(s)	IRQ0	I(s)	MISO2	I(s)/O	—	—	—	—	—	—
284	AA4	P3_5	I(s)/O	—	—	LCD0_TCON4	O	ET_RXER	I(s)	SSIWS1	I(s)/O	AUDIO_XOUT3	O	SCI_TXD0	O	TIOC3B	I(s)/O	TxD3	O	—	—
285	AA5	P10_1	I(s)/O	—	—	DV0_VSYNC	I(s)	TCLKB	I(s)	PWM2B	O	ET_TXER	O	LCD0_DATA22	O	VIO_VD	I(s)	—	—	—	—
286	AA6	P3_3	I(s)/O	—	—	LCD0_TCON2	O	ET_MDIO	I(s)/O	IRQ4	I(s)	$\overline{\text{BS}}$	O	$\overline{\text{SCI\_CTS1/}}$ $\overline{\text{RTS1}}$	I(s)/O	DACK0	O	PWM2D	O	MISO3	I(s)/O
287	AA7	P3_1	I(s)/O	—	—	LCD0_TCON0	O	ET_TXER	O	IRQ6	I(s)	TxD2	O	SCI_TXD1	O	AUDIO_CLK	I(s)	PWM2B	O	SSL30	I(s)/O
288	AA8	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
289	AA9	P0_5	I(s)	—	—	RTC_X4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—

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		Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O
290	AA10	Vss																			
291	AA11	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
292	AA12	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
293	AA13	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
294	AA14	Vss																			
295	AA15	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
296	AA16	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
297	AA17	P1_8	I(s)	—	—	AN0	I(a)	—	—	IRQ2	I(s)	DREQ0	I(s)	VIO_D14	I(s)	DV0_ DATA14	I(s)	—	—	—	—
298	AA18	P1_11	I(s)	—	—	AN3	I(a)	—	—	IRQ5	I(s)	TCLKD	I(s)	—	—	—	—	—	—	—	—
299	AA19	P1_14	I(s)	—	—	AN6	I(a)	—	—	—	—	ET_ COL	I(s)	—	—	—	—	—	—	—	—
300	AA20	AVcc																			
301	AA21	PVcc																			
302	AA22	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
303	AB1	PVcc																			
304	AB2	P9_0	I(s)/O	—	—	A24	O	SPBIO 21_0	I(s)/O	CAN0TX	O	TCLKC	I(s)	MOSI2	I(s)/O	—	—	—	—	—	—
305	AB3	P3_6	I(s)/O	—	—	LCD0_ TCON5	O	ET_ RXDV	I(s)	SSIRxD1	I(s)	—	—	SCI_ RXD0	I(s)	TIOC3C	I(s)/O	RxD3	I(s)	—	—
306	AB4	P10_0	I(s)/O	—	—	DV0_ CLK	I(s)	TCLKA	I(s)	PWM2A	O	ET_ TXCLK	I(s)	LCD0_ DATA23	O	VIO_ CLK	I(s)	—	—	—	—
307	AB5	P10_3	I(s)/O	—	—	—	—	TCLKD	I(s)	PWM2D	O	ET_ CRS	I(s)	LCD0_ DATA20	O	VIO_ FLD	I(s)	—	—	—	—
308	AB6	P3_0	I(s)/O	—	—	LCD0_ CLK	O	ET_ TXCLK	I(s)	IRQ2	I(s)	SCK2	I(s)/O	SCI_ SCK1	I(s)/O	TxD2	O	PWM2A	O	RSPCK3	I(s)/O
309	AB7	Vss																			
310	AB8	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
311	AB9	P0_4	I(s)	—	—	RTC_X3	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—
312	AB10	Vss																			
313	AB11	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
314	AB12	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
315	AB13	Vss																			
316	AB14	USB APVcc																			
317	AB15	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
318	AB16	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
319	AB17	Vss																			
320	AB18	P1_9	I(s)	—	—	AN1	I(a)	—	—	IRQ3	I(s)	—	—	VIO_ D15	I(s)	DV0_ DATA15	I(s)	—	—	—	—
321	AB19	P1_12	I(s)	—	—	AN4	I(a)	DV0_ VSYNC	I(s)	—	—	VIO_ FLD	I(s)	—	—	—	—	—	—	—	—
322	AB20	AVss																			
323	AB21	AVref																			
324	AB22	Vss																			

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