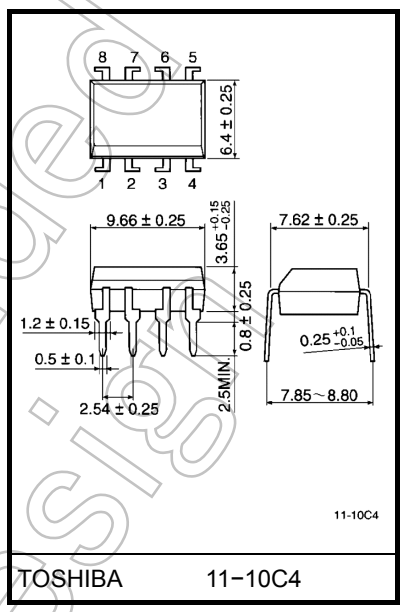
TOSHIBA Photocoupler GaAℓAs Ired & Photo IC

6N135, 6N136

Digital Logic Isolation
Line Receiver
Power Supply Control
Switching Power Supply
Transistor Inverter

Unit: mm



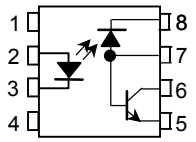
TOSHIBA 11−10C4

Weight: 0.54 g (typ.)

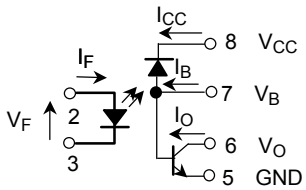
The TOSHIBA 6N135 and 6N136 consists of a high emitting diode and a one chip photo diode−transistor.
Each unit is 8−lead DIP package.

- Isolation voltage: 2500 V_{rms} (min)
- High speed: t_{pHL}, t_{pLH} = 0.5 μs (typ.) (R_L = 1.9kΩ)
- TTL compatible
- If base pin is open, output signal will be noisy by environmental condition. For this base, TLP550 is suitable
- UL recognized: UL1577, file no. E67349

Pin Configurations



1 : N.C.
2 : ANODE
3 : CATHODE
4 : N.C.
5 : EMITTER
6 : COLLECTOR
7 : BASE, ANODE
8 : CATHODE



Not Recommended for New Design

Start of commercial production
1982/10

Absolute Maximum Ratings (Ta = 25°C)

Characteristic			Symbol	Rating	Unit
LED	Forward current	(Note 1)	I_F	25	mA
	Pulse forward current	(Note 2)	I_{FP}	50	mA
	Total pulse forward current	(Note 3)	I_{FPT}	1	A
	Reverse voltage		V_R	5	V
	Diode power dissipation	(Note 4)	P_D	45	mW
Detector	Output current		I_O	8	mA
	Peak output current		I_{OP}	16	mA
	Emitter–base reverse voltage (pin 5–7)		V_{EB}	5	V
	Supply voltage		V_{CC}	–0.5 to 15	V
	Output voltage		V_O	–0.5 to 15	V
	Base current (pin 7)		I_B	5	mA
	Output power dissipation	(Note 5)	P_o	100	mW
Operating temperature range			T_{opr}	–55 to 100	°C
Storage temperature range			T_{stg}	–55 to 125	°C
Lead solder temperature (10s)		(Note 6)	T_{sol}	260	°C
Isolation voltage		(Note 7)	BV_S	2500	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

(Note 1) Derate 0.8 mA above 70°C.
(Note 2) 50% duty cycle, 1ms pulse width.
Derate 1.6 mA / °C above 70°C.
(Note 3) Pulse width 1μs, 300pps.
(Note 4) Derate 0.9 mW / °C above 70°C.
(Note 5) Derate 2 mW / °C above 70°C.
(Note 6) Soldering portion of lead: Up to 2mm from the body of the device.
(Note 7) R.H. ≤ 60%, AC, 1minute

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Electrical Characteristics
Over Recommended Temperature (Ta = 0°C~70°C unless otherwise noted)

Characteristic		Symbol	Test Condition	Min	(**)Typ.	Max	Unit
Current transfer ratio	6N135	CTR	I_F = 16mA, V_O = 0.4V, V_{CC} = 4.5V, Ta = 25°C (Note 8)	7	18	—	%
	6N136			19	24	—	%
	6N135	CTR	I_F = 16mA, V_O = 0.5V, V_{CC} = 4.5V (Note 1)	5	13	—	%
	6N136			15	21	—	%
Logic low output voltage	6N135	V_{OL}	I_F = 16mA, I_O = 1.1mA, V_{CC} = 4.5V	—	0.1	0.4	V
	6N136		I_F = 16mA, I_O = 2.4mA, V_{CC} = 4.5V	—	0.1	0.4	V
Logic high output current		I_{OH}	I_F = 0mA, V_O = V_{CC} = 5.5V, Ta = 25°C	—	3	500	nA
			I_F = 0mA, V_O = V_{CC} = 15V, Ta = 25°C	—	0.1	1	μA
		I_{OH}	I_F = 0 mA, V_O = V_{CC} = 15V	—	—	50	μA
Logic low supply current		I_{CCL}	I_F = 16mA, V_O = open, V_{CC} = 15V	—	40	—	μA
Logic high supply current		I_{CCH}	I_F = 0mA, V_O = open, V_{CC} = 15V, Ta = 25°C	—	0.01	1	μA
		I_{CCH}	I_F = 0mA, V_O = open, V_{CC} = 15V	—	—	2	μA
Input forward voltage		V_F	I_F = 16mA, Ta = 25°C	—	1.65	1.7	V
Temperature coefficient of forward voltage		$\Delta V_F / \Delta Ta$	I_F = 16mA	—	−1.9	—	mV / °C
Input reverse breakdown voltage		BV_R	I_R = 10μA, Ta = 25°C	5	—	—	V
Input capacitance		C_{IN}	f = 1MHz, V_F = 0	—	60	—	pF
Resistance (input−output)		R_{I-O}	V_{I-O} = 500V, R.H. ≤ 60% (Note 9)	—	10^{12}	—	Ω
Capacitance (input−output)		C_{I-O}	f = 1MHz (Note 9)	—	0.6	—	pF
Transistor DC current gain		h_{FE}	V_O = 5V, I_O = 3mA	—	80	—	—

(**) All typical values are at Ta = 25°C

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Switching Specifications
(unless otherwise specified. Ta = 25°C, V_{CC} = 5V, I_F = 16mA)

Characteristic		Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time to logic low at output	6N135	t_{pHL}	1	R_L = 4.1kΩ	—	0.2	1.5	μs
	6N136			R_L = 1.9kΩ	—	0.2	0.8	μs
Propagation delay time to logic high at output	6N135	t_{pLH}	1	R_L = 4.1kΩ	—	1.0	1.5	μs
	6N136			R_L = 1.9kΩ	—	0.5	0.8	μs
Common mode transient immunity at logic high level output (Note 10)	6N135	CM_H	2	I_F = 0mA V_{CM} = $10V_{p-p}$ R_L = 4.1kΩ	—	1000	—	V / μs
	6N136			I_F = 0mA V_{CM} = $10V_{p-p}$ R_L = 1.9kΩ	—	1000	—	V / μs
Common mode transient immunity at logic low level output (Note 10)	6N135	CM_L	2	V_{CM} = $10V_{p-p}$ R_L = 4.1kΩ I_F = 16mA	—	−1000	—	V / μs
	6N136			V_{CM} = $10V_{p-p}$ R_L = 1.9kΩ I_F = 16mA	—	−1000	—	V / μs
Bandwidth (Note 11)		BW	—	R_L = 100Ω	—	2	—	MHz

(Note 8) DC current transfer ratio is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100%.

(Note 9) Device considered a two−terminal device: Pins 1, 2, 3 and 4 shorted together and pins 5, 6, 7 and 8 shorted together.

(Note 10) Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{CM} / dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0V).
Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{CM} / dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8V).

(Note 11) The frequency at which the AC output voltage is 3dB below the low frequency asymptote.

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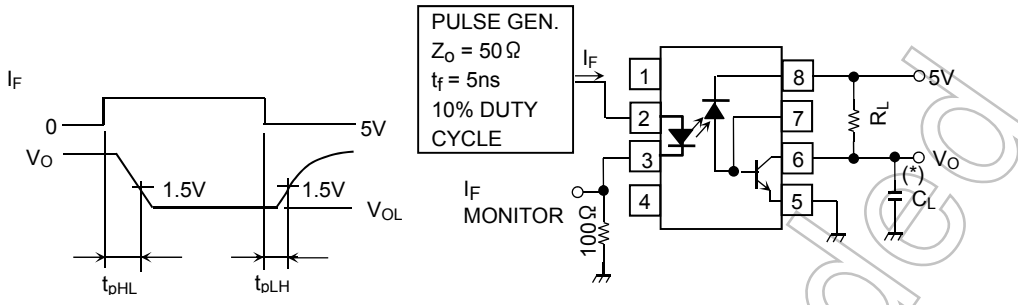
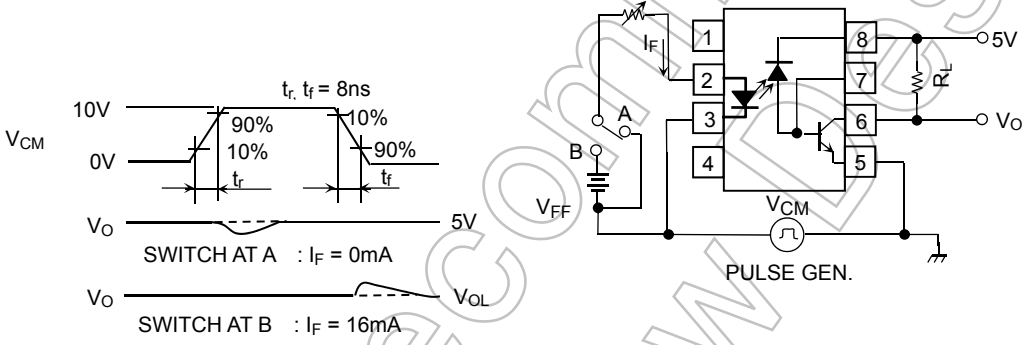
Test Circuit 1.



(*) C_L is approximately 15pF which includes probe and stray wiring capacitance.

Test Circuit 2.



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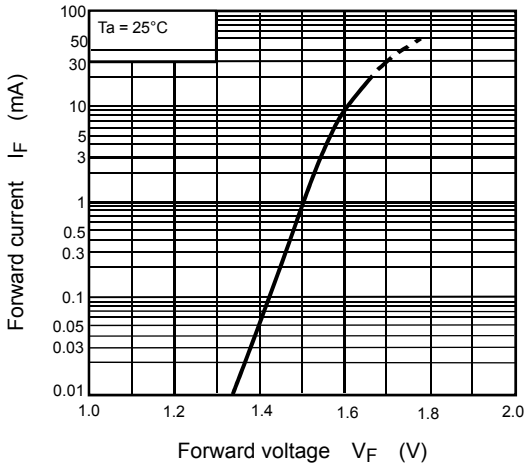
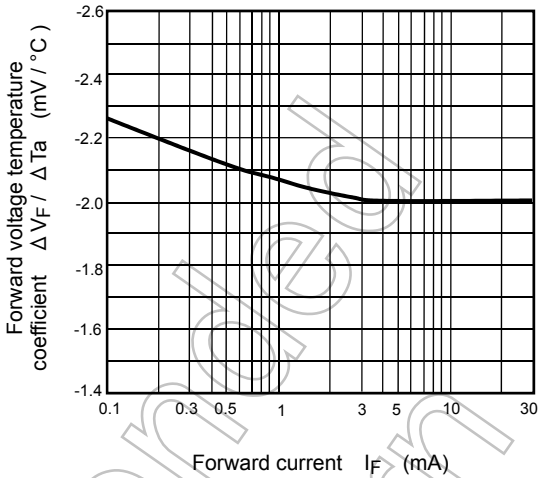
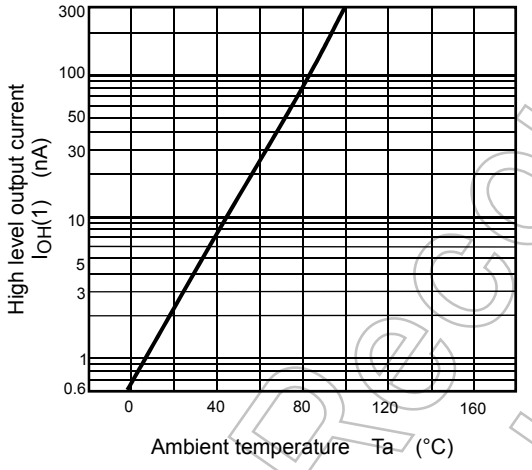
$I_F - V_F$



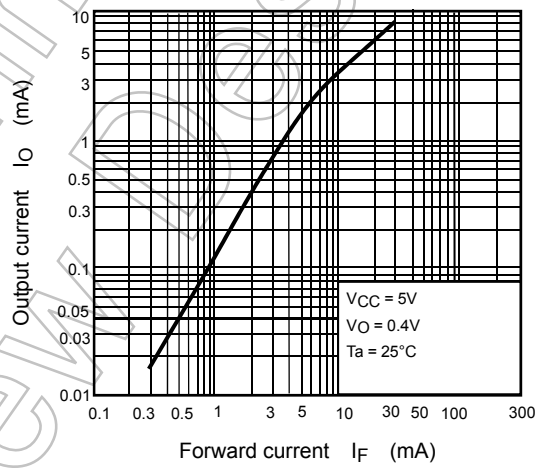
$\Delta V_F / \Delta Ta - I_F$



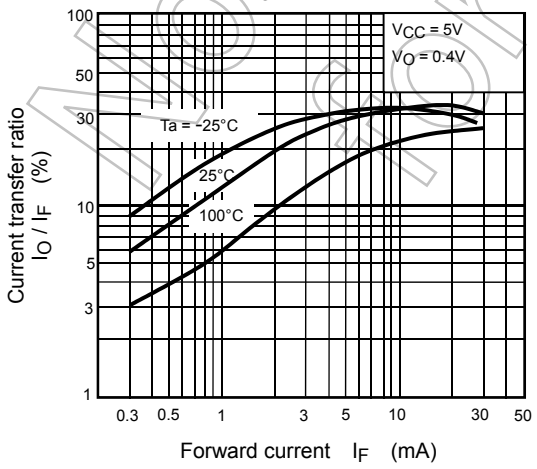
I_{OH} (1) – Ta



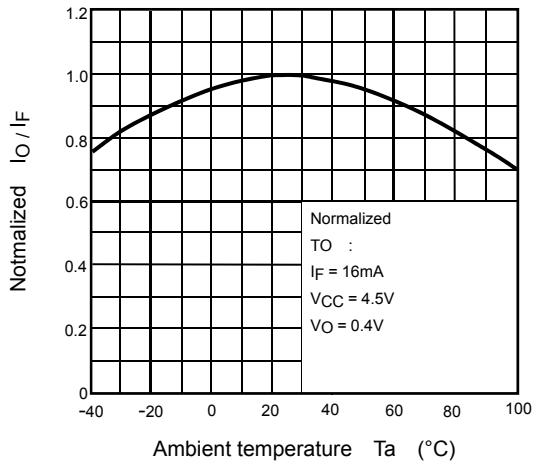
I_O - I_F



I_O / I_F – I_F



I_O / I_F – Ta



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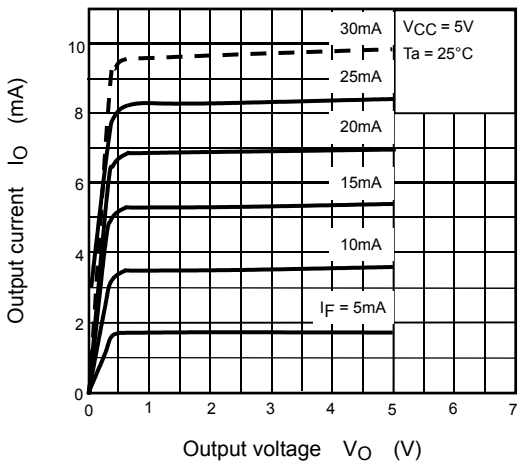
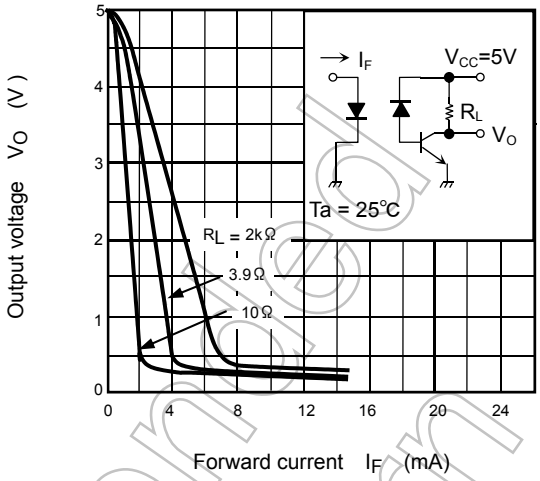
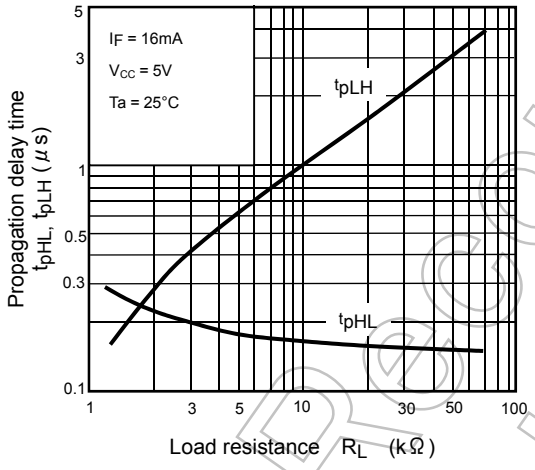
$I_O - V_O$



$V_O - I_F$



$t_{pHL}, t_{pLH} - R_L$



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