

74HCU04

Hex inverter

Rev. 6 — 27 December 2012

Product data sheet

1. General description

The 74HCU04 is a hex unbuffered inverter. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

2. Features and benefits

- Complies with JEDEC standard JESD7A
- Balanced propagation delays
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from -40 °C to $+125\text{ °C}$

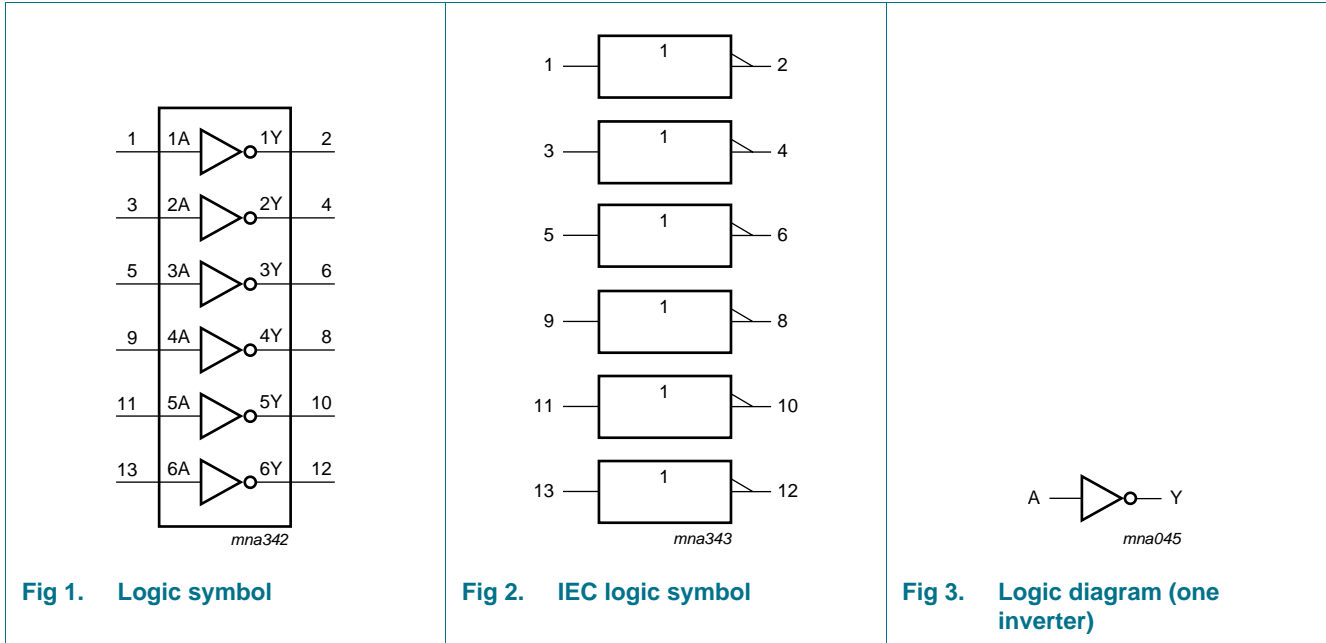
3. Ordering information

Table 1. Ordering information

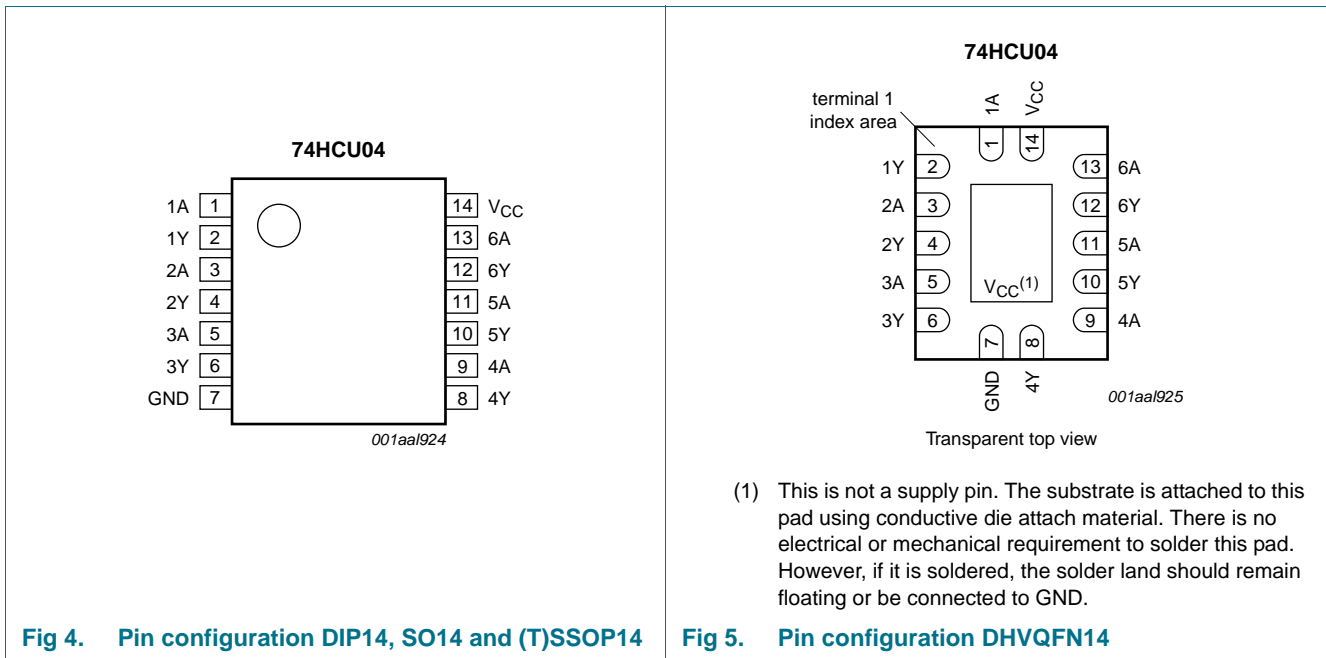
Type number	Package			
	Temperature range	Name	Description	Version
74HCU04N	-40 °C to $+125\text{ °C}$	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
74HCU04D	-40 °C to $+125\text{ °C}$	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74HCU04DB	-40 °C to $+125\text{ °C}$	SSOP14	plastic shrink small outline package; 14 leads; body width 5.3 mm	SOT337-1
74HCU04PW	-40 °C to $+125\text{ °C}$	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74HCU04BQ	-40 °C to $+125\text{ °C}$	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body $2.5 \times 3 \times 0.85\text{ mm}$	SOT762-1



4. Functional diagram



5. Pinning information



5.1 Pin description

Table 2. Pin description

Symbol	Pin	Description
1A	1	data input
1Y	2	data output
2A	3	data input
2Y	4	data output
3A	5	data input
3Y	6	data output
GND	7	ground (0 V)
4Y	8	data output
4A	9	data input
5Y	10	data output
5A	11	data input
6Y	12	data output
6A	13	data input
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level

Input	Output
nA	nY
L	H
H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	[1] -	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	[1] -	±50	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	-	±25	mA
I _{CC}	supply current		-	50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation		[2]		
	DIP14 package		-	750	mW
	SO14, (T)SSOP14 and DHVQFN14 packages		-	500	mW

- [1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
- [2] For DIP14 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
 For SO14 package: P_{tot} derates linearly with 8 mW/K above 70 °C.
 For (T)SSOP14 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
 For DHVQFN14 packages: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	supply voltage		2.0	5.0	6.0	V
V_I	input voltage		0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0\text{ V}$	1.7	1.4	-	1.7	-	1.7	-	V
		$V_{CC} = 3.0\text{ V}$	3.6	2.6	-	3.6	-	3.6	-	V
		$V_{CC} = 5.5\text{ V}$	4.8	3.4	-	4.8	-	4.8	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0\text{ V}$	-	0.6	0.3	-	0.3	-	0.3	V
		$V_{CC} = 3.0\text{ V}$	-	1.9	0.9	-	0.9	-	0.9	V
		$V_{CC} = 5.5\text{ V}$	-	2.6	1.2	-	1.2	-	1.2	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = -20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	1.8	2.0	-	1.8	-	1.8	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	4.0	4.5	-	4.0	-	4.0	-	V
		$I_O = -4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	3.98	4.32	-	3.84	-	3.7	-	V
		$I_O = -20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	5.5	6.0	-	5.5	-	5.5	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}								
		$I_O = 20\ \mu\text{A}; V_{CC} = 2.0\text{ V}$	-	0	0.2	-	0.2	-	0.2	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 4.5\text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 4.0\text{ mA}; V_{CC} = 4.5\text{ V}$	-	0.15	0.26	-	0.33	-	0.4	V
		$I_O = 20\ \mu\text{A}; V_{CC} = 6.0\text{ V}$	-	0	0.5	-	0.5	-	0.5	V
		$I_O = 5.2\text{ mA}; V_{CC} = 6.0\text{ V}$	-	0.16	0.26	-	0.33	-	0.4	V

Table 6. Static characteristics ...continued
 Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	±0.1	-	±1.0	-	±1.0	µA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0$ A; $V_{CC} = 6.0$ V	-	-	2	-	20	-	20	µA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics
 Voltages are referenced to GND (ground = 0 V); For test circuit see [Figure 7](#).

Symbol	Parameter	Conditions	25 °C		-40 °C to +85 °C	-40 °C to +125 °C	Unit
			Typ	Max	Max	Max	
t_{pd}	propagation delay	nA to nY; see Figure 6 [1]					
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	19	70	90	105	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	7	14	18	21	ns
		$V_{CC} = 5.0$ V; $C_L = 15$ pF	5	-	-	-	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	6	12	15	18	ns
t_t	transition time	see Figure 6 [2]					
		$V_{CC} = 2.0$ V; $C_L = 50$ pF	19	75	95	110	ns
		$V_{CC} = 4.5$ V; $C_L = 50$ pF	7	15	19	22	ns
		$V_{CC} = 6.0$ V; $C_L = 50$ pF	6	13	16	19	ns
C_{PD}	power dissipation capacitance	per inverter; $V_I =$ GND to V_{CC} [3]	10	-			pF

[1] t_{pd} is the same as t_{PHL} , t_{PLH} .

[2] t_t is the same as t_{THL} , t_{TLH} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

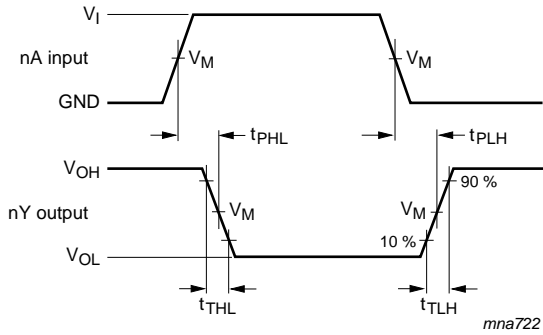
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

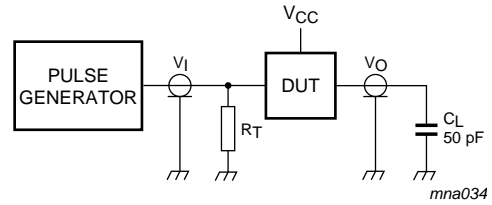
$\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



$V_M = 0.5 \times V_{CC}$; $V_I = \text{GND to } V_{CC}$.

Fig 6. The input (nA) to output (nY) propagation delay times



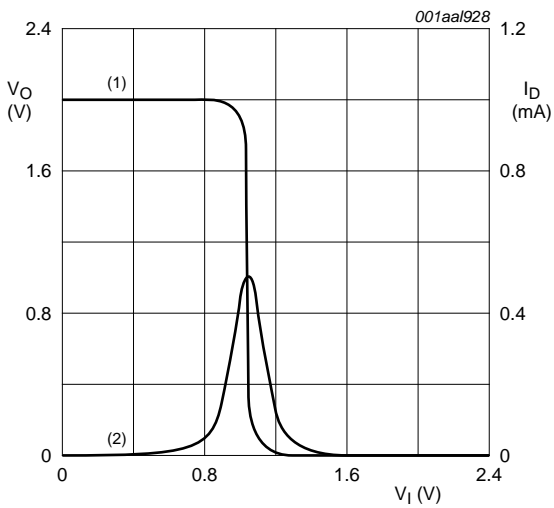
Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

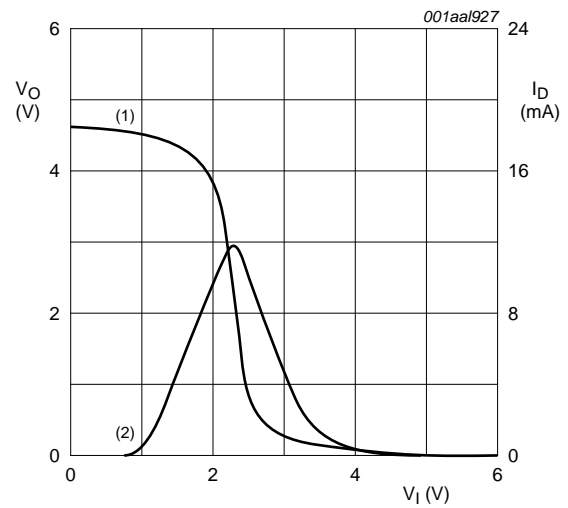
Fig 7. Load circuit for switching times

12. Typical transfer characteristics



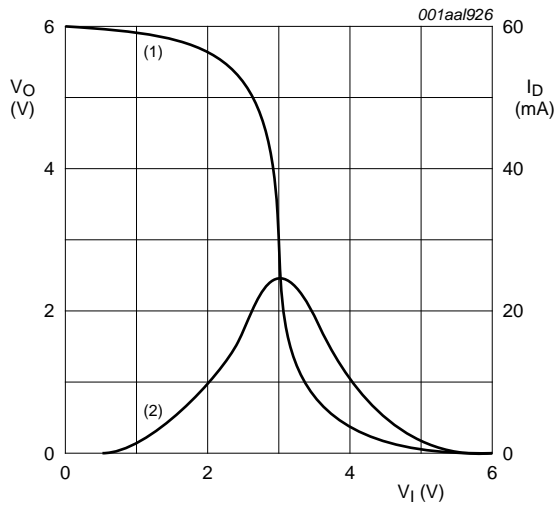
$T_{amb} = 25 \text{ }^\circ\text{C}$.

Fig 8. $V_{CC} = 2.0 \text{ V}$; $I_O = 0 \text{ A}$



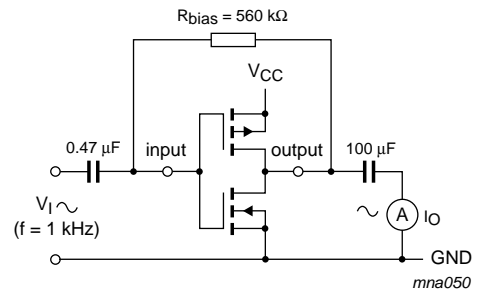
$T_{amb} = 25 \text{ }^\circ\text{C}$.

Fig 9. $V_{CC} = 4.5 \text{ V}$; $I_O = 0 \text{ A}$



T_{amb} = 25 °C.

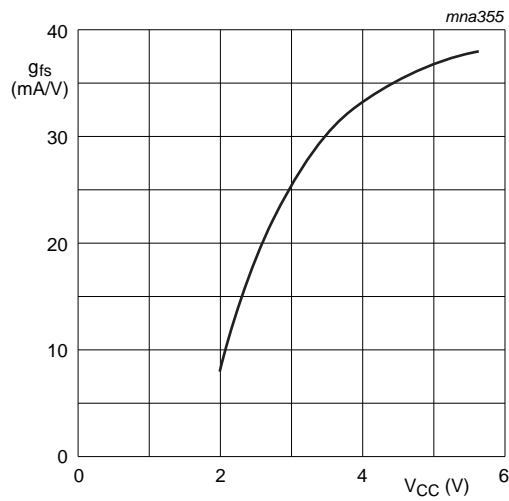
Fig 10. V_{CC} = 6.0 V; I_O = 0 A



$$g_{fs} = \frac{\Delta I_O}{\Delta V_I}$$

f_i = 1 kHz at V_O is constant

Fig 11. Test set-up for measuring forward transconductance



T_{amb} = 25 °C.

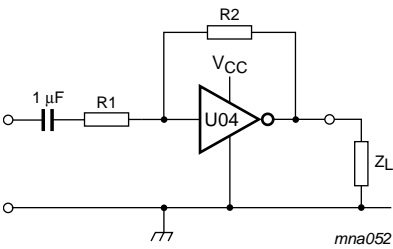
Fig 12. Typical forward transconductance as a function of the supply voltage

13. Application information

Some applications are:

- Linear amplifier (see [Figure 13](#))
- Crystal oscillator design (see [Figure 14](#))
- Astable multivibrator (see [Figure 15](#))

Remark: All values given are typical unless otherwise specified.

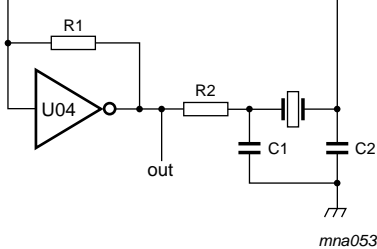


Maximum $V_{O(p-p)} = V_{CC} - 2.0 \text{ V}$ centered at $0.5 \times V_{CC}$.

$$G_v = - \frac{G_{ol}}{1 + \frac{R1}{R2}(1 + G_{ol})}$$

G_{ol} = open loop gain
 G_v = voltage gain
 $R1 \geq 3 \text{ k}\Omega$, $R2 \leq 1 \text{ M}\Omega$
 $Z_L > 10 \text{ k}\Omega$; $G_{ol} = 20$ (typical)
 $V_{CC} = 6.0 \text{ V}$
 Typical unity gain bandwidth product is 5 MHz.

Fig 13. Used as a linear amplifier



$C1 = 47 \text{ pF}$ (typical)
 $C2 = 33 \text{ pF}$ (typical)
 $R1 = 1 \text{ M}\Omega$ to $10 \text{ M}\Omega$ (typical)
 $R2$ optimum value depends on the frequency and required stability against changes in V_{CC} or average minimum I_{CC} . I_{CC} is typically 5 mA at $V_{CC} = 5 \text{ V}$ and $f_i = 10 \text{ MHz}$.

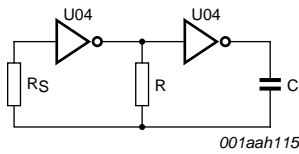
Fig 14. Crystal oscillator configuration

Table 8. External components for resonator ($f < 1 \text{ MHz}$)
 All values given are typical and must be used as an initial set-up.

Frequency	R1	R2	C1	C2
10 kHz to 15.9 kHz	22 M Ω	220 k Ω	56 pF	20 pF
16 kHz to 24.9 kHz	22 M Ω	220 k Ω	56 pF	10 pF
25 kHz to 54.9 kHz	22 M Ω	100 k Ω	56 pF	10 pF
55 kHz to 129.9 kHz	22 M Ω	100 k Ω	47 pF	5 pF
130 kHz to 199.9 kHz	22 M Ω	47 k Ω	47 pF	5 pF
200 kHz to 349.9 kHz	10 M Ω	47 k Ω	47 pF	5 pF
350 kHz to 600 kHz	10 M Ω	47 k Ω	47 pF	5 pF

Table 9. Optimum value for R2

Frequency	R2	Optimum for
3 kHz	2.0 kΩ	minimum required I _{CC}
	8.0 kΩ	minimum influence due to change in V _{CC}
6 kHz	1.0 kΩ	minimum required I _{CC}
	4.7 kΩ	minimum influence by V _{CC}
10 kHz	0.5 kΩ	minimum required I _{CC}
	2.0 kΩ	minimum influence by V _{CC}
14 kHz	0.5 kΩ	minimum required I _{CC}
	1.0 kΩ	minimum influence by V _{CC}
>14 kHz	-	replace R2 by C3 with a typical value of 35 pF

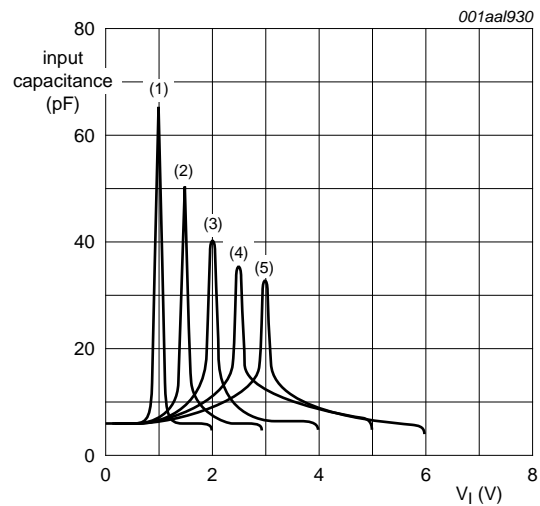


$$f = \frac{1}{T} \approx \frac{1}{2.2RC}$$

$$R_S \approx 2 \times R$$

The average I_{CC} (mA) is approximately 3.5 + 0.05 × f (MHz) × C (pF) at V_{CC} = 5.0 V.

Fig 15. Astable multivibrator



V_{CC} = 2.0 V

V_{CC} = 3.0 V

V_{CC} = 4.0 V

V_{CC} = 5.0 V

V_{CC} = 6.0 V

T_{amb} = 25 °C.

Fig 16. Input capacitance as function of input voltage

14. Package outline

DIP14: plastic dual in-line package; 14 leads (300 mil)

SOT27-1

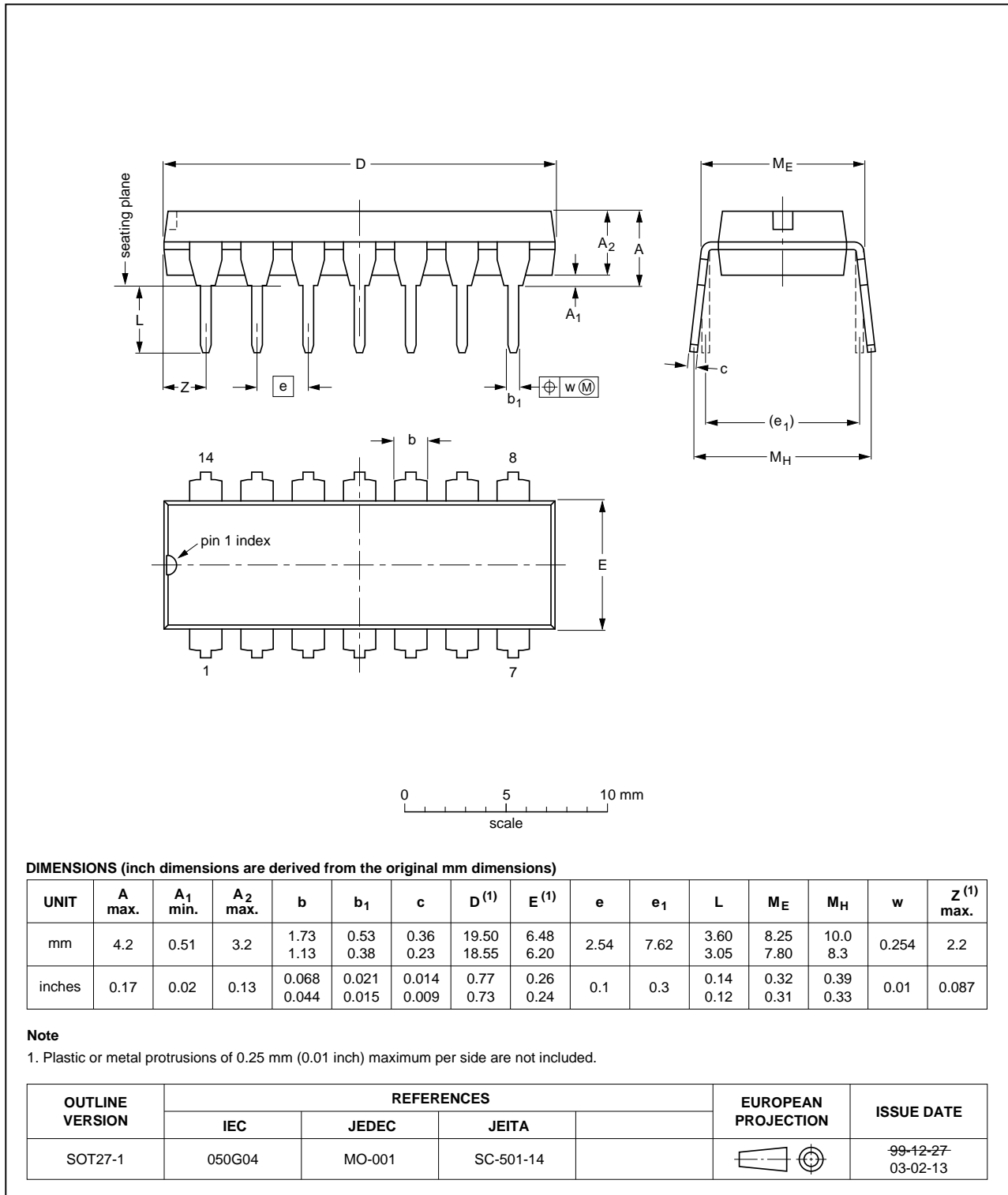


Fig 17. Package outline SOT27-1 (DIP14)

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

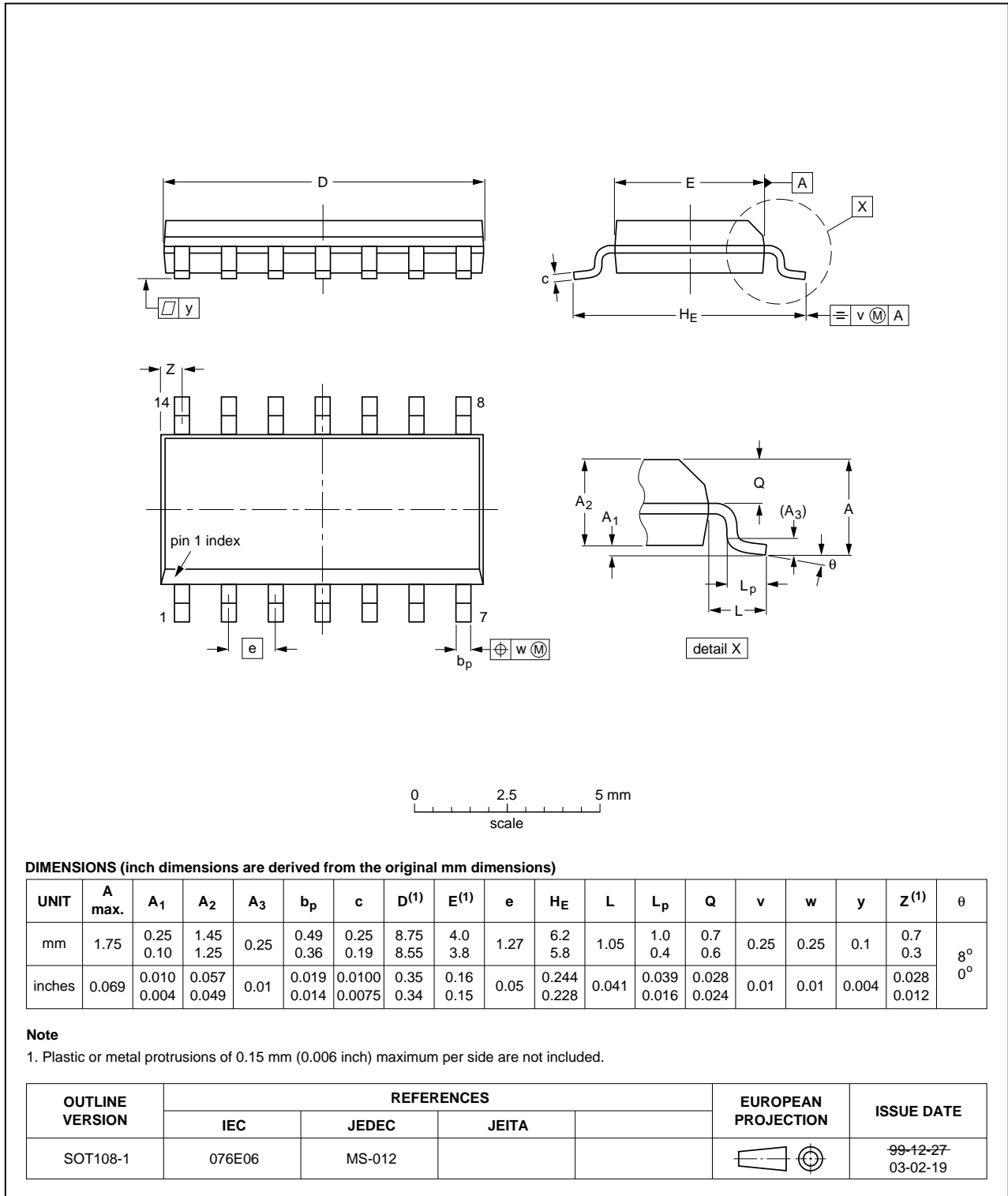


Fig 18. Package outline SOT108-1 (SO14)

SSOP14: plastic shrink small outline package; 14 leads; body width 5.3 mm

SOT337-1

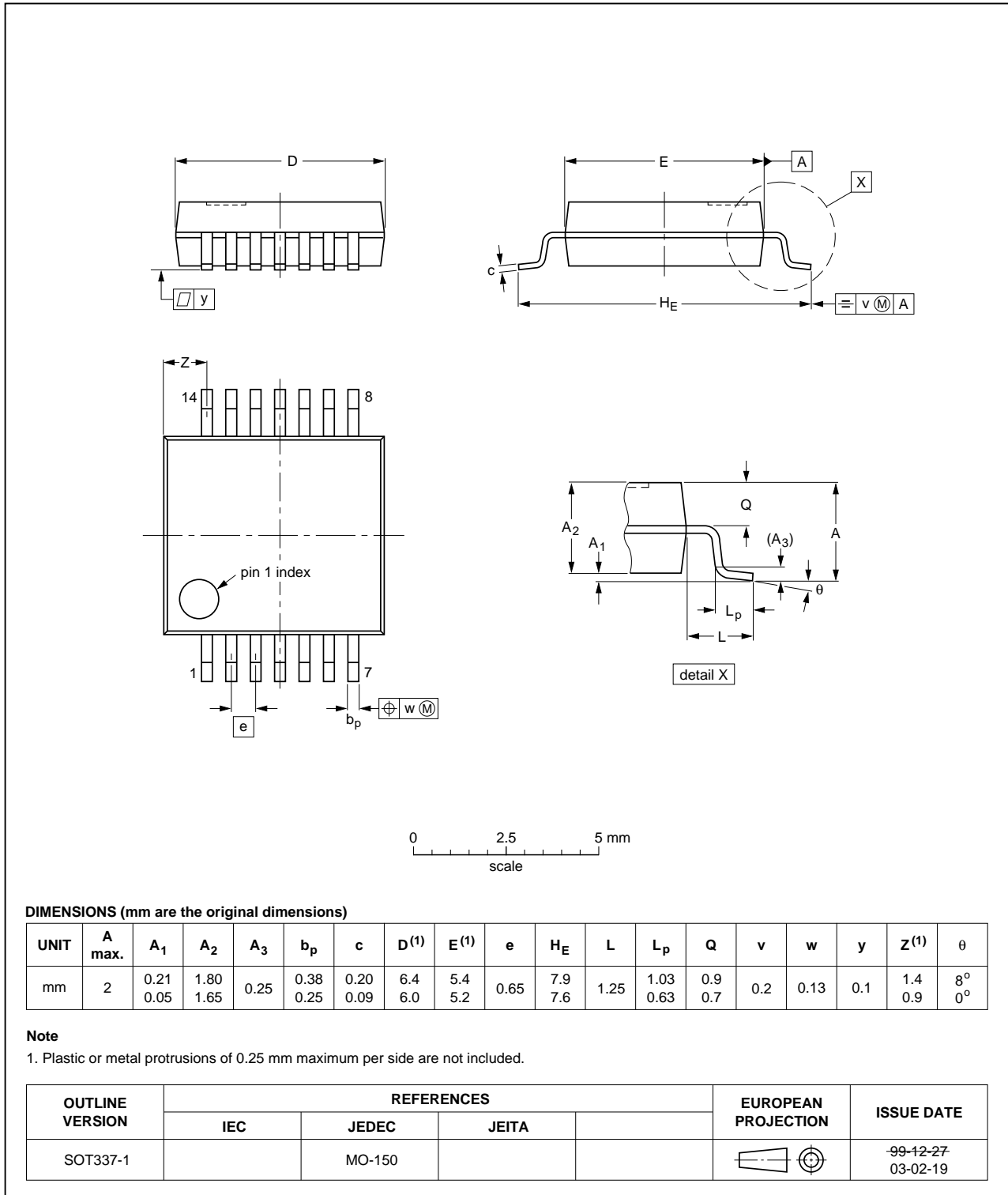


Fig 19. Package outline SOT337-1 (SSOP14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

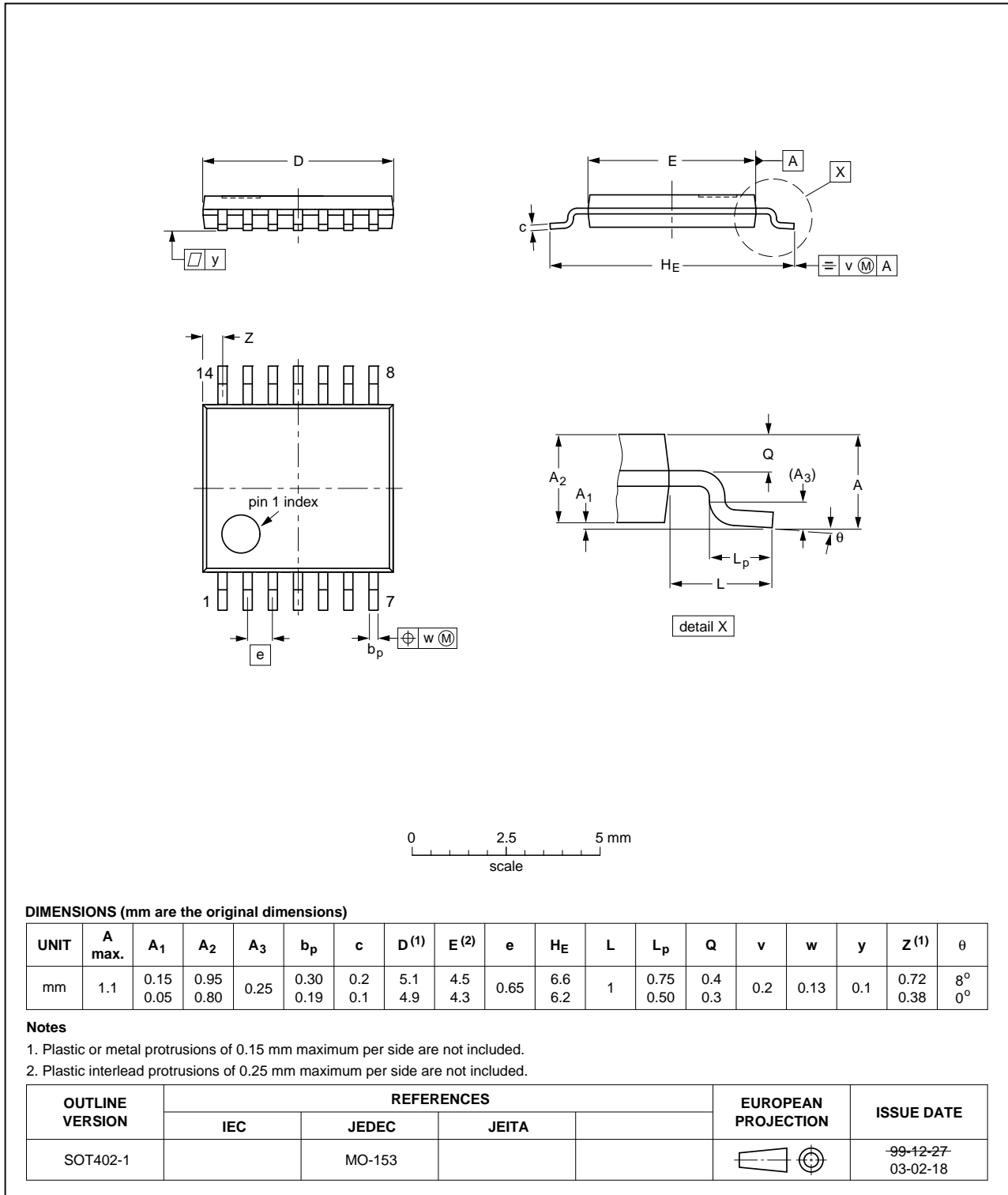


Fig 20. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1

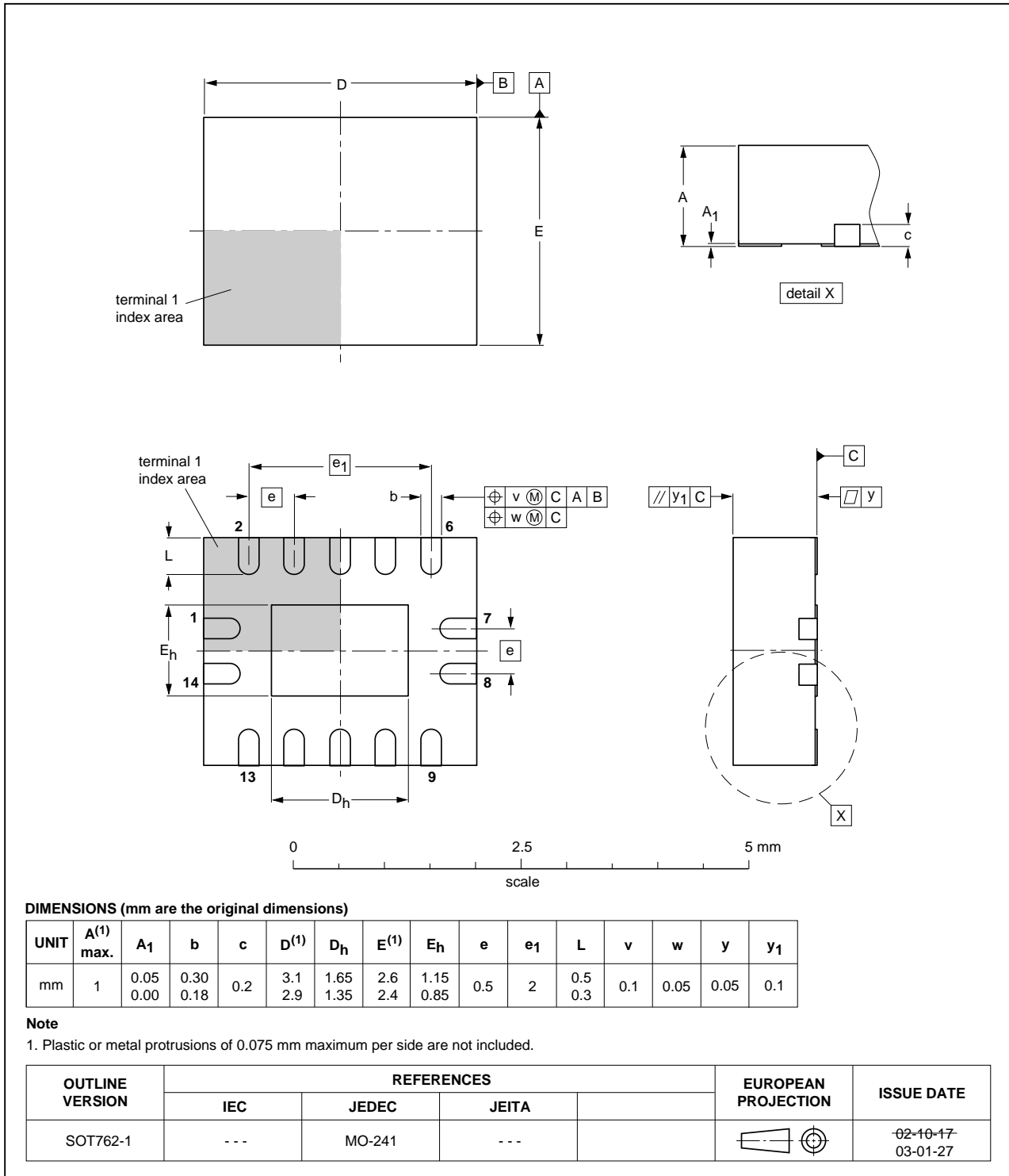


Fig 21. Package outline SOT762-1 (DHVQFN14)

15. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
LSTTL	Low-power Schottky Transistor-Transistor Logic
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
CDM	Charge Device Model
TTL	Transistor-Transistor Logic

16. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HCU04 v.6	20121227	Product data sheet	-	74HCU04 v.5
Modifications:	<ul style="list-style-type: none"> • New general description. 			
74HCU04 v.5	20120806	Product data sheet	-	74HCU04 v.4
Modifications:	<ul style="list-style-type: none"> • Measurement points added to figure 6 (errata). 			
74HCU04 v.4	20111212	Product data sheet	-	74HCU04 v.3
Modifications:	<ul style="list-style-type: none"> • Legal pages updated. 			
74HCU04 v.3	20100916	Product data sheet	-	74HCU04_CNV v.2
74HCU04_CNV v.2	19970826	Product specification	-	-

17. Legal information

17.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

19. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	1
4	Functional diagram	2
5	Pinning information	2
5.1	Pin description	3
6	Functional description	3
7	Limiting values	3
8	Recommended operating conditions	4
9	Static characteristics	4
10	Dynamic characteristics	5
11	Waveforms	6
12	Typical transfer characteristics	6
13	Application information	8
14	Package outline	10
15	Abbreviations	15
16	Revision history	15
17	Legal information	16
17.1	Data sheet status	16
17.2	Definitions	16
17.3	Disclaimers	16
17.4	Trademarks	17
18	Contact information	17
19	Contents	18

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2012.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 27 December 2012

Document identifier: 74HCU04

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for [Logic Gates](#) category:

Click to view products by [NXP](#) manufacturer:

Other Similar products are found below :

[5962-8769901BCA](#) [74HC85N](#) [NL17SG08P5T5G](#) [NL17SG32DFT2G](#) [NLU1G32AMUTCG](#) [NLV7SZ58DFT2G](#) [NLVHC1G08DFT1G](#)
[NLVVHC1G14DTT1G](#) [NLX2G08DMUTCG](#) [NLX2G08MUTCG](#) [MC74HCT20ADR2G](#) [091992B](#) [091993X](#) [093560G](#) [634701C](#) [634921A](#)
[NL17SG32P5T5G](#) [NL17SG86DFT2G](#) [NLU1G32CMUTCG](#) [NLV14001UBDR2G](#) [NLVVHC1G132DTT1G](#) [NLVVHC1G86DTT1G](#)
[NLX1G11AMUTCG](#) [NLX1G97MUTCG](#) [746427X](#) [74AUP1G17FW5-7](#) [74LS38](#) [74LVC1G08Z-7](#) [74LVC32ADTR2G](#) [74LVC1G125FW4-7](#)
[74LVC08ADTR2G](#) [MC74HCT20ADTR2G](#) [NLV14093BDTR2G](#) [NLV17SZ00DFT2G](#) [NLV17SZ02DFT2G](#) [NLV17SZ126DFT2G](#)
[NLV27WZ17DFT2G](#) [NLV74HC02ADR2G](#) [NLV74HC08ADR2G](#) [NLVVHC1GT32DFT1G](#) [74HC32S14-13](#) [74LS133](#) [74LVC1G32Z-7](#)
[M38510/30402BDA](#) [74LVC1G86Z-7](#) [74LVC2G08RA3-7](#) [M38510/06202BFA](#) [NLV74HC08ADTR2G](#) [NLV74HC14ADR2G](#)
[NLV74HC20ADR2G](#)