

# 74LVC4245A

Octal dual supply translating transceiver; 3-state

Rev. 10 — 18 December 2012

Product data sheet

## 1. General description

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The 74LVC4245A is an octal dual supply translating transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions. It is designed to interface between a 3 V and 5 V bus in a mixed 3 V and 5 V supply environment.

The device features an output enable input (pin  $\overline{\text{OE}}$ ) for easy cascading and a send/receive input (pin DIR) for direction control. Pin  $\overline{\text{OE}}$  controls the outputs so that the buses are effectively isolated.

In suspend mode, when  $V_{\text{CC(A)}}$  is zero, there will be no current flow from one supply to the other supply. The A-outputs must be set 3-state and the voltage on the A-bus must be smaller than  $V_{\text{diode}}$  (typical 0.7 V).

$V_{\text{CC(A)}} \geq V_{\text{CC(B)}}$ , except in suspend mode.

## 2. Features and benefits

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- 5 V tolerant inputs/outputs, for interfacing with 5 V logic
- Wide supply voltage range:
  - ◆ 3 V bus ( $V_{\text{CC(B)}}$ ): 1.5 V to 3.6 V
  - ◆ 5 V bus ( $V_{\text{CC(A)}}$ ): 1.5 V to 5.5 V
- CMOS low-power consumption
- Direct interface with TTL levels
- Inputs accept voltages up to 5.5 V
- High-impedance when  $V_{\text{CC(A)}} = 0$  V
- Complies with JEDEC standard no. JESD8B/JESD36
- ESD protection:
  - ◆ HBM JESD22-A114F exceeds 2000 V
  - ◆ MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from  $-40$  °C to  $+85$  °C and  $-40$  °C to  $+125$  °C



### 3. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74LVC4245AD	-40 °C to +125 °C	SO24	plastic small outline package; 24 leads; body width 7.5 mm	SOT137-1
74LVC4245ADB	-40 °C to +125 °C	SSOP24	plastic shrink small outline package; 24 leads; body width 5.3 mm	SOT340-1
74LVC4245APW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74LVC4245ABQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

### 4. Functional diagram

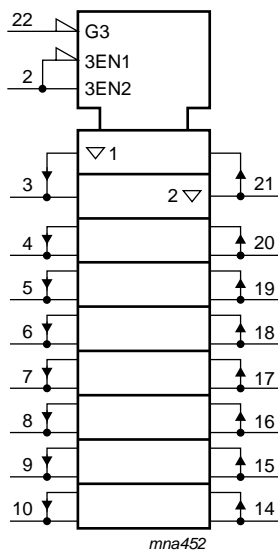


Fig 1. IEC Logic symbol

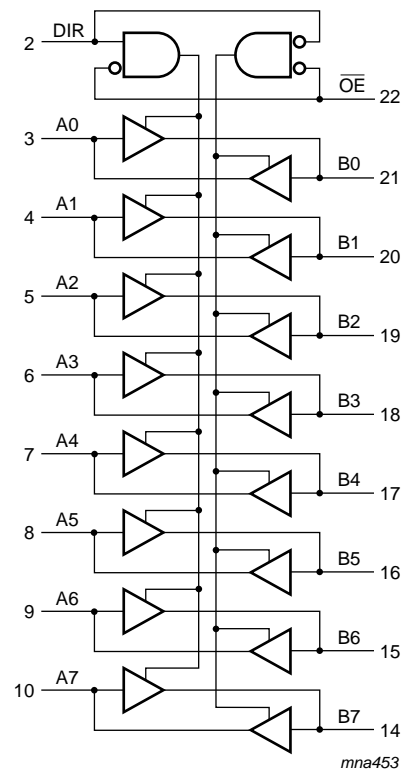
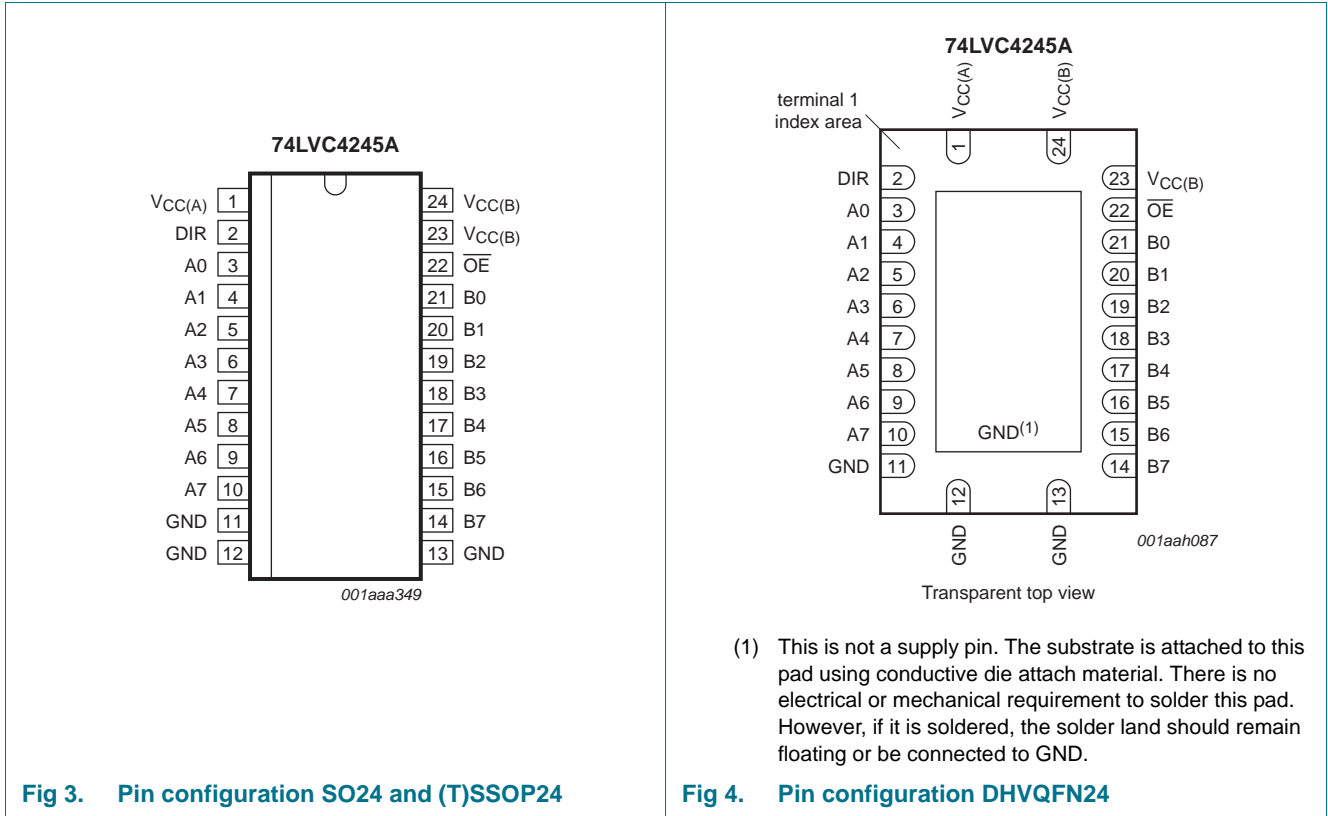


Fig 2. Logic diagram

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V <sub>CC(A)</sub>	1	supply voltage (5 V bus)
V <sub>CC(B)</sub>	23, 24	supply voltage (3 V bus)
GND	11, 12, 13	ground (0 V)
DIR	2	direction control
A[0:7]	3, 4, 5, 6, 7, 8, 9, 10	data input or output
B[0:7]	21, 20, 19, 18, 17, 16, 15, 14	data input or output
$\overline{OE}$	22	output enable input (active LOW)

## 6. Functional description

Table 3. Functional table<sup>[1]</sup>

Input		Input/output		
OE	DIR	An	Bn	
L	L	A = B	input	
L	H	input	B = A	
H	X	Z	Z	

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC(A)}$	supply voltage A		-0.5	+6.5	V
$V_{CC(B)}$	supply voltage B		-0.5	+4.6	V
$I_{IK}$	input clamping current	$V_I < 0$ V	-50	-	mA
$V_I$	input voltage		[1] -0.5	+6.5	V
$I_{OK}$	output clamping current	$V_O > V_{CCO}$ or $V_O < 0$ V	[3] -	$\pm 50$	mA
$V_O$	output voltage	output HIGH or LOW state	[1] -0.5	$V_{CC} + 0.5$	V
		output 3-state	[1] -0.5	+6.5	V
$I_O$	output current	$V_O = 0$ V to $V_{CCO}$	[3] -	$\pm 50$	mA
$I_{CC}$	supply current		-	100	mA
$I_{GND}$	ground current		-100	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$P_{tot}$	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SO24 packages: above 70 °C the value of  $P_{tot}$  derates linearly with 8 mW/K.  
 For (T)SSOP24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 5.5 mW/K.  
 For DHVQFN24 packages: above 60 °C the value of  $P_{tot}$  derates linearly with 4.5 mW/K.

[3]  $V_{CCO}$  is the supply voltage associated with the output.

## 8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC(A)}$	supply voltage A	$V_{CC(A)} \geq V_{CC(B)}$ ; see <a href="#">Figure 5</a> for maximum speed performance	1.5	-	5.5	V
$V_{CC(B)}$	supply voltage B	$V_{CC(A)} \geq V_{CC(B)}$ ; see <a href="#">Figure 5</a> for low-voltage applications	1.5	-	3.6	V
$V_I$	input voltage	for control inputs	0	-	5.5	V

Table 5. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V <sub>O</sub>	output voltage	output HIGH or LOW state	0	-	V <sub>CC</sub>	V
		output 3-state	0	-	5.5	V
T <sub>amb</sub>	ambient temperature		-40	-	+125	°C
Δt/ΔV	input transition rise and fall rate	V <sub>CC(B)</sub> = 2.7 V to 3.0 V	-	-	20	ns/V
		V <sub>CC(B)</sub> = 3.0 V to 3.6 V	-	-	10	ns/V
		V <sub>CC(A)</sub> = 3.0 V to 4.5 V	-	-	20	ns/V
		V <sub>CC(A)</sub> = 4.5 V to 5.5 V	-	-	10	ns/V

## 9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
T <sub>amb</sub> = -40 °C to +85 °C						
V <sub>IH</sub>	HIGH-level input voltage	V <sub>CC(B)</sub> = 2.7 V to 3.6 V	2.0	-	-	V
		V <sub>CC(A)</sub> = 4.5 V to 5.5 V	2.0	-	-	V
V <sub>IL</sub>	LOW-level input voltage	V <sub>CC(B)</sub> = 2.7 V to 3.6 V	-	-	0.8	V
		V <sub>CC(A)</sub> = 4.5 V to 5.5 V	-	-	0.8	V
V <sub>OH</sub>	HIGH-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		V <sub>CC(B)</sub> = 2.7 V to 3.6 V; I <sub>O</sub> = -100 μA	V <sub>CC(B)</sub> - 0.2	V <sub>CC(B)</sub>	-	V
		V <sub>CC(B)</sub> = 2.7 V; I <sub>O</sub> = -12 mA	V <sub>CC(B)</sub> - 0.5	-	-	V
		V <sub>CC(B)</sub> = 3.0 V; I <sub>O</sub> = -24 mA	V <sub>CC(B)</sub> - 0.8	-	-	V
		V <sub>CC(A)</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = -100 μA	V <sub>CC(A)</sub> - 0.2	V <sub>CC(A)</sub>	-	V
		V <sub>CC(A)</sub> = 4.5 V; I <sub>O</sub> = -12 mA	V <sub>CC(A)</sub> - 0.5	-	-	V
V <sub>OL</sub>	LOW-level output voltage	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>				
		V <sub>CC(B)</sub> = 2.7 V to 3.6 V; I <sub>O</sub> = 100 μA	-	-	0.20	V
		V <sub>CC(B)</sub> = 2.7 V; I <sub>O</sub> = 12 mA	-	-	0.40	V
		V <sub>CC(B)</sub> = 3.0 V; I <sub>O</sub> = 24 mA	-	-	0.55	V
		V <sub>CC(A)</sub> = 4.5 V to 5.5 V; I <sub>O</sub> = 100 μA	-	-	0.20	V
		V <sub>CC(A)</sub> = 4.5 V; I <sub>O</sub> = 12 mA	-	-	0.40	V
I <sub>I</sub>	input leakage current	V <sub>I</sub> = 5.5 V or GND	-	±0.1	±5	μA
I <sub>OZ</sub>	OFF-state output current	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> <sup>[2]</sup>				
		V <sub>CC(B)</sub> = 3.6 V; V <sub>O</sub> = V <sub>CC(B)</sub> or GND	-	±0.1	±5	μA
		V <sub>CC(A)</sub> = 5.5 V; V <sub>O</sub> = V <sub>CC(A)</sub> or GND	-	±0.1	±5	μA
I <sub>CC</sub>	supply current	I <sub>O</sub> = 0 A				
		V <sub>CC(B)</sub> = 3.6 V; other inputs at V <sub>CC(B)</sub> or GND	-	0.1	10	μA
		V <sub>CC(A)</sub> = 5.5 V; other inputs at V <sub>CC(A)</sub> or GND	-	0.1	10	μA

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$\Delta I_{CC}$	additional supply current	per control pin; $I_O = 0$ A	[3]			
		$V_{CC(B)} = 2.7$ V to 3.6 V; $V_I = V_{CC(B)} - 0.6$ V; other inputs at $V_{CC(B)}$ or GND	-	5	500	$\mu$ A
		$V_{CC(A)} = 4.5$ V to 5.5 V; $V_I = V_{CC(A)} - 0.6$ V; other inputs at $V_{CC(A)}$ or GND	-	5	500	$\mu$ A
$C_I$	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance	An and Bn	-	5.0	-	pF
<b><math>T_{amb} = -40</math> °C to <math>+125</math> °C</b>						
$V_{IH}$	HIGH-level input voltage	$V_{CC(B)} = 2.7$ V to 3.6 V	2.0	-	-	V
		$V_{CC(A)} = 4.5$ V to 5.5 V	2.0	-	-	V
$V_{IL}$	LOW-level input voltage	$V_{CC(B)} = 2.7$ V to 3.6 V	-	-	0.8	V
		$V_{CC(A)} = 4.5$ V to 5.5 V	-	-	0.8	V
$V_{OH}$	HIGH-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$V_{CC(B)} = 2.7$ V to 3.6 V; $I_O = -100$ $\mu$ A	$V_{CC(B)} - 0.3$	-	-	V
		$V_{CC(B)} = 2.7$ V; $I_O = -12$ mA	$V_{CC(B)} - 0.65$	-	-	V
		$V_{CC(B)} = 3.0$ V; $I_O = -24$ mA	$V_{CC(B)} - 1.0$	-	-	V
		$V_{CC(A)} = 4.5$ V to 5.5 V; $I_O = -100$ $\mu$ A	$V_{CC(A)} - 0.3$	-	-	V
		$V_{CC(A)} = 4.5$ V; $I_O = -12$ mA	$V_{CC(A)} - 0.65$	-	-	V
$V_{OL}$	LOW-level output voltage	$V_I = V_{IH}$ or $V_{IL}$				
		$V_{CC(B)} = 2.7$ V to 3.6 V; $I_O = 100$ $\mu$ A	-	-	0.30	V
		$V_{CC(B)} = 2.7$ V; $I_O = 12$ mA	-	-	0.60	V
		$V_{CC(B)} = 3.0$ V; $I_O = 24$ mA	-	-	0.80	V
		$V_{CC(A)} = 4.5$ V to 5.5 V; $I_O = 100$ $\mu$ A	-	-	0.30	V
		$V_{CC(A)} = 4.5$ V; $I_O = 12$ mA	-	-	0.60	V
		$V_{CC(A)} = 4.5$ V; $I_O = 24$ mA	-	-	0.80	V
$I_I$	input leakage current	$V_I = 5.5$ V or GND	-	-	$\pm 20$	$\mu$ A
$I_{OZ}$	OFF-state output current	$V_I = V_{IH}$ or $V_{IL}$	[2]			
		$V_{CC(B)} = 3.6$ V; $V_O = V_{CC(B)}$ or GND	-	-	$\pm 20$	$\mu$ A
		$V_{CC(A)} = 5.5$ V; $V_O = V_{CC(A)}$ or GND	-	-	$\pm 20$	$\mu$ A
$I_{CC}$	supply current	$I_O = 0$ A				
		$V_{CC(B)} = 3.6$ V; other inputs at $V_{CC(B)}$ or GND	-	-	40	$\mu$ A
		$V_{CC(A)} = 5.5$ V; other inputs at $V_{CC(A)}$ or GND	-	-	40	$\mu$ A

**Table 6. Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ <sup>[1]</sup>	Max	Unit
$\Delta I_{CC}$	additional supply current	per control pin; $I_O = 0$ A		[3]		
		$V_{CC(B)} = 2.7$ V to 3.6 V; $V_I = V_{CC(B)} - 0.6$ V; other inputs at $V_{CC(B)}$ or GND	-	-	5000	$\mu$ A
		$V_{CC(A)} = 4.5$ V to 5.5 V; $V_I = V_{CC(A)} - 0.6$ V; other inputs at $V_{CC(A)}$ or GND	-	-	5000	$\mu$ A

[1] All typical values are measured at  $V_{CC(A)} = 5.0$  V,  $V_{CC(B)} = 3.3$  V and  $T_{amb} = 25$  °C.

[2] For transceivers, the parameter  $I_{OZ}$  includes the input leakage current.

[3]  $V_{CC(B)} = 2.7$  V to 3.6 V: other inputs at  $V_{CC(B)}$  or GND.

$V_{CC(A)} = 4.5$  V to 5.5 V: other inputs at  $V_{CC(A)}$  or GND.

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

Voltages are referenced to GND (ground = 0 V).  $V_{CC(A)} = 4.5$  V to 5.5 V;  $t_r = t_f \leq 2.5$  ns. For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$	-40 °C to +85 °C			-40 °C to +125 °C		Unit
				Min	Typ <sup>[1]</sup>	Max	Min	Max	
$t_{PHL}$	HIGH to LOW propagation delay	An to Bn; see <a href="#">Figure 6</a>	2.7 V	1.0	3.6	6.3	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.3	6.3	1.0	8.0	ns
		Bn to An; see <a href="#">Figure 6</a>	2.7 V	1.0	3.4	6.1	1.0	8.0	ns
			3.0 V to 3.6 V	1.0	3.4	6.1	1.0	8.0	ns
$t_{PLH}$	LOW to HIGH propagation delay	An to Bn; see <a href="#">Figure 6</a>	2.7 V	1.0	3.3	6.7	1.0	8.5	ns
			3.0 V to 3.6 V	1.0	2.8	6.5	1.0	8.5	ns
		Bn to An; see <a href="#">Figure 6</a>	2.7 V	1.0	3.0	5.0	1.0	6.5	ns
			3.0 V to 3.6 V	1.0	3.0	5.0	1.0	6.5	ns
$t_{PZL}$	OFF-state to LOW propagation delay	$\overline{OE}$ to An; see <a href="#">Figure 7</a>	2.7 V	1.0	4.5	9.0	1.0	11.5	ns
			3.0 V to 3.6 V	1.0	4.5	9.0	1.0	11.5	ns
		$\overline{OE}$ to Bn; see <a href="#">Figure 7</a>	2.7 V	1.0	4.4	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.8	8.1	1.0	10.5	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	$\overline{OE}$ to An; see <a href="#">Figure 7</a>	2.7 V	1.0	4.5	8.1	1.0	10.5	ns
			3.0 V to 3.6 V	1.0	4.5	8.1	1.0	10.5	ns
		$\overline{OE}$ to Bn; see <a href="#">Figure 7</a>	2.7 V	1.0	4.3	8.7	1.0	11.0	ns
			3.0 V to 3.6 V	1.0	3.2	8.1	1.0	10.5	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	$\overline{OE}$ to An; see <a href="#">Figure 7</a>	2.7 V	1.0	2.9	7.0	1.0	9.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.0	1.0	9.0	ns
		$\overline{OE}$ to Bn; see <a href="#">Figure 7</a>	2.7 V	1.0	3.9	7.7	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	3.5	7.7	1.0	10.0	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	$\overline{OE}$ to An; see <a href="#">Figure 7</a>	2.7 V	1.0	2.8	5.8	1.0	7.5	ns
			3.0 V to 3.6 V	1.0	2.8	5.8	1.0	7.5	ns
		$\overline{OE}$ to Bn; see <a href="#">Figure 7</a>	2.7 V	1.0	3.3	7.8	1.0	10.0	ns
			3.0 V to 3.6 V	1.0	2.9	7.8	1.0	10.0	ns

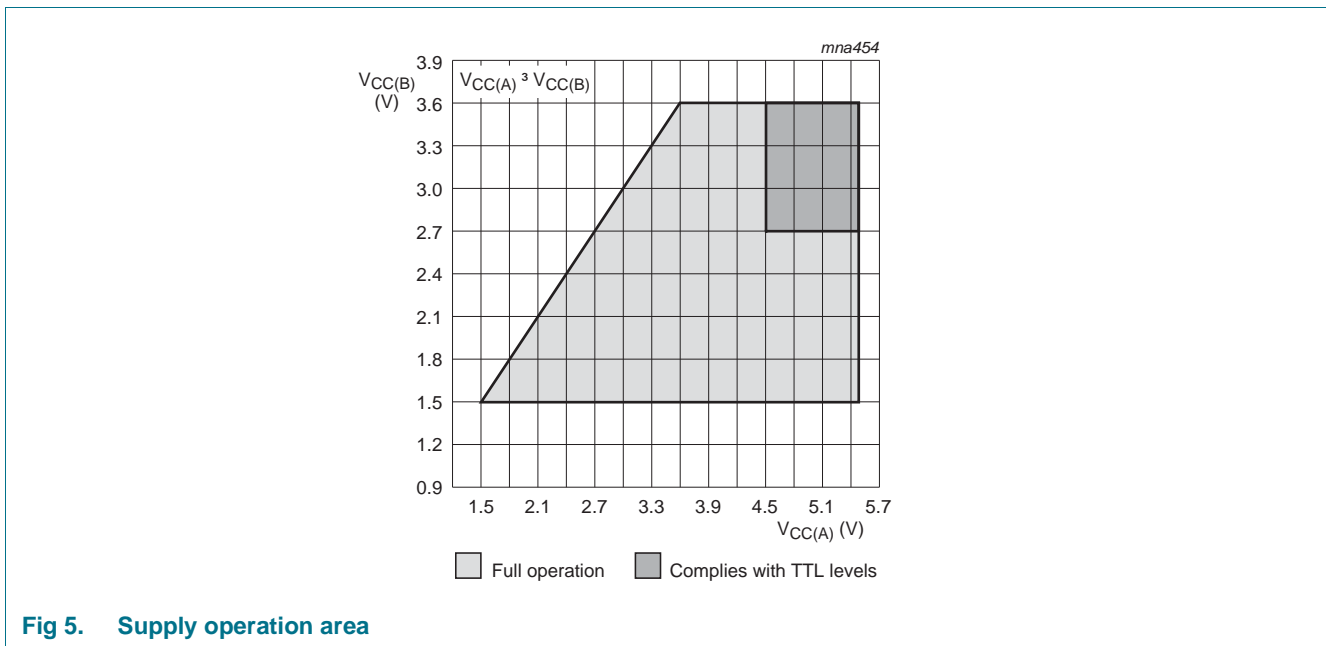
**Table 7. Dynamic characteristics ...continued**

Voltages are referenced to GND (ground = 0 V).  $V_{CC(A)} = 4.5\text{ V to }5.5\text{ V}$ ;  $t_r = t_f \leq 2.5\text{ ns}$ . For test circuit see [Figure 8](#).

Symbol	Parameter	Conditions	$V_{CC(B)}$	-40 °C to +85 °C			-40 °C to +125 °C		Unit		
				Min	Typ <sup>[1]</sup>	Max	Min	Max			
$t_{sk(o)}$	output skew time			[2]	-	-	1.0	-	1.5	ns	
$C_{PD}$	power dissipation capacitance	5 V bus: Bn to An; $V_I = \text{GND to } V_{CC(A)}$ ; $V_{CC(A)} = 5.0\text{ V}$		[3]	outputs enabled	-	17	-	-	-	pF
					outputs disabled	-	5	-	-	-	pF
		3 V bus: An to Bn; $V_I = \text{GND to } V_{CC(B)}$ ; $V_{CC(B)} = 3.3\text{ V}$		[3]	outputs enabled	-	17	-	-	-	pF
					outputs disabled	-	5	-	-	-	pF

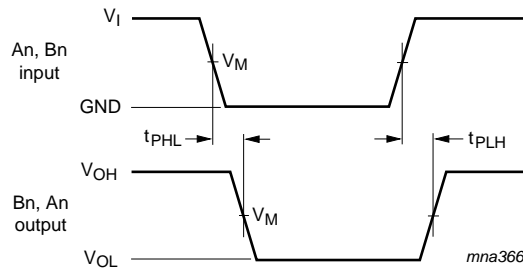
- [1] Typical values are measured at  $T_{amb} = 25\text{ °C}$ ,  $V_{CC(A)} = 5.0\text{ V}$ , and  $V_{CC(B)} = 2.7\text{ V}$  and  $3.3\text{ V}$  respectively.
- [2] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.
- [3]  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ).  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $f_o$  = output frequency in MHz  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in Volts  
 $N$  = number of inputs switching  
 $\Sigma(C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs

## 11. AC waveforms



**Fig 5. Supply operation area**



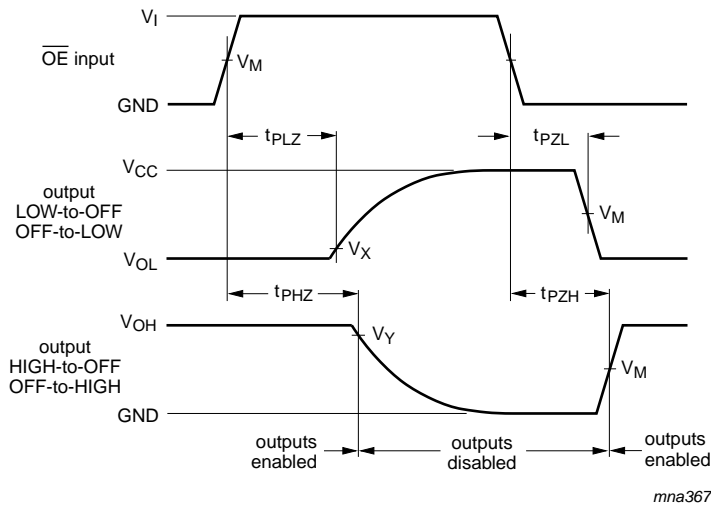


$V_M = 1.5 \text{ V}$  at  $2.7 \text{ V} \leq V_{CC(B)} \leq 3.6 \text{ V}$ ;

$V_M = 0.5 V_{CC(A)}$  at  $V_{CC(A)} \geq 4.5 \text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 6. Input (An, Bn) to output (Bn, An) propagation delays**



$V_M = 1.5 \text{ V}$  at  $2.7 \text{ V} \leq V_{CC(B)} \leq 3.6 \text{ V}$ ;

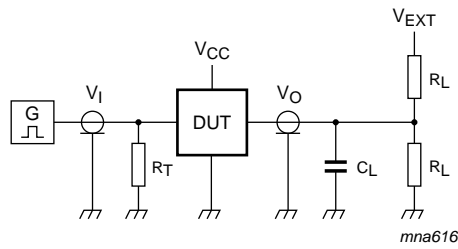
$V_M = 0.5 V_{CC(A)}$  at  $V_{CC(A)} \geq 4.5 \text{ V}$ .

$V_X = V_{OL} + 0.3 \text{ V}$  at  $V_{CC(B)} \geq 2.7 \text{ V}$ ;

$V_Y = V_{OH} - 0.3 \text{ V}$  at  $V_{CC(B)} \geq 2.7 \text{ V}$ .

$V_{OL}$  and  $V_{OH}$  are typical output voltage drops that occur with the output load.

**Fig 7. 3-state enable and disable times**



Test data is given in [Table 8](#). Definitions for test circuit:

$R_L$  = Load resistance.

$C_L$  = Load capacitance including jig and probe capacitance.

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

**Fig 8. Load circuitry for switching times**

**Table 8. Test data**

Supply voltage		Input	Load		$V_{EXT}$		
$V_{CC(A)}$	$V_{CC(B)}$	$V_I$ [1]	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PZH}, t_{PHZ}$	$t_{PZL}, t_{PLZ}$ [2]
< 2.7 V	< 2.7 V	$V_{CCI}$	50 pF	500 $\Omega$	open	GND	$2 \times V_{CCO}$
-	2.7 V to 3.6 V	2.7 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CCO}$
4.5 V to 5.5 V	-	3.0 V	50 pF	500 $\Omega$	open	GND	$2 \times V_{CCO}$

[1]  $V_{CCI}$  is the supply voltage associated with the data input port.

[2]  $V_{CCO}$  is the supply voltage associated with the output port.

12. Package outline

SO24: plastic small outline package; 24 leads; body width 7.5 mm

SOT137-1

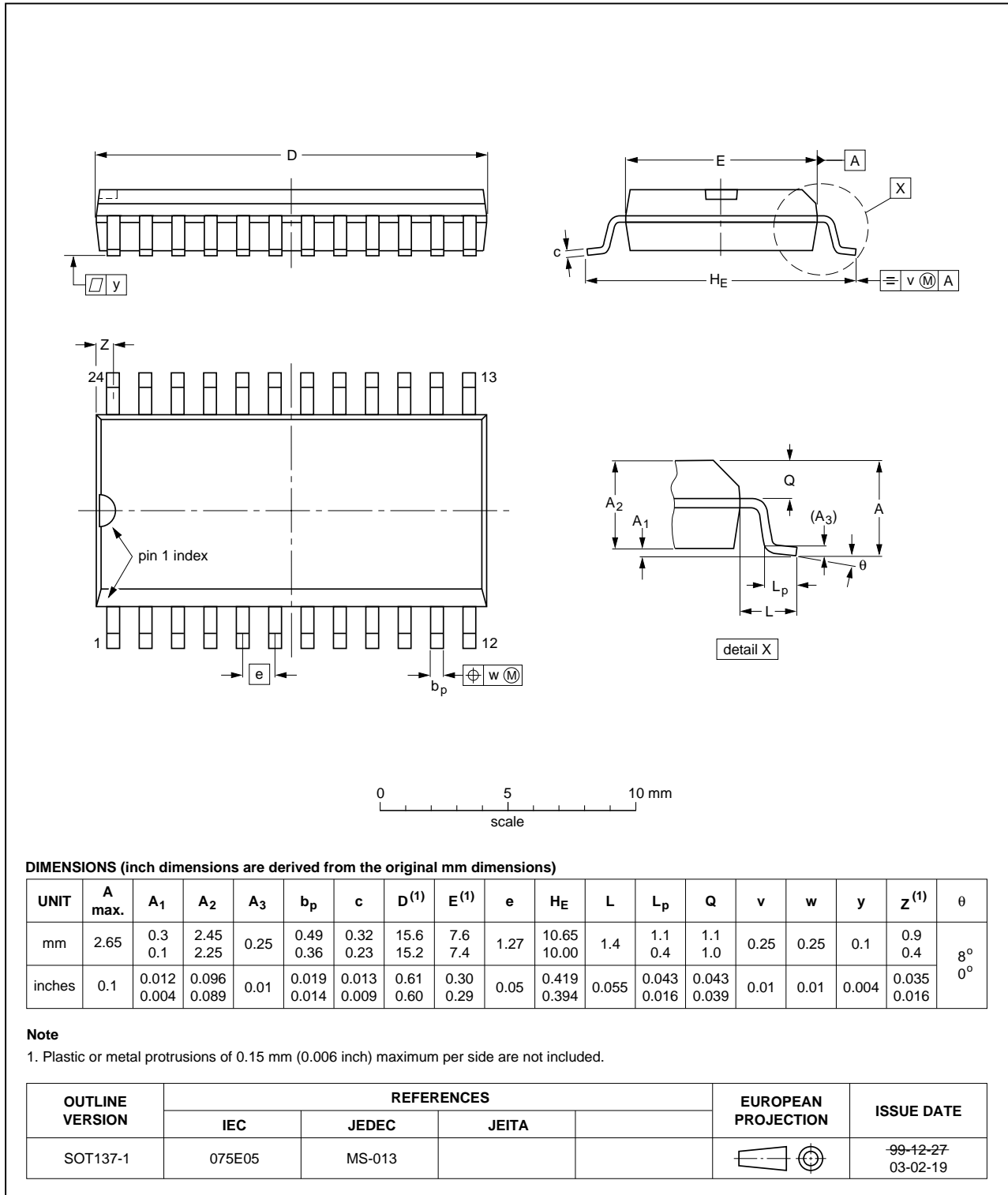


Fig 9. Package outline SOT137-1 (SO24)

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm

SOT340-1

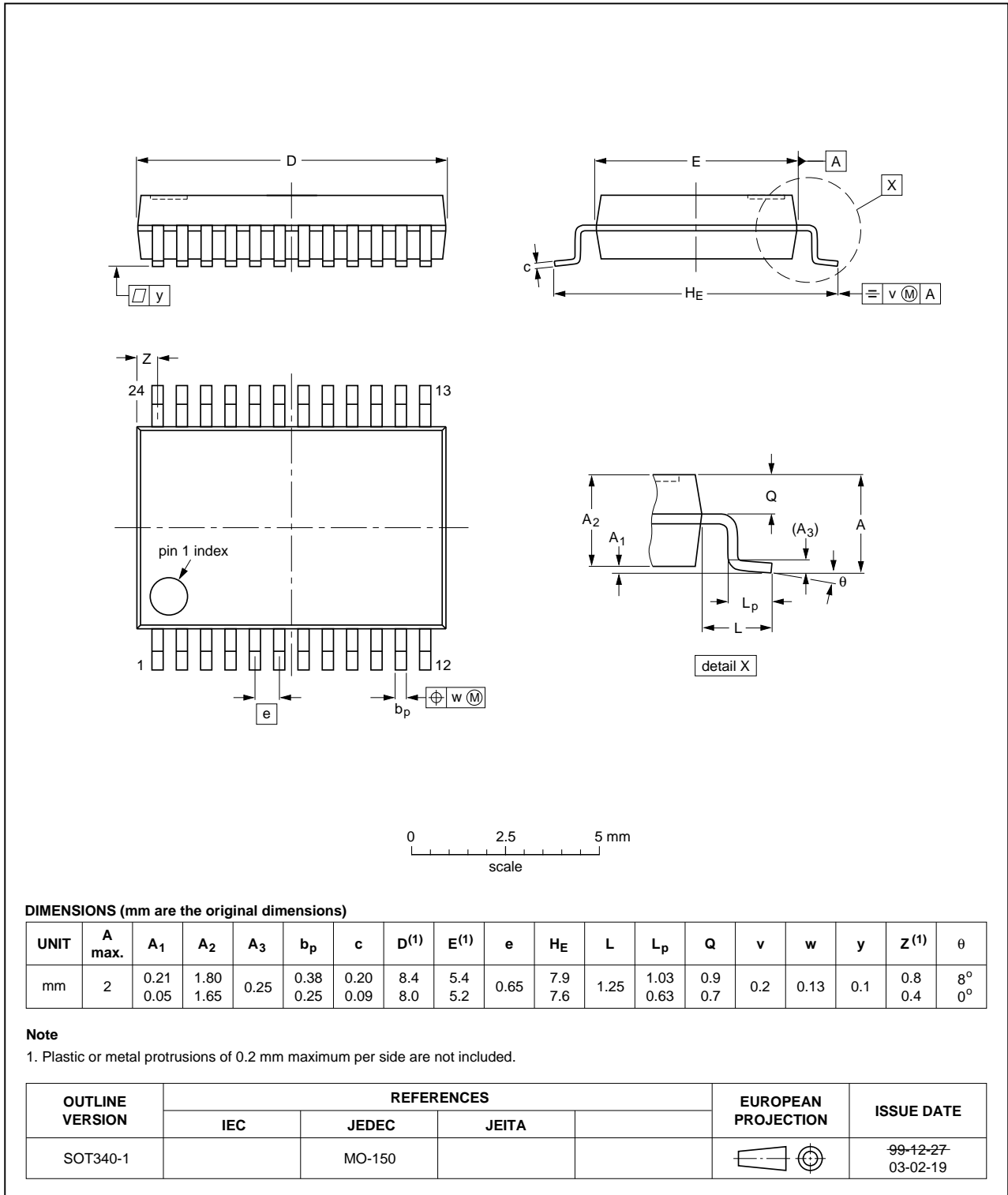


Fig 10. Package outline SOT340-1 (SSOP24)

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

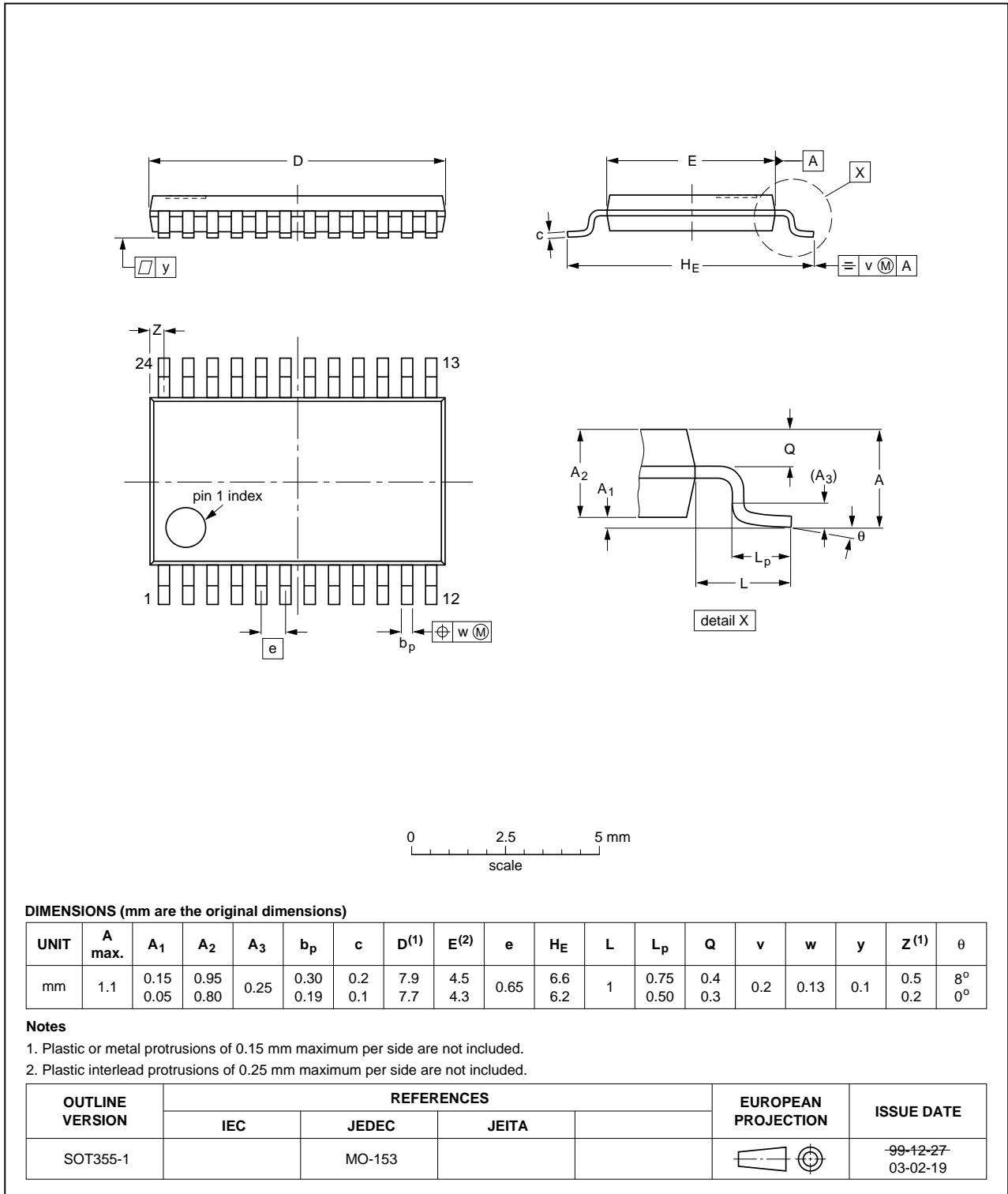


Fig 11. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

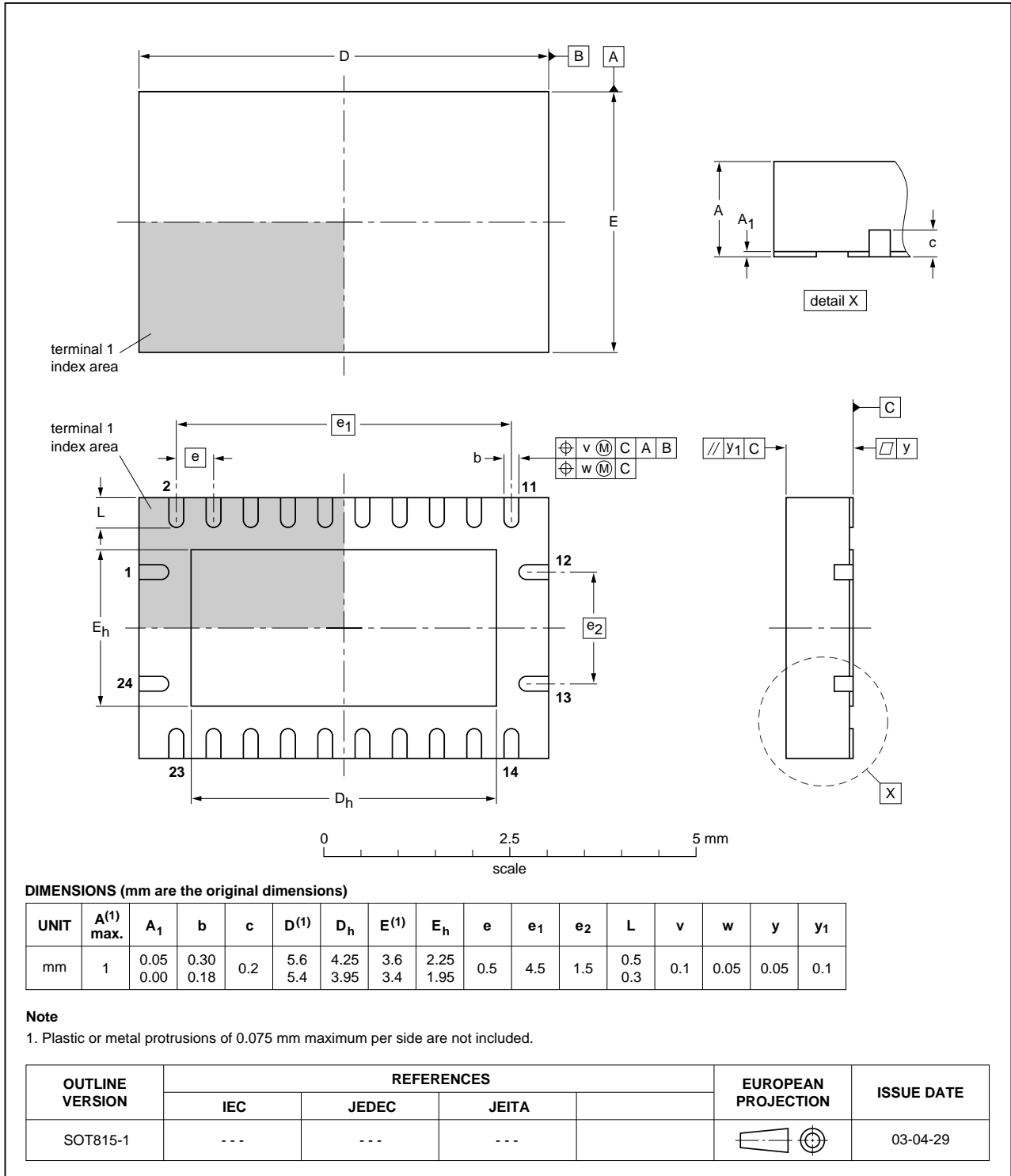


Fig 12. Package outline SOT815-1 (DHVQFN24)

## 13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

## 14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC4245A v.10	20121218	Product data sheet	-	74LVC4245A v.9
Modifications:	<ul style="list-style-type: none"> <li><math>V_{CC(A)}</math> and <math>V_{CC(B)}</math> changed into <math>V_{CC(A)}</math> and <math>V_{CC(B)}</math> (errata)</li> </ul>			
74LVC4245A v.9	20121120	Product data sheet	-	74LVC4245A v.8
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Figure 4</a>: Pin configuration drawing corrected for DHVQFN24 package</li> </ul>			
74LVC4245A v.8	20111122	Product data sheet	-	74LVC4245A v.7
74LVC4245A v.7	20110812	Product data sheet	-	74LVC4245A v.6
74LVC4245A v.6	20080118	Product data sheet	-	74LVC4245A v.5
74LVC4245A v.5	20040330	Product specification	-	74LVC4245A v.4
74LVC4245A v.4	20040211	Product specification	-	74LVC4245A v.3
74LVC4245A v.3	19990615	Product specification	-	74LVC4245A v.2
74LVC4245A v.2	19980729	Product specification	-	74LVC4245A v.1
74LVC4245A v.1	19980729	Product specification	-	-

## 15. Legal information

### 15.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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