

# HEF4050B

## Hex non-inverting buffers

Rev. 8 — 18 November 2011

Product data sheet

### 1. General description

The HEF4050B provides six non-inverting buffers with high current output capability suitable for driving TTL or high capacitive loads. Since input voltages in excess of the buffers' supply voltage are permitted, the buffers may also be used to convert logic levels of up to 15 V to standard TTL levels. Their guaranteed fan-out into common bipolar logic elements is shown in [Table 3](#).

It operates over a recommended  $V_{DD}$  power supply range of 3 V to 15 V referenced to  $V_{SS}$  (usually ground). Unused inputs must be connected to  $V_{DD}$ ,  $V_{SS}$ , or another input.

### 2. Features and benefits

- Accepts input voltages in excess of the supply voltage
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$
- Complies with JEDEC standard JESD 13-B

### 3. Applications

- LOCMOS (Local Oxidation CMOS) to DTL/TTL converter
- HIGH sink current for driving two TTL loads
- HIGH-to-LOW level logic conversion

### 4. Ordering information

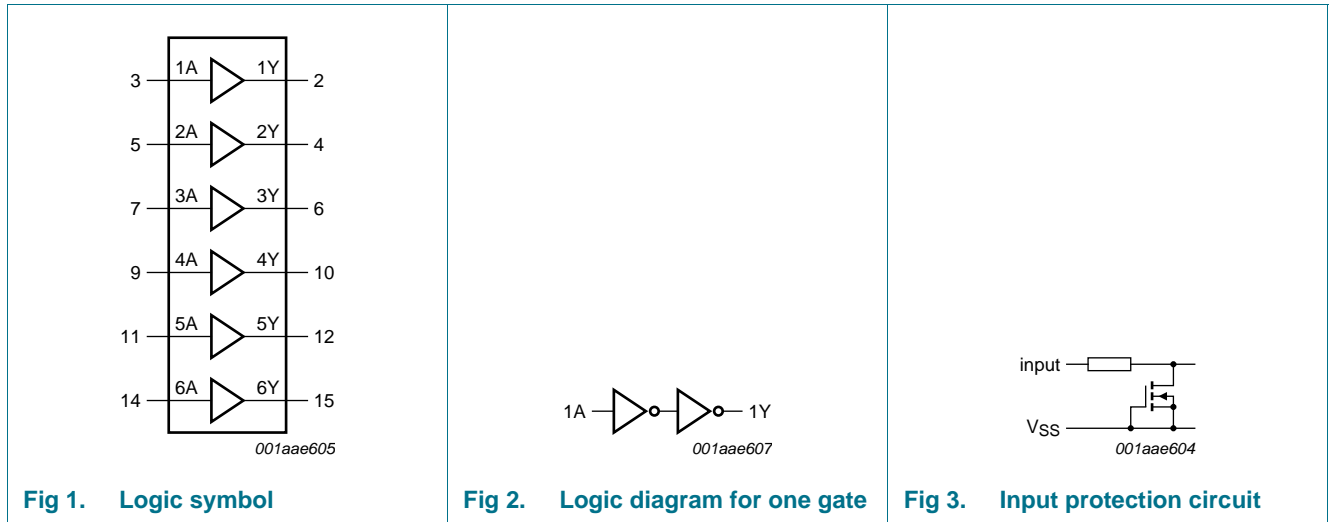
**Table 1. Ordering information**

All types operate from  $-40\text{ }^{\circ}\text{C}$  to  $+85\text{ }^{\circ}\text{C}$ .

Type number	Package		Version
	Name	Description	
HEF4050BP	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
HEF4050BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

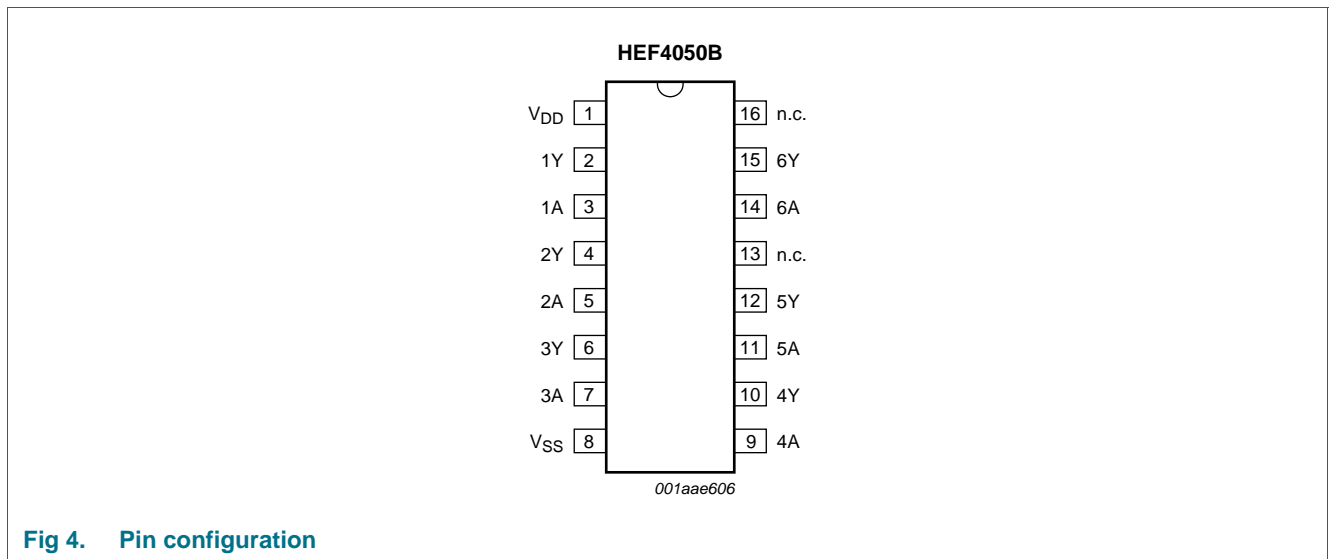


## 5. Functional diagram



## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
V <sub>DD</sub>	1	supply voltage
1Y to 6Y	2, 4, 6, 10, 12, 15	output

Table 2. Pin description ...continued

Symbol	Pin	Description
1A to 6A	3, 5, 7, 9, 11, 14,	input
V <sub>SS</sub>	8	ground supply voltage
n.c.	13, 16	not connected

## 7. Functional description

Table 3. Guaranteed fan-out

Driven element	Guaranteed fan-out
Standard TTL	2
74 LS	9
74 L	16

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DD</sub>	supply voltage		-0.5	+18	V	
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V	
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA	
I <sub>I/O</sub>	input/output current		-	10	mA	
I <sub>DD</sub>	supply current		-	50	mA	
T <sub>stg</sub>	storage temperature		-65	+150	°C	
T <sub>amb</sub>	ambient temperature		-40	+85	°C	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> -40 °C to +85 °C				
		DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output	-	100	mW	

[1] For DIP16 package: P<sub>tot</sub> derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P<sub>tot</sub> derates linearly with 8 mW/K above 70 °C.

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		3	15	V
V <sub>I</sub>	input voltage		0	V <sub>DD</sub>	V
T <sub>amb</sub>	ambient temperature	in free air	-40	+85	°C

Table 5. Recommended operating conditions ...continued

Symbol	Parameter	Conditions	Min	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ }^\circ\text{C}$		$T_{amb} = 25\text{ }^\circ\text{C}$		$T_{amb} = 85\text{ }^\circ\text{C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\text{ }\mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	4.75 V	3.5	-	2.9	-	2.3	-	mA
		$V_O = 0.5\text{ V}$	10 V	12.0	-	10.0	-	8.0	-	mA
		$V_O = 1.5\text{ V}$	15 V	24.0	-	20.0	-	16.0	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	4.0	-	4.0	-	30	$\mu\text{A}$
			10 V	-	8.0	-	8.0	-	60	$\mu\text{A}$
			15 V	-	16.0	-	16.0	-	120	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$ ; for test circuit see [Figure 6](#); unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nA to nY; see <a href="#">Figure 5</a>	5 V	[1] $26\text{ ns} + (0.18\text{ ns/pF})C_L$	-	35	70	ns
			10 V	$16\text{ ns} + (0.08\text{ ns/pF})C_L$	-	20	35	ns
			15 V	$12\text{ ns} + (0.05\text{ ns/pF})C_L$	-	15	30	ns
$t_{PLH}$	LOW to HIGH propagation delay	nA to nY; see <a href="#">Figure 5</a>	5 V	[1] $28\text{ ns} + (0.55\text{ ns/pF})C_L$	-	55	110	ns
			10 V	$14\text{ ns} + (0.23\text{ ns/pF})C_L$	-	25	55	ns
			15 V	$12\text{ ns} + (0.16\text{ ns/pF})C_L$	-	20	40	ns
$t_{THL}$	HIGH to LOW output transition time	see <a href="#">Figure 5</a>	5 V	[1] $7\text{ ns} + (0.35\text{ ns/pF})C_L$	-	25	50	ns
			10 V	$3\text{ ns} + (0.14\text{ ns/pF})C_L$	-	10	20	ns
			15 V	$2\text{ ns} + (0.09\text{ ns/pF})C_L$	-	7	14	ns
$t_{TLH}$	LOW to HIGH output transition time	see <a href="#">Figure 5</a>	5 V	[1] $10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns

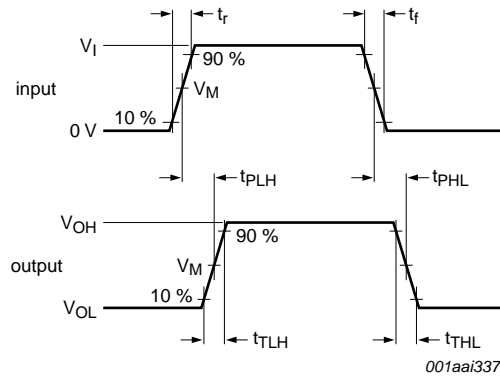
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz,
		10 V	$P_D = 11600 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_o$ = output frequency in MHz,
		15 V	$P_D = 65900 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs.

12. Waveforms

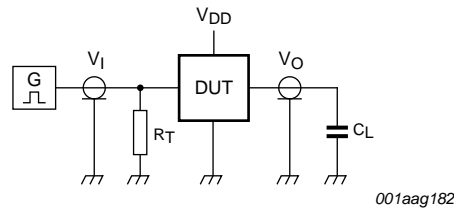


Measurement points are given in [Table 9](#).  
 $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig 5. Input to output propagation delays

Table 9. Measurement points

Input		Output
$V_M$	$V_I$	$V_M$
$0.5V_{DD}$	0 V to $V_{DD}$	$0.5V_{DD}$



Test data is given in [Table 10](#).  
 Definitions for test circuit:  
 $C_L$  = Load capacitance including jig and probe capacitance.  
 $R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator.

Fig 6. Test circuit for switching times

Table 10. Test data

Supply voltage	Input			Load
	$V_I$	$V_M$	$t_r, t_f$	$C_L$
5 V to 15 V	$V_{DD}$	$0.5V_I$	$\leq 20$ ns	50 pF

13. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil)

SOT38-4

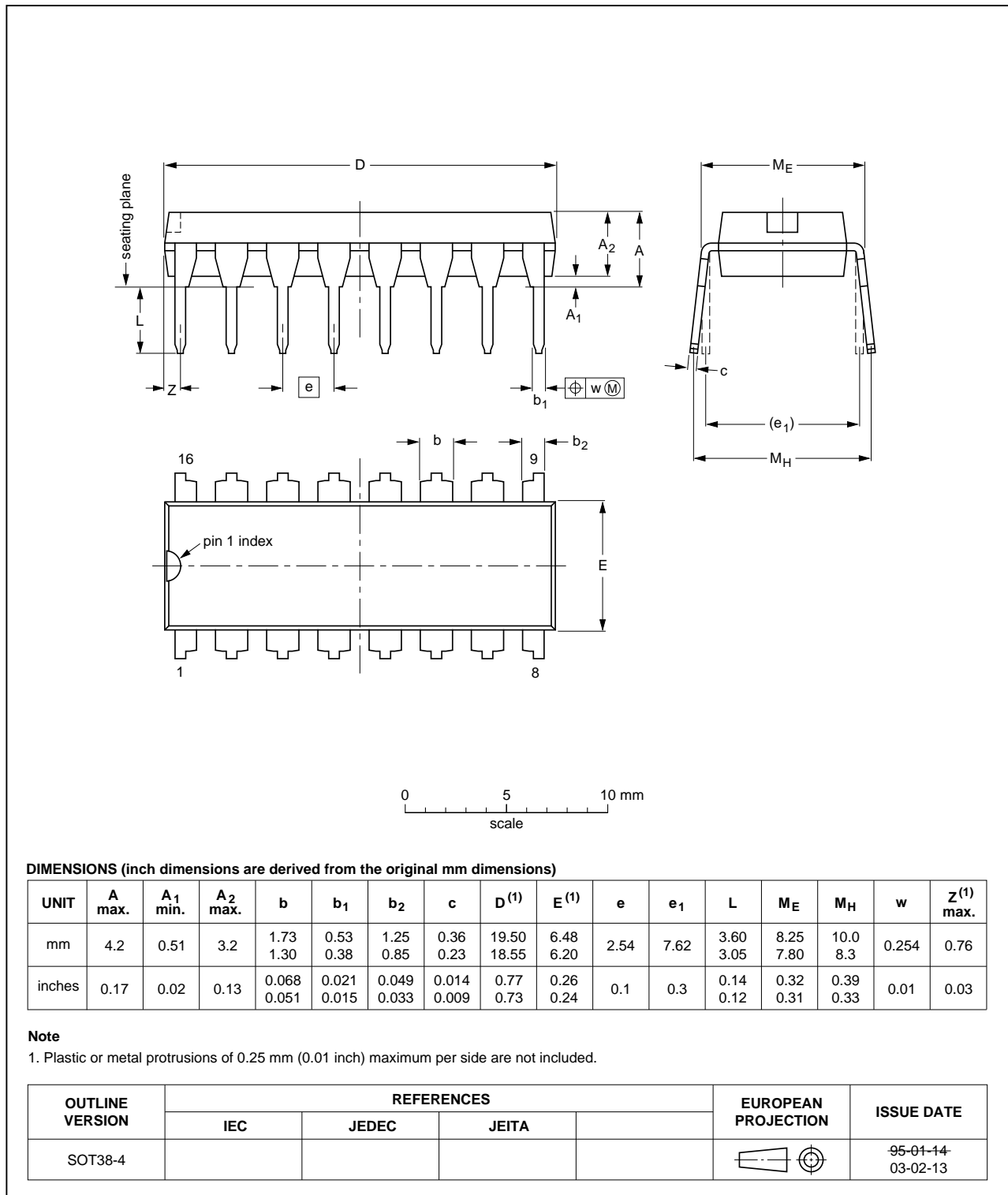


Fig 7. Package outline SOT38-4 (DIP16)

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

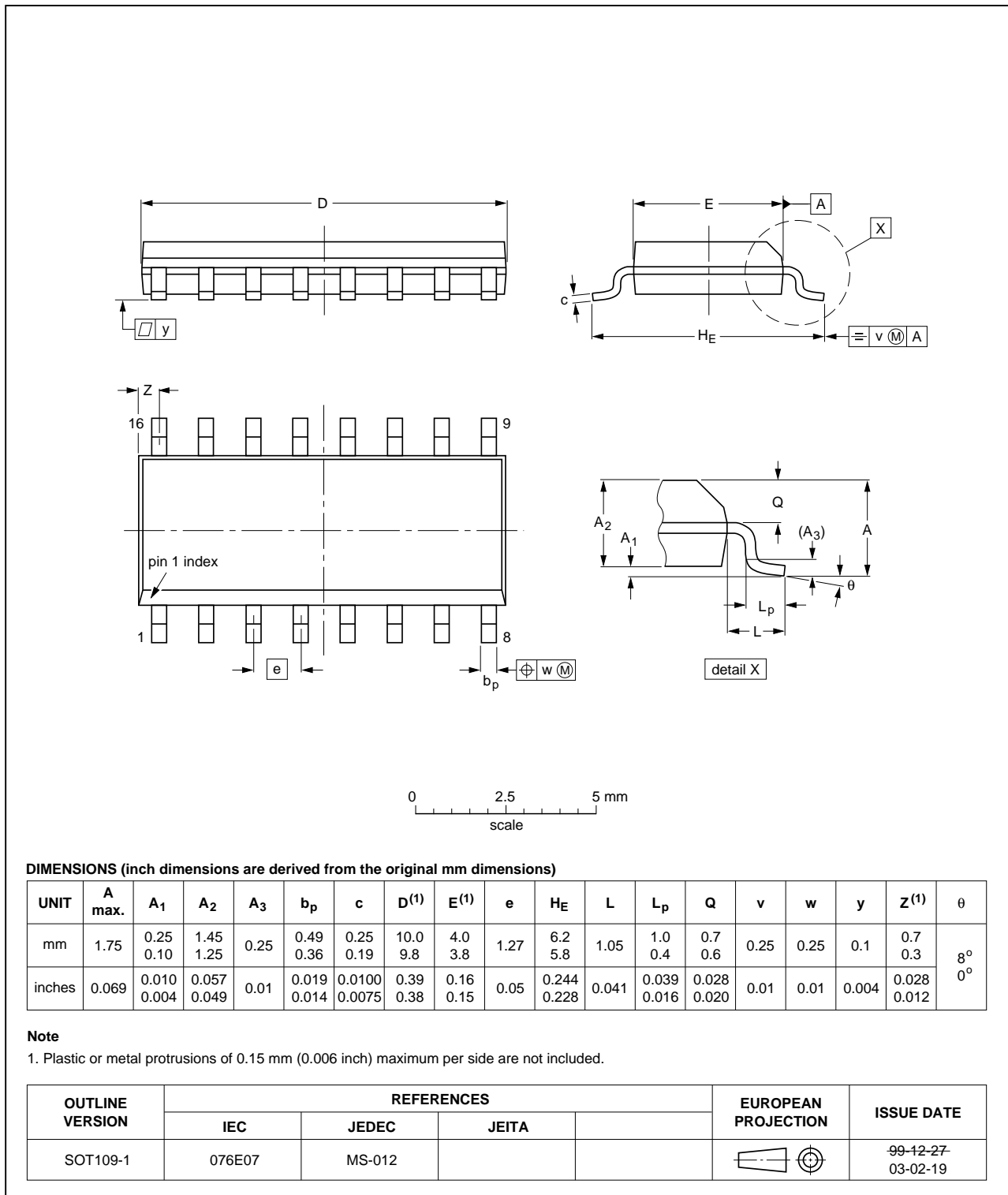


Fig 8. Package outline SOT109-1 (SO16)



## 14. Abbreviations

Table 11. Abbreviations

Acronym	Description
DTL	Diode Transistor Logic
DUT	Device Under Test
LOC MOS	Local Oxidation CMOS
TTL	Transistor-Transistor Logic

## 15. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4050B v.8	20111118	Product data sheet	-	HEF4050B v.7
Modifications:		<ul style="list-style-type: none"><li>• <a href="#">Table 6</a>: I<sub>OH</sub> minimum values changed to maximum</li><li>• <a href="#">Table 11</a>: DUT added</li></ul>		
HEF4050B v.7	20091201	Product data sheet	-	HEF4050B v.6
HEF4050B v.6	20090723	Product data sheet	-	HEF4050B v.5
HEF4050B v.5	20081111	Product data sheet	-	HEF4050B v.4
HEF4050B v.4	20080702	Product data sheet	-	HEF4050B_CNV v.3
HEF4050B_CNV v.3	19950101	Product specification	-	HEF4050B_CNV v.2
HEF4050B_CNV v.2	19950101	Product specification	-	-

## 16. Legal information

### 16.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

### 16.2 Definitions

**Draft** — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet** — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification** — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

### 16.3 Disclaimers

**Limited warranty and liability** — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes** — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use** — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or

malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications** — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values** — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale** — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nxp.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license** — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control** — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products** — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond

NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

## 16.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 17. Contact information

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

## 18. Contents

1	General description . . . . .	1
2	Features and benefits . . . . .	1
3	Applications . . . . .	1
4	Ordering information . . . . .	1
5	Functional diagram . . . . .	2
6	Pinning information . . . . .	2
6.1	Pinning . . . . .	2
6.2	Pin description . . . . .	2
7	Functional description . . . . .	3
8	Limiting values . . . . .	3
9	Recommended operating conditions . . . . .	3
10	Static characteristics . . . . .	4
11	Dynamic characteristics . . . . .	5
12	Waveforms . . . . .	6
13	Package outline . . . . .	7
14	Abbreviations . . . . .	9
15	Revision history . . . . .	9
16	Legal information . . . . .	10
16.1	Data sheet status . . . . .	10
16.2	Definitions . . . . .	10
16.3	Disclaimers . . . . .	10
16.4	Trademarks . . . . .	11
17	Contact information . . . . .	11
18	Contents . . . . .	12

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2011.

All rights reserved.

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: 18 November 2011

Document identifier: HEF4050B

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Bus Transmitters](#) category:*

*Click to view products by [NXP](#) manufacturer:*

Other Similar products are found below :

[NLV7SB3257DTT1G](#) [7SB3257DTT2G](#) [7SB3257DTT1G](#) [7SB385DTT1G](#) [74HC1G125GW](#) [74AHC125D.112](#) [74AHC244D.112](#)  
[74AHC245D.112](#) [74AHC541D.112](#) [74HC245D.652](#) [74HCT365D.652](#) [74ABT125D.602](#) [74ABT16245BDGG.112](#) [74AHCT245D.112](#)  
[74HC245PW.112](#) [74HC367D.652](#) [74HC541D.652](#) [74HC541D.653](#) [74HC7541D.112](#) [74HCT367D.652](#) [74HCT541D.653](#) [74LVC244AD.112](#)  
[74LVC4245AD.112](#) [74LVC541AD.112](#) [74HC240D.652](#) [74HC4049D.653](#) [74HC540D.652](#) [74HCT125D.652](#) [74HCT244D.652](#)  
[74HCT245PW.112](#) [74HCT367N.652](#) [74HC125D.652](#) [74HC244D.652](#) [74HC245DB.118](#) [HEF4050BT.652](#) [74HC05PW.112](#) [74HC125PW.112](#)  
[74HC2G16GVH](#) [74LVC06AD.112](#) [74LVC06APW.112](#) [74LVC125APW.112](#) [74LVC126APW.112](#) [74VHC126FT\(BE\)](#) [7SB3257MUTCG](#)  
[7SB384MUTCG](#) [7SB384DTT1G](#) [74AHCT245PW.118](#) [74HC126DB.118](#) [74HC240PW.112](#) [74HC241DB.118](#)