1. General description

The HEF4081B is a quad 2-input AND gate. The outputs are fully buffered for highest noise immunity and pattern insensitivity to output impedance variations.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Inputs and outputs are protected against electrostatic effects
- Specified from -40 °C to +85 °C and -40 °C to +125 °C
- Complies with JEDEC standard JESD 13-B

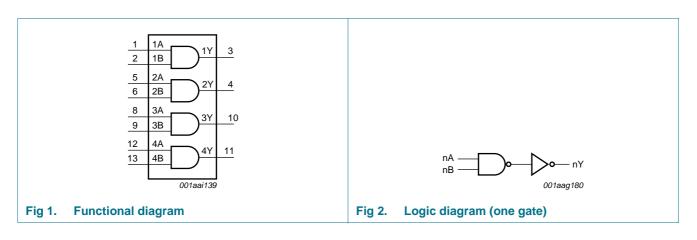
3. Ordering information

Table 1.Ordering information

All types operate from -40 °C to +125 °C.

Type number	Package						
	Name	Description	Version				
HEF4081BP	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1				
HEF4081BT	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1				

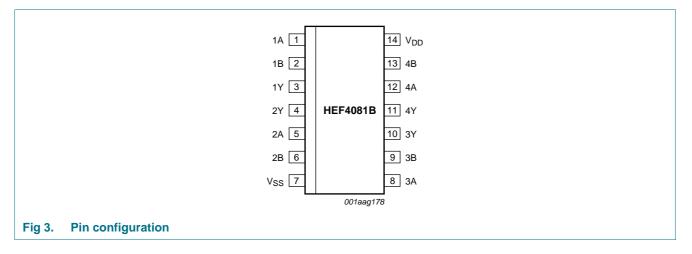
4. Functional diagram





5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2.	Pin description		
Symbol	Pin	Description	
1A to 4A	1, 5, 8, 12	input	
1B to 4B	2, 6, 9, 13	input	
1Y to 4Y	3, 4, 10, 11	output	
V _{SS}	7	ground (0 V)	
V _{DD}	14	supply voltage	

6. Functional description

Table 3. Function table^[1]

Input		Output
nA	nB	nY
L	L	L
L	Н	L
Н	L	L
Н	Н	Н

[1] H = HIGH voltage level; L = LOW voltage level.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to $V_{SS} = 0 V$ (ground).

					-
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{\rm I}$ < –0.5 V or $V_{\rm I}$ > $V_{\rm DD}$ + 0.5 V	-	±10	mA
VI	input voltage		-0.5	$V_{DD} + 0.5$	V
I _{OK}	output clamping current	$V_{\rm O}$ < –0.5 V or $V_{\rm O}$ > $V_{\rm DD}$ + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mA
I _{DD}	supply current		-	50	mA
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+125	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to + 125 °C			
		DIP14	<u>[1]</u> _	750	mW
		SO14	[2] _	500	mW
Р	power dissipation	per output	-	100	mW

[1] For DIP14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 12 mW/K.

[2] For SO14 packages: above T_{amb} = 70 °C, P_{tot} derates linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

	1 0				
Symbol	Parameter	Conditions	Min	Max	Unit
V _{DD}	supply voltage		3	15	V
VI	input voltage		0	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5 V$	-	3.75	μs/V
		V _{DD} = 10 V	-	0.5	μs/V
		V _{DD} = 15 V	-	0.08	μs/V
-					

9. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	–40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} =	+125 °C	Unit
				Min	Мах	Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level	$ I_0 < 1 \ \mu A$	5 V	3.5	-	3.5	-	3.5	-	3.5	-	V
	input voltage		10 V	7.0	-	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level		5 V	-	1.5	-	1.5	-	1.5	-	1.5	V
input voltage	input voltage		10 V	-	3.0	-	3.0	-	3.0	-	3.0	V
		15 V	-	4.0	-	4.0	-	4.0	-	4.0	V	

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Symbol	Parameter	Conditions	V _{DD}	T _{amb} =	−40 °C	T _{amb} =	+25 °C	T _{amb} =	+85 °C	T _{amb} = ·	⊦125 °C	Unit
				Min	Max	Min	Max	Min	Max	Min	Max	
V _{OH}	HIGH-level	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	4.95	-	V
	output voltage		10 V	9.95	-	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	14.95	-	V
V _{OL}	LOW-level	$ I_0 < 1 \ \mu A$	5 V	-	0.05	-	0.05	-	0.05	-	0.05	V
	output voltage		10 V	-	0.05	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	$V_O = 2.5 V$	5 V	-	-1.7	-	-1.4	-	-1.1	-	-1.1	mA
		$V_{O} = 4.6 V$	5 V	-	-0.64	-	-0.5	-	-0.36	-	-0.36	mA
		$V_O = 9.5 V$	10 V	-	-1.6	-	-1.3	-	-0.9	-	-0.9	mA
		$V_{O} = 13.5 V$	15 V	-	-4.2	-	-3.4	-	-2.4	-	-2.4	mA
I _{OL}	LOW-level output current	$V_{O} = 0.4 V$	5 V	0.64	-	0.5	-	0.36	-	0.36	-	mA
		$V_O = 0.5 V$	10 V	1.6	-	1.3	-	0.9	-	0.9	-	mA
		$V_{O} = 1.5 V$	15 V	4.2	-	3.4	-	2.4	-	2.4	-	mA
l _l	input leakage current		15 V	-	±0.1	-	±0.1	-	±1.0	-	±1.0	μA
I _{DD}	supply current	all valid input	5 V	-	0.25	-	0.25	-	7.5	-	7.5	μA
		combinations; I _O = 0 A	10 V	-	0.5	-	0.5	-	15.0	-	15.0	μA
			15 V	-	1.0	-	1.0	-	30.0	-	30.0	μA
CI	input capacitance			-	-	-	7.5	-	-	-	-	pF

Table 6. Static characteristics ...continued

 $V_{SS} = 0$ V; $V_I = V_{SS}$ or V_{DD} ; unless otherwise specified.

10. Dynamic characteristics

Table 7. Dynamic characteristics

 $T_{amb} = 25 \text{ °C}$; for waveforms see <u>Figure 4</u>; for test circuit see <u>Figure 5</u>; unless otherwise specified. [1]

					•			
Symbol	Parameter	Conditions	V _{DD}	Extrapolation formula	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	nA or nB to nY	5 V	28 ns + (0.55 ns/pF)C _L	-	55	110	ns
	propagation delay		10 V	14 ns + (0.23 ns/pF)C _L	-	25	50	ns
			15 V	12 ns + (0.16 ns/pF)C _L	-	20	40	ns
t _{PLH}	LOW to HIGH	nA or nB to nY	5 V	18 ns + (0.55 ns/pF)C _L	-	45	90	ns
	propagation delay		10 V	9 ns + (0.23 ns/pF)C _L	-	20	40	ns
			15 V	7 ns + (0.16 ns/pF)C _L	-	15	30	ns
t _{THL}	HIGH to LOW output		5 V	10 ns + (1.0 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _{TLH} LOW to HIGH of	LOW to HIGH output		5 V	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
	transition time		10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns

[1] The typical value of the propagation delay and output transition time can be calculated with the extrapolation formula (C_L in pF).

Table 8. Dynamic power dissipation

 $V_{SS} = 0 V; t_r = t_f \le 20 ns; T_{amb} = 25$ °C.

Symbol	Parameter	V_{DD}	Typical formula	where:
PD	dynamic power dissipation	5 V	$P_D = 450 \times f_i + \Sigma (f_o \times C_L) \times V_DD^2 \ (\muW)$	f_i = input frequency in MHz;
		10 V	$P_D = 2900 \times f_i + \Sigma(f_o \times C_L) \times V_DD^2 \ (\muW)$	$f_o = output frequency in MHz;$
		15 V	$P_D = 11700 \times f_i + \Sigma(f_o \times C_L) \times V_DD^2 \ (\muW)$	C_L = output load capacitance in pF;
				$\Sigma(f_o \times C_L)$ = sum of the outputs;
				V_{DD} = supply voltage in V.

11. Waveforms

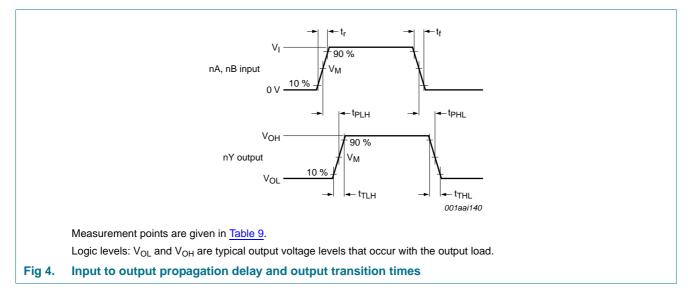


Table 9. Measurement points

Supply voltage	Input	Output
V _{DD}	V _M	V _M
5 V to 15 V	0.5V _{DD}	0.5V _{DD}

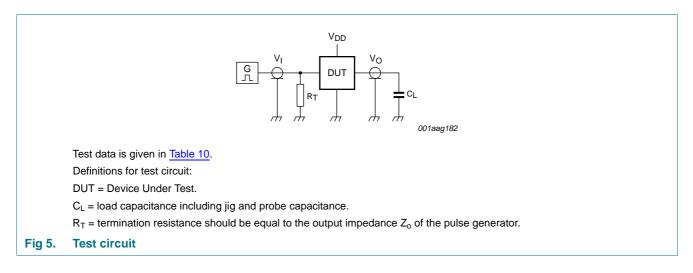


Table 10. Test data

Supply voltage	Input	Load	
V _{DD}	VI	t _r , t _f	CL
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

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12. Package outline

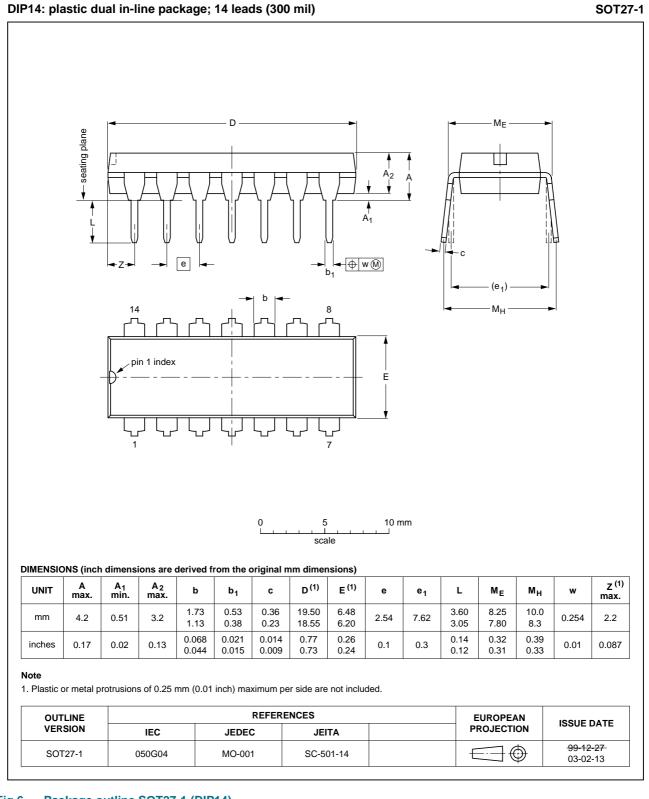
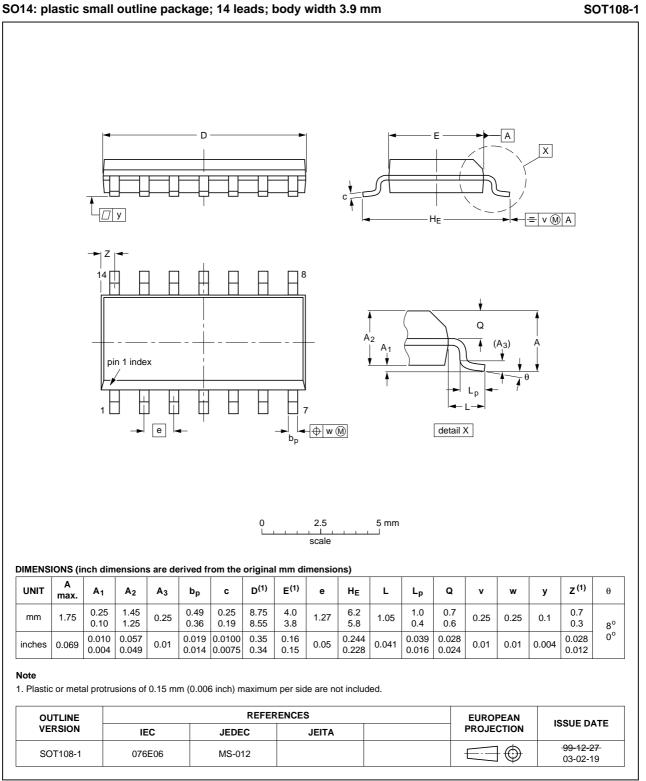


Fig 6. Package outline SOT27-1 (DIP14)

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SO14: plastic small outline package; 14 leads; body width 3.9 mm

Package outline SOT108-1 (SO14) Fig 7.

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13. Revision history

Table 11. Revision history **Document ID Release date** Data sheet status **Change notice Supersedes** HEF4081B v.7 20111116 Product data sheet HEF4081B v.6 _ Modifications: • Table 6: I_{OH} minimum values changed to maximum HEF4081B v.6 Product data sheet HEF4081B v.5 20091202 -HEF4081B v.5 20090629 Product data sheet HEF4081B v.4 -HEF4081B v.4 Product data sheet HEF4081B_CNV v.3 20080526 -HEF4081B_CNV v.3 Product specification HEF4081B_CNV v.2 19950101 -HEF4081B_CNV v.2 19950101 Product specification --

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