# HEF4520B

## Dual binary counter

Rev. 6 — 18 November 2011 Product data sheet

## 1. General description

The HEF4520B is a dual 4-bit internally synchronous binary counter. The counter has an active HIGH clock input (nCP0) and an active LOW clock input (n$\overline{CP}$1), buffered outputs from all four bit positions (nQ0 to nQ3) and an active HIGH overriding asynchronous master reset input (nMR).

The counter advances on either the LOW-to-HIGH transition of the nCP0 input if n$\overline{CP}$1 is HIGH or the HIGH-to-LOW transition of the n$\overline{CP}$1 input if nCP0 is LOW. Either nCP0 or n$\overline{CP}$1 may be used as the clock input to the counter while the other clock input may be used as a clock enable input. Schmitt trigger action makes the clock input highly tolerant of slower clock rise and fall times. A HIGH on nMR resets the counter (nQ0 to nQ3 = LOW) independent of nCP0 and n$\overline{CP}$1.

It operates over a recommended $V_{DD}$ power supply range of 3 V to 15 V referenced to $V_{SS}$ (usually ground). Unused inputs must be connected to $V_{DD}$, $V_{SS}$, or another input.

## 2. Features and benefits

- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

## 3. Ordering information

**Table 1. Ordering information**

*All types operate from −40 °C to +85 °C.*

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| HEF4520BP | DIP16 | plastic dual in-line package; 16 leads (300 mil) | SOT38-4 |
| HEF4520BT | SO16 | plastic small outline package; 16 leads; body width 3.9 mm | SOT109-1 |

## 4. Functional diagram

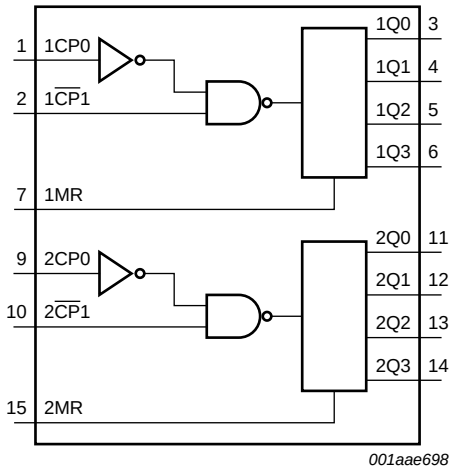



**Fig 1. Functional diagram**

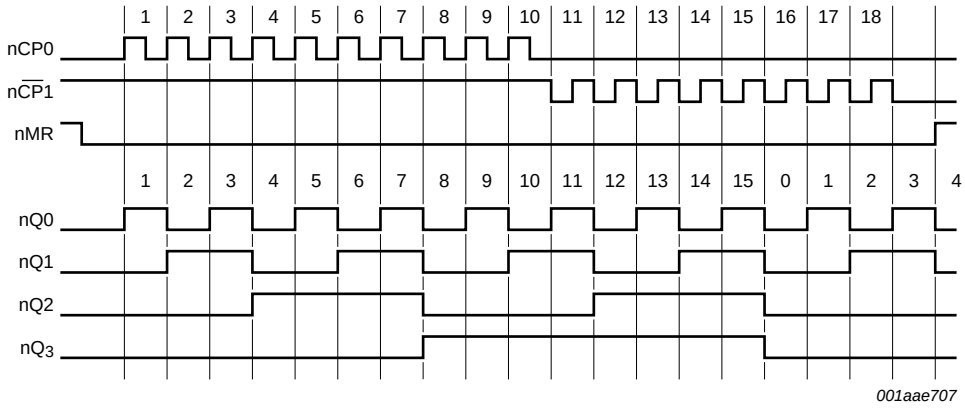



**Fig 2. Timing diagram**

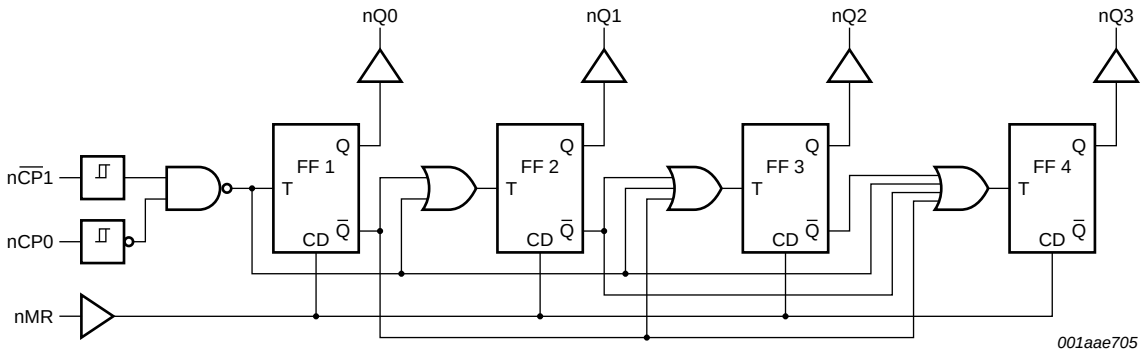



**Fig 3. Logic diagram for one counter**

# 5. Pinning information

## 5.1 Pinning

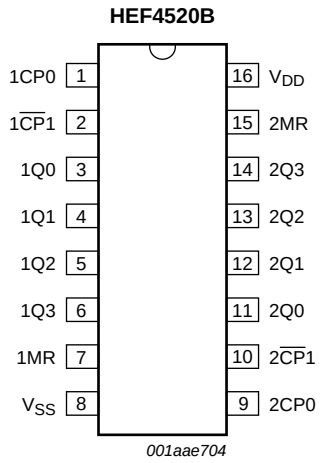



**Fig 4. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| 1CP0, 2CP0 | 1, 9 | clock input (LOW-to-HIGH triggered) |
| $1\overline{CP}1$, $2\overline{CP}1$ | 2, 10 | clock input (HIGH-to-LOW triggered) |
| 1Q0 to 1Q3 | 3, 4, 5, 6 | output |
| 1MR, 2MR | 7, 15 | master reset input |
| $V_{SS}$ | 8 | ground supply voltage |
| 2Q0 to 2Q3 | 11, 12, 13, 14 | output |
| $V_{DD}$ | 16 | supply voltage |

# 6. Functional description

**Table 3. Function table[1]**

| nCP0 | $n\overline{CP}1$ | nMR | Mode |
|---|---|---|---|
| ↑ | H | L | counter advances |
| L | ↓ | L | counter advances |
| ↓ | X | L | no change |
| X | ↑ | L | no change |
| ↑ | L | L | no change |
| H | ↓ | L | no change |
| X | X | H | nQ0 to nQ3 = LOW |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition; ↓ = negative-going transition.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | | −0.5 | +18 | V |
| $I_{IK}$ | input clamping current | $V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $V_I$ | input voltage | | | −0.5 | $V_{DD} + 0.5$ | V |
| $I_{OK}$ | output clamping current | $V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V | | - | ±10 | mA |
| $I_{I/O}$ | input/output current | | | - | ±10 | mA |
| $I_{DD}$ | supply current | | | - | 50 | mA |
| $T_{stg}$ | storage temperature | per output | | −65 | +150 | °C |
| $T_{amb}$ | ambient temperature | | | −40 | +85 | °C |
| $P_{tot}$ | total power dissipation | DIP16 package | [1] | - | 750 | mW |
| | | SO16 package | [2] | - | 500 | mW |
| P | power dissipation | | | - | 100 | mW |

[1] For DIP16 package: $P_{tot}$ derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: $P_{tot}$ derates linearly with 8 mW/K above 70 °C.

## 8. Recommended operating conditions

**Table 5. Recommended operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | 3 | - | 15 | V |
| $V_I$ | input voltage | | 0 | - | $V_{DD}$ | V |
| $T_{amb}$ | ambient temperature | in free air | −40 | - | +85 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{DD}$ = 5 V | - | - | 3.75 | µs/V |
| | | $V_{DD}$ = 10 V | - | - | 0.5 | µs/V |
| | | $V_{DD}$ = 15 V | - | - | 0.08 | µs/V |

## 9. Static characteristics

**Table 6. Static characteristics**

*$V_{SS}$ = 0 V; $V_I$ = $V_{SS}$ or $V_{DD}$ unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | $T_{amb}$ = –40 °C | | $T_{amb}$ = 25 °C | | $T_{amb}$ = 85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Max | Min | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $\|I_O\|$ < 1 μA | 5 V | 3.5 | - | 3.5 | - | 3.5 | - | V |
| | | | 10 V | 7.0 | - | 7.0 | - | 7.0 | - | V |
| | | | 15 V | 11.0 | - | 11.0 | - | 11.0 | - | V |
| $V_{IL}$ | LOW-level input voltage | $\|I_O\|$ < 1 μA | 5 V | - | 1.5 | - | 1.5 | - | 1.5 | V |
| | | | 10 V | - | 3.0 | - | 3.0 | - | 3.0 | V |
| | | | 15 V | - | 4.0 | - | 4.0 | - | 4.0 | V |
| $V_{OH}$ | HIGH-level output voltage | $\|I_O\|$ < 1 μA; $V_I$ = $V_{SS}$ or $V_{DD}$ | 5 V | 4.95 | - | 4.95 | - | 4.95 | - | V |
| | | | 10 V | 9.95 | - | 9.95 | - | 9.95 | - | V |
| | | | 15 V | 14.95 | - | 14.95 | - | 14.95 | - | V |
| $V_{OL}$ | LOW-level output voltage | $\|I_O\|$ < 1 μA; $V_I$ = $V_{SS}$ or $V_{DD}$ | 5 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 10 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| | | | 15 V | - | 0.05 | - | 0.05 | - | 0.05 | V |
| $I_{OH}$ | HIGH-level output current | $V_O$ = 2.5 V | 5 V | - | –1.7 | - | –1.4 | - | –1.1 | mA |
| | | $V_O$ = 4.6 V | 5 V | - | –0.52 | - | –0.44 | - | –0.36 | mA |
| | | $V_O$ = 9.5 V | 10 V | - | –1.3 | - | –1.1 | - | –0.9 | mA |
| | | $V_O$ = 13.5 V | 15 V | - | –3.6 | - | –3.0 | - | –2.4 | mA |
| $I_{OL}$ | LOW-level output current | $V_O$ = 0.4 V | 5 V | 0.52 | - | 0.44 | - | 0.36 | - | mA |
| | | $V_O$ = 0.5 V | 10 V | 1.3 | - | 1.1 | - | 0.9 | - | mA |
| | | $V_O$ = 1.5 V | 15 V | 3.6 | - | 3.0 | - | 2.4 | - | mA |
| $I_I$ | input leakage current | $V_{DD}$ = 15 V | 15 V | - | ±0.3 | - | ±0.3 | - | ±1.0 | μA |
| $I_{DD}$ | supply current | $I_O$ = 0 A; $V_I$ = $V_{SS}$ or $V_{DD}$ | 5 V | - | 20 | - | 20 | - | 150 | μA |
| | | | 10 V | - | 40 | - | 40 | - | 300 | μA |
| | | | 15 V | - | 80 | - | 80 | - | 600 | μA |
| $C_I$ | input capacitance | | - | - | - | - | 7.5 | - | - | pF |

## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 6; unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | Extrapolation formula | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| $t_{PHL}$ | HIGH to LOW propagation delay | nCP0, $\overline{nCP1}$ → nQn; see Figure 5 | 5 V [1] | 83 ns + (0.55 ns/pF)$C_L$ | - | 110 | 220 | ns |
| | | | 10 V | 39 ns + (0.23 ns/pF)$C_L$ | - | 50 | 100 | ns |
| | | | 15 V | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| | | nMR → nQn; see Figure 5 | 5 V | 48 ns + (0.55 ns/pF)$C_L$ | - | 75 | 150 | ns |
| | | | 10 V | 24 ns + (0.23 ns/pF)$C_L$ | - | 35 | 70 | ns |
| | | | 15 V | 17 ns + (0.16 ns/pF)$C_L$ | - | 25 | 50 | ns |

**Table 7. Dynamic characteristics** *...continued*

*$V_{SS}$ = 0 V; $T_{amb}$ = 25 °C; for test circuit see Figure 6; unless otherwise specified.*

| Symbol | Parameter | Conditions | $V_{DD}$ | | Extrapolation formula | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$ | LOW to HIGH propagation delay | nCP0, $\overline{nCP1}$ → nQn; see Figure 5 | 5 V | [1] | 83 ns + (0.55 ns/pF)$C_L$ | - | 110 | 220 | ns |
| | | | 10 V | | 39 ns + (0.23 ns/pF)$C_L$ | - | 50 | 100 | ns |
| | | | 15 V | | 32 ns + (0.16 ns/pF)$C_L$ | - | 40 | 80 | ns |
| $t_t$ | transition time | nQn; see Figure 5 | 5 V | [1] | 10 ns + (1.00 ns/pF)$C_L$ | - | 60 | 120 | ns |
| | | | 10 V | | 9 ns + (0.42 ns/pF)$C_L$ | - | 30 | 60 | ns |
| | | | 15 V | | 6 ns + (0.28 ns/pF)$C_L$ | - | 20 | 40 | ns |
| $t_W$ | pulse width | nCP0 input LOW; minimum width; see Figure 5 | 5 V | | | 60 | 30 | - | ns |
| | | | 10 V | | | 30 | 15 | - | ns |
| | | | 15 V | | | 20 | 10 | - | ns |
| | | $\overline{nCP1}$ input HIGH; minimum width; see Figure 5 | 5 V | | | 60 | 30 | - | ns |
| | | | 10 V | | | 30 | 15 | - | ns |
| | | | 15 V | | | 20 | 10 | - | ns |
| | | nMR input HIGH; minimum width; see Figure 5 | 5 V | | | 30 | 15 | - | ns |
| | | | 10 V | | | 20 | 10 | - | ns |
| | | | 15 V | | | 16 | 8 | - | ns |
| $t_{su}$ | set-up time | nCP0 → $\overline{nCP1}$; see Figure 5 | 5 V | | | 50 | 25 | - | ns |
| | | | 10 V | | | 30 | 15 | - | ns |
| | | | 15 V | | | 20 | 10 | - | ns |
| | | $\overline{nCP1}$ → nCP0; see Figure 5 | 5 V | | | 50 | 25 | - | ns |
| | | | 10 V | | | 30 | 15 | - | ns |
| | | | 15 V | | | 20 | 10 | - | ns |
| $t_{rec}$ | recovery time | see Figure 5 | 5 V | | | 50 | 25 | - | ns |
| | | | 10 V | | | 30 | 15 | - | ns |
| | | | 15 V | | | 20 | 10 | - | ns |
| $f_{max}$ | maximum frequency | nCP0, $\overline{nCP1}$; see Figure 5 | 5 V | | | 8 | 16 | - | MHz |
| | | | 10 V | | | 15 | 30 | - | MHz |
| | | | 15 V | | | 20 | 40 | - | MHz |

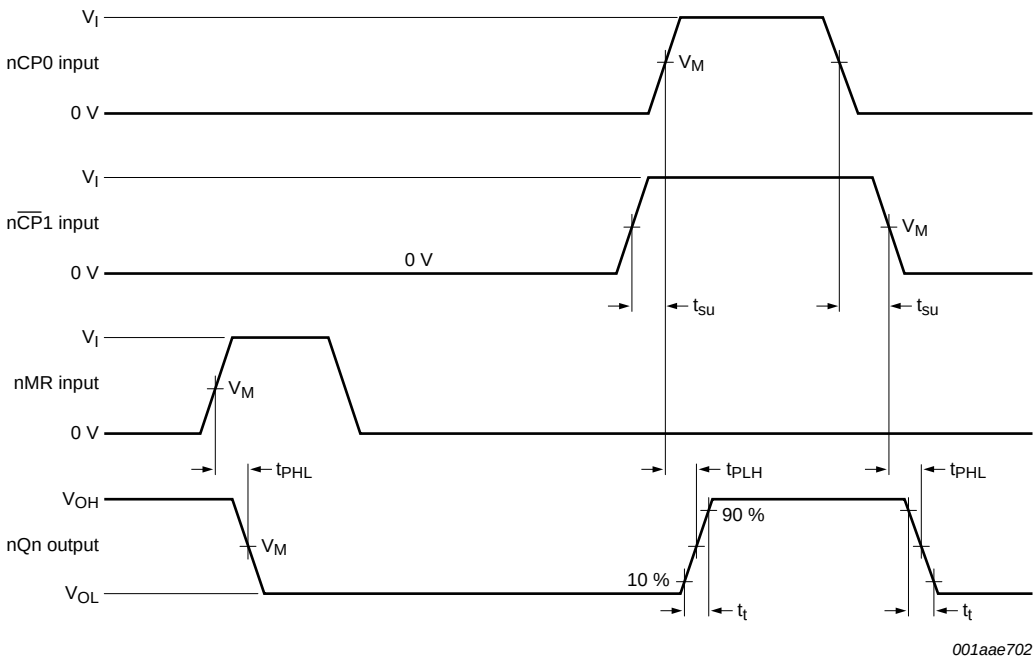
[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ($C_L$ in pF).

**Table 8. Dynamic power dissipation $P_D$**

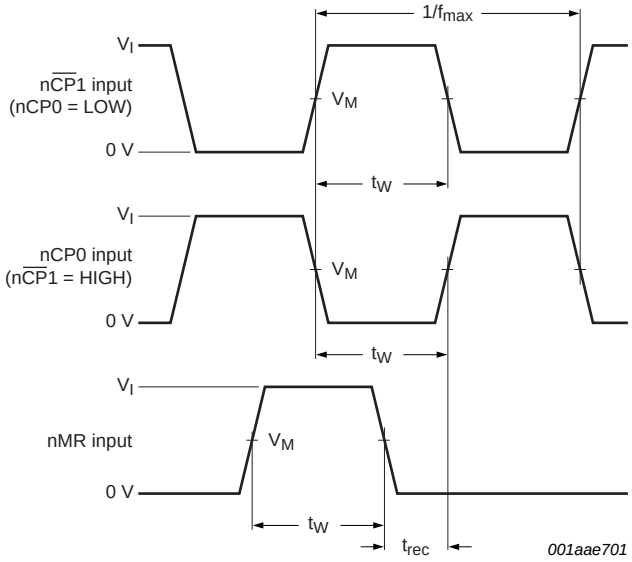
*$P_D$ can be calculated from the formulas shown. $V_{SS}$ = 0 V; $t_r = t_f \leq 20$ ns; $T_{amb}$ = 25 °C.*

| Symbol | Parameter | $V_{DD}$ | Typical formula for $P_D$ (µW) | Where: |
|---|---|---|---|---|
| $P_D$ | dynamic power dissipation | 5 V | $P_D = 850 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | $f_i$ = input frequency in MHz, $f_o$ = output frequency in MHz, $C_L$ = output load capacitance in pF, $V_{DD}$ = supply voltage in V, $\Sigma(f_o \times C_L)$ = sum of the outputs. |
| | | 10 V | $P_D = 3800 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |
| | | 15 V | $P_D = 10200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$ | |

## 11. Waveforms




a. nCP0 and nCP1 set-up times, propagation delays and output transition times

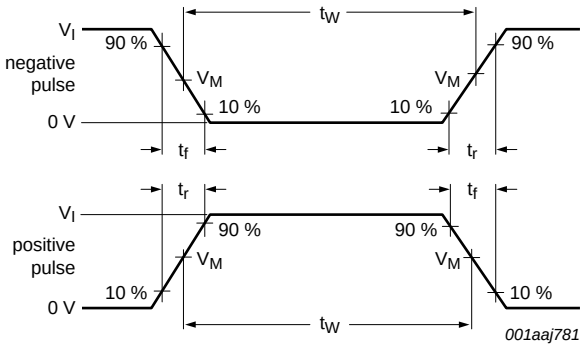



b. nMR recovery time, minimum nCP0, nCP1, and nMR pulse widths and maximum frequency

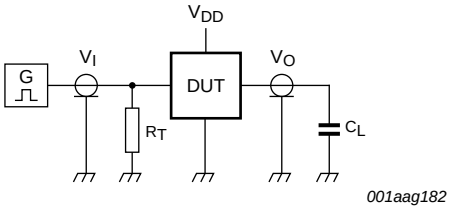
Measurement points are given in Table 9.

The logic levels $V_{OH}$ and $V_{OL}$ are typical output voltage levels that occur with the output load.

**Fig 5. Waveforms showing measurements for switching times**




a. Input waveforms




b. Test circuit

Test data is given in Table 9.

Definitions for test circuit:

DUT = Device Under Test;

$C_L$ = Load capacitance including jig and probe capacitance;

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

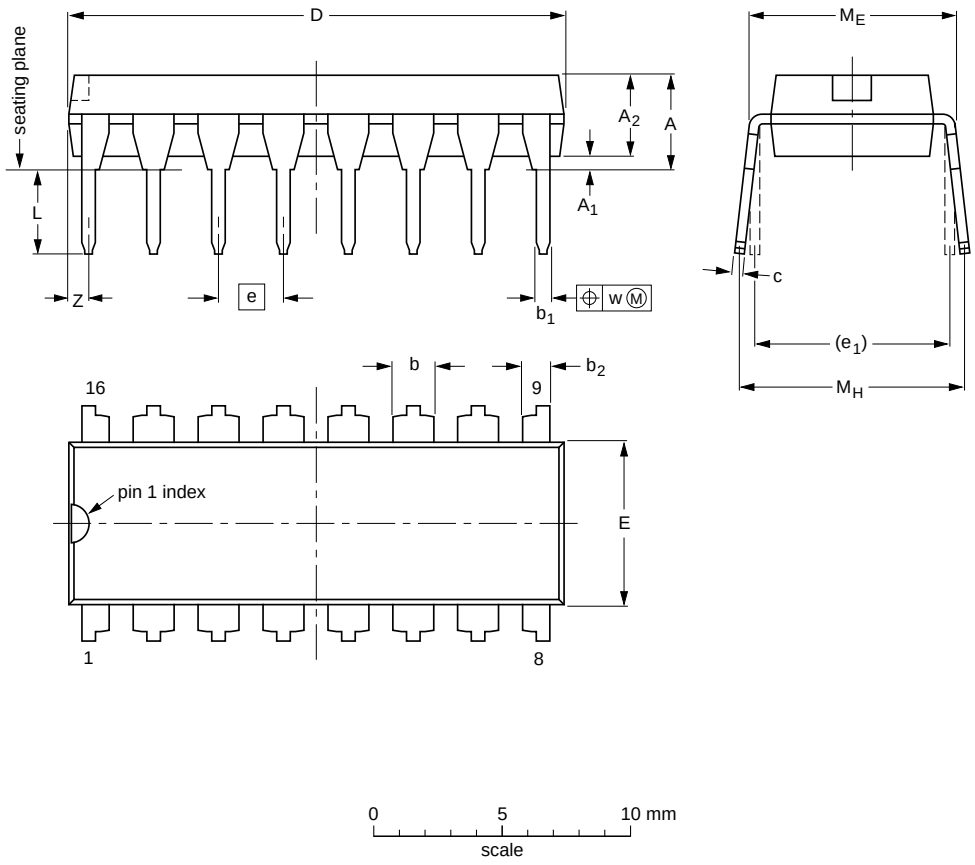
**Fig 6. Test circuit for measuring switching times**

**Table 9. Measurement points and test data**

| Supply voltage | Input | | | Load |
|---|---|---|---|---|
| | $V_I$ | $V_M$ | $t_r$, $t_f$ | $C_L$ |
| 5 V to 15 V | $V_{DD}$ | $0.5V_I$ | ≤ 20 ns | 50 pF |

## 12. Package outline

**DIP16: plastic dual in-line package; 16 leads (300 mil)** **SOT38-4**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ min. | $A_2$ max. | b | $b_1$ | $b_2$ | c | D (1) | E (1) | e | $e_1$ | L | $M_E$ | $M_H$ | w | Z (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 4.2 | 0.51 | 3.2 | 1.73<br>1.30 | 0.53<br>0.38 | 1.25<br>0.85 | 0.36<br>0.23 | 19.50<br>18.55 | 6.48<br>6.20 | 2.54 | 7.62 | 3.60<br>3.05 | 8.25<br>7.80 | 10.0<br>8.3 | 0.254 | 0.76 |
| inches | 0.17 | 0.02 | 0.13 | 0.068<br>0.051 | 0.021<br>0.015 | 0.049<br>0.033 | 0.014<br>0.009 | 0.77<br>0.73 | 0.26<br>0.24 | 0.1 | 0.3 | 0.14<br>0.12 | 0.32<br>0.31 | 0.39<br>0.33 | 0.01 | 0.03 |

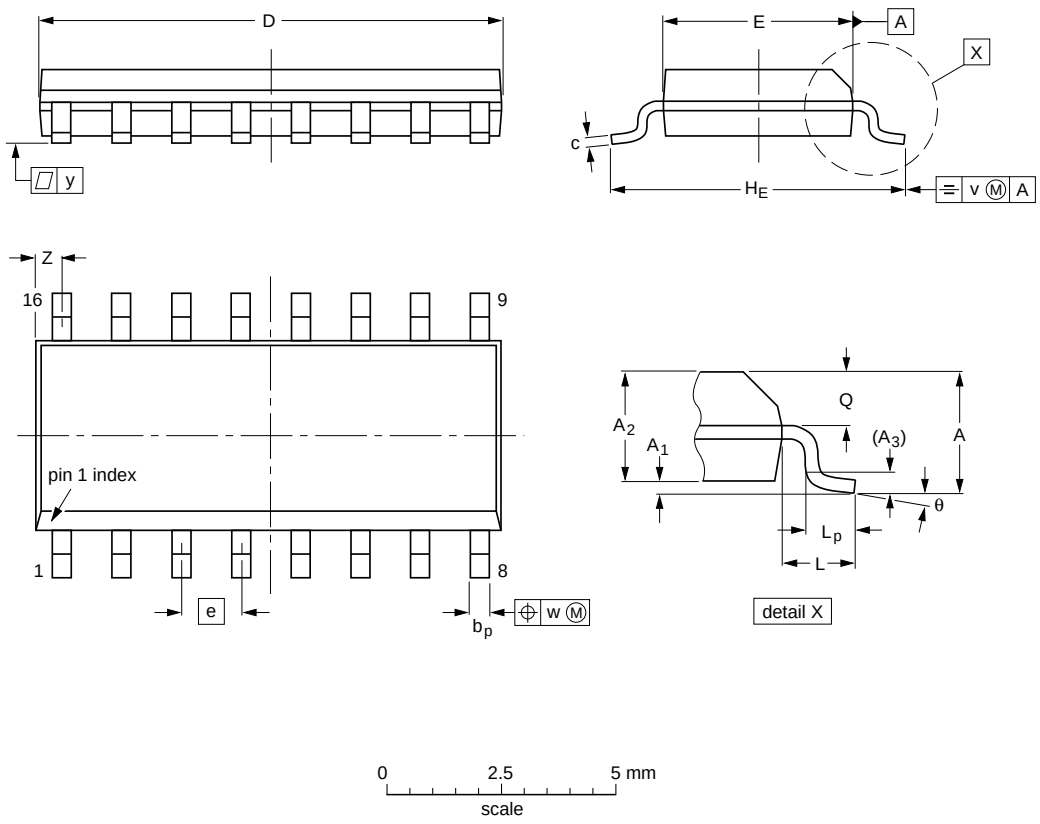
**Note**

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT38-4 | | | | | | ~~95-01-14~~<br>03-02-13 |

**Fig 7. Package outline SOT38-4 (DIP16)**

**SO16: plastic small outline package; 16 leads; body width 3.9 mm** **SOT109-1**




**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(1)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | $Z^{(1)}$ | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.75 | 0.25<br>0.10 | 1.45<br>1.25 | 0.25 | 0.49<br>0.36 | 0.25<br>0.19 | 10.0<br>9.8 | 4.0<br>3.8 | 1.27 | 6.2<br>5.8 | 1.05 | 1.0<br>0.4 | 0.7<br>0.6 | 0.25 | 0.25 | 0.1 | 0.7<br>0.3 | $8^o$<br>$0^o$ |
| inches | 0.069 | 0.010<br>0.004 | 0.057<br>0.049 | 0.01 | 0.019<br>0.014 | 0.0100<br>0.0075 | 0.39<br>0.38 | 0.16<br>0.15 | 0.05 | 0.244<br>0.228 | 0.041 | 0.039<br>0.016 | 0.028<br>0.020 | 0.01 | 0.01 | 0.004 | 0.028<br>0.012 | |

**Note**

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT109-1 | 076E07 | MS-012 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT109-1 (SO16)**

## 13. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| HEF4520B v.6 | 20111118 | Product data sheet | - | HEF4520B v.5 |
| Modifications: | • Section Applications removed<br>• Table 6: $I_{OH}$ minimum values changed to maximum | | | |
| HEF4520B v.5 | 20091210 | Product data sheet | - | HEF4520B v.4 |
| HEF4520B v.4 | 20090828 | Product data sheet | - | HEF4520B_CNV v.3 |
| HEF4520B_CNV v.3 | 19950101 | Product specification | - | HEF4520B_CNV v.2 |
| HEF4520B_CNV v.2 | 19950101 | Product specification | - | - |

# 14. Legal information

## 14.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

## 14.2 Definitions

**Draft —** The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

**Short data sheet —** A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

**Product specification —** The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

## 14.3 Disclaimers

**Limited warranty and liability —** Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

**Right to make changes —** NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

**Suitability for use —** NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

**Applications —** Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

**Limiting values —** Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

**Terms and conditions of commercial sale —** NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

**No offer to sell or license —** Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

**Export control —** This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

**Non-automotive qualified products —** Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

### 14.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

## 15. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

## 16. Contents





For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

**Date of release: 18 November 2011**
**Document identifier: HEF4520B**

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** Counter ICs ***category:***

***Click to view products by*** NXP ***manufacturer:***

Other Similar products are found below :

HEF4516BT 069748E 569054R 634844F 74HC40102N 74HCT4024N NLV14040BDR2G TC74HC4040AF(EL,F) TC74VHC4040F(E,K,F 74VHC163FT XD4059 CD4015BF3A 74HC193PW,118 74VHC163FT(BJ) SN54HC4024J 74HC4017D.652 74HC4020D.652 74HC393D.652 74HC4040D.652 74HC4040D.653 74HC4060D.653 74HCT393D.652 74HCT4040D.653 74HC191D.652 74HC4060D.652 74HCT4040D.652 HEF4040BT.652 HEF4060BT.653 HEF4521BT.652 HEF4518BT.652 HEF4520BT.652 HEF4017BT.652 74VHC4020FT(BJ) 74HCT4040PW,118 74HCT193PW,118 74HC393BQ-Q100X SN74AS161NSR 74HC390DB,112 74HC4060D-Q100,118 74HC160D,652 74HC390DB,118 TC74HC7292AP(F) SN74ALS169BDR HEF4060BT-Q100J 74HC4017BQ-Q100X 74HC163PW.112 74HC191PW.112 74HC390PW.112 74HC393DB.118 74HC4024D.652