



IMPORTANT NOTICE

10 December 2015

1. Global joint venture starts operations as WeEn Semiconductors

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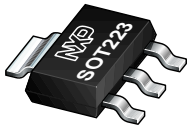
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WeEn Semiconductors





MCR08BT1

SCR

23 July 2014

Product data sheet

1. General description

Planar passivated SCR with sensitive gate in a SOT223 surface mountable plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

2. Features and benefits

- Sensitive gate
- Planar passivated for voltage ruggedness and reliability
- Direct triggering from low power drivers and logic ICs
- Surface mountable package

3. Applications

- General purpose switching and phase control
- Ignition circuits, CDI for 2- and 3-wheelers
- Motor control - e.g. small kitchen appliances

4. Quick reference data

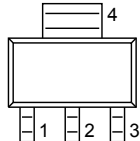

Table 1. Quick reference data

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------|--------------------------------------|---|-----|-----|-----|---------------|
| V_{DRM} | repetitive peak off-state voltage | | - | - | 200 | V |
| V_{RRM} | repetitive peak reverse voltage | | - | - | 200 | V |
| I_{TSM} | non-repetitive peak on-state current | half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5 | - | - | 8 | A |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 1 | - | - | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 2 ; Fig. 3 | - | - | 0.8 | A |
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 9 | - | 50 | 200 | μA |



5. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|------------------------|---|---|
| 1 | K | cathode |  <p>SC-73 (SOT223)</p> |  <p>sym037</p> |
| 2 | A | anode | | |
| 3 | G | gate | | |
| 4 | A | mb; connected to anode | | |

6. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| MCR08BT1 | SC-73 | plastic surface-mounted package with increased heatsink; 4 leads | SOT223 |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|--------------|--------------------------------------|--|-----|------|------------------|
| V_{DRM} | repetitive peak off-state voltage | | - | 200 | V |
| V_{RRM} | repetitive peak reverse voltage | | - | 200 | V |
| $I_{T(AV)}$ | average on-state current | half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 1 | - | 0.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | half sine wave; $T_{sp} \leq 112\text{ °C}$; Fig. 2 ; Fig. 3 | - | 0.8 | A |
| I_{TSM} | non-repetitive peak on-state current | half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5 | - | 8 | A |
| | | half sine wave; $T_{j(\text{init})} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$ | - | 9 | A |
| I^2t | I^2t for fusing | $t_p = 10\text{ ms}$; SIN | - | 0.32 | A ² s |
| dl_T/dt | rate of rise of on-state current | $I_T = 2\text{ A}$; $I_G = 10\text{ mA}$; $dl_G/dt = 100\text{ mA}/\mu\text{s}$ | - | 50 | A/ μs |
| I_{GM} | peak gate current | | - | 1 | A |
| V_{RGM} | peak reverse gate voltage | | - | 5 | V |
| P_{GM} | peak gate power | | - | 2 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | - | 0.1 | W |
| T_{stg} | storage temperature | | -40 | 150 | °C |
| T_j | junction temperature | | - | 125 | °C |

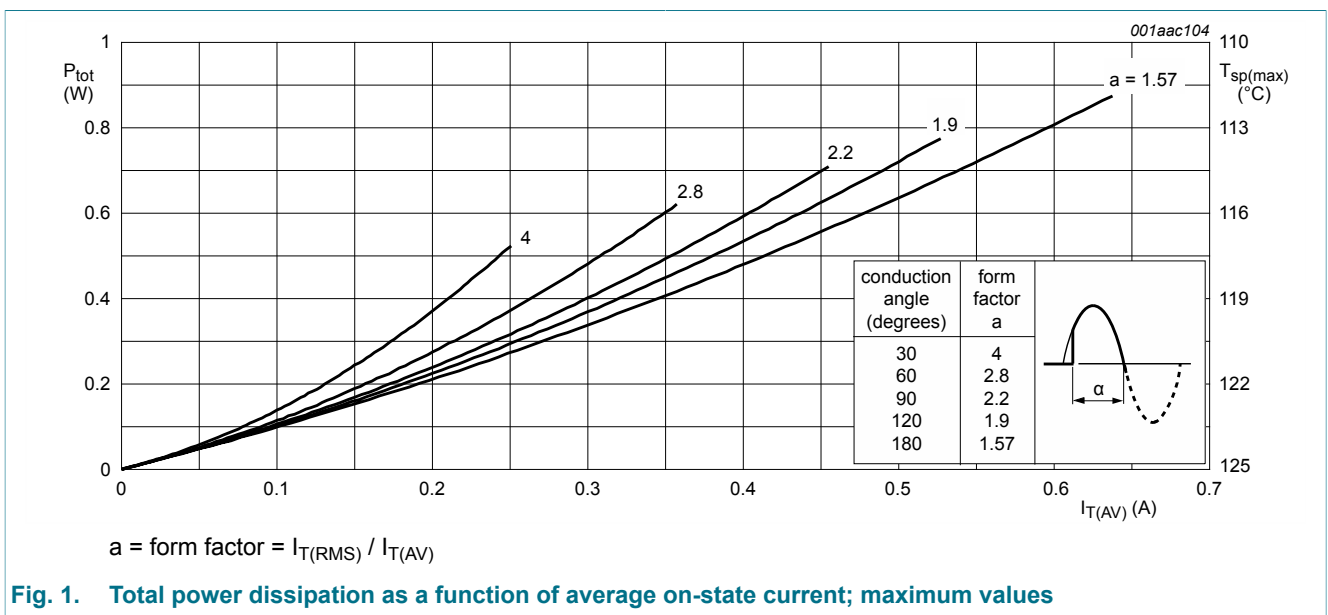
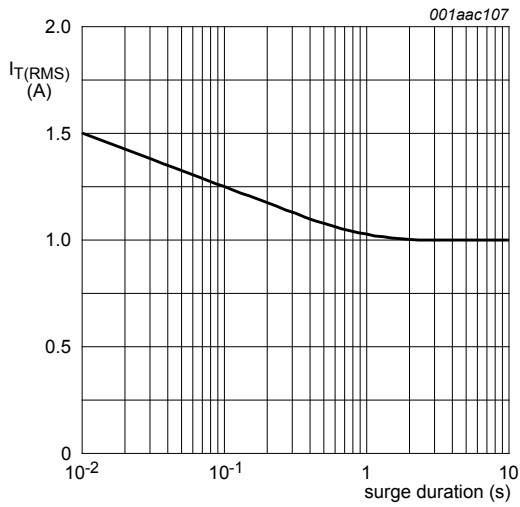


Fig. 1. Total power dissipation as a function of average on-state current; maximum values



$f = 50 \text{ Hz}; T_{sp} = 112 \text{ }^\circ\text{C}$

Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents; maximum values

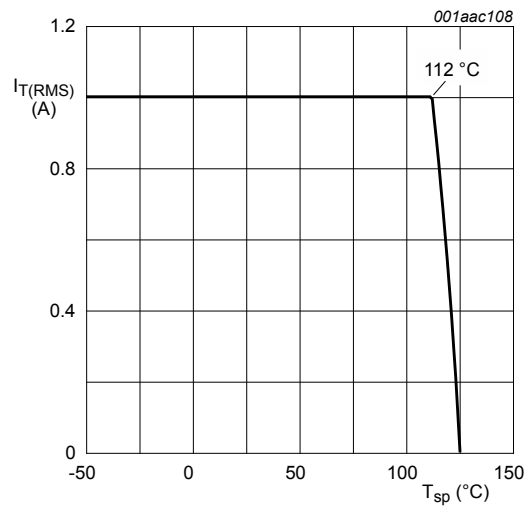
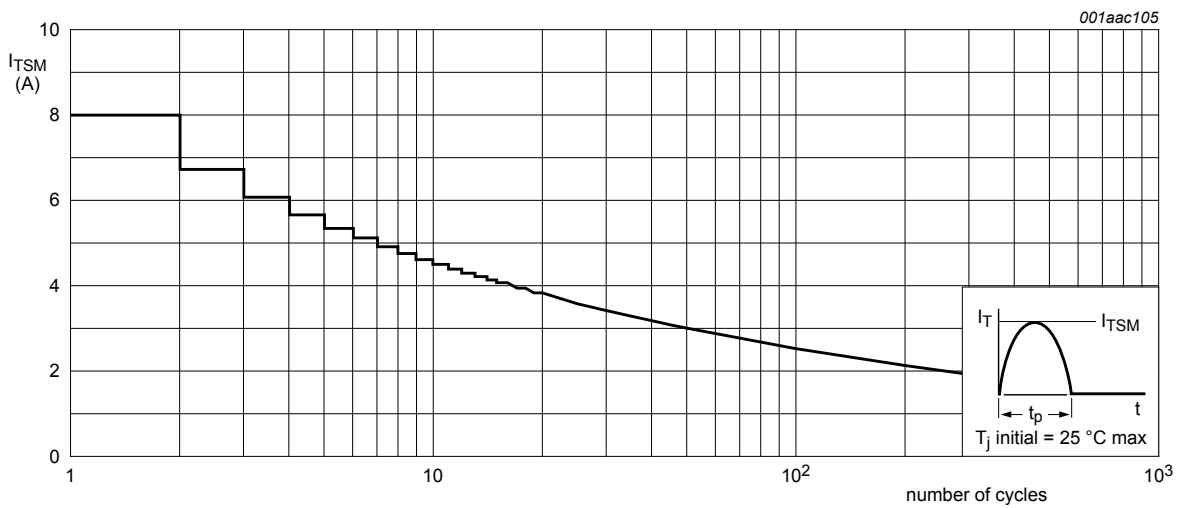
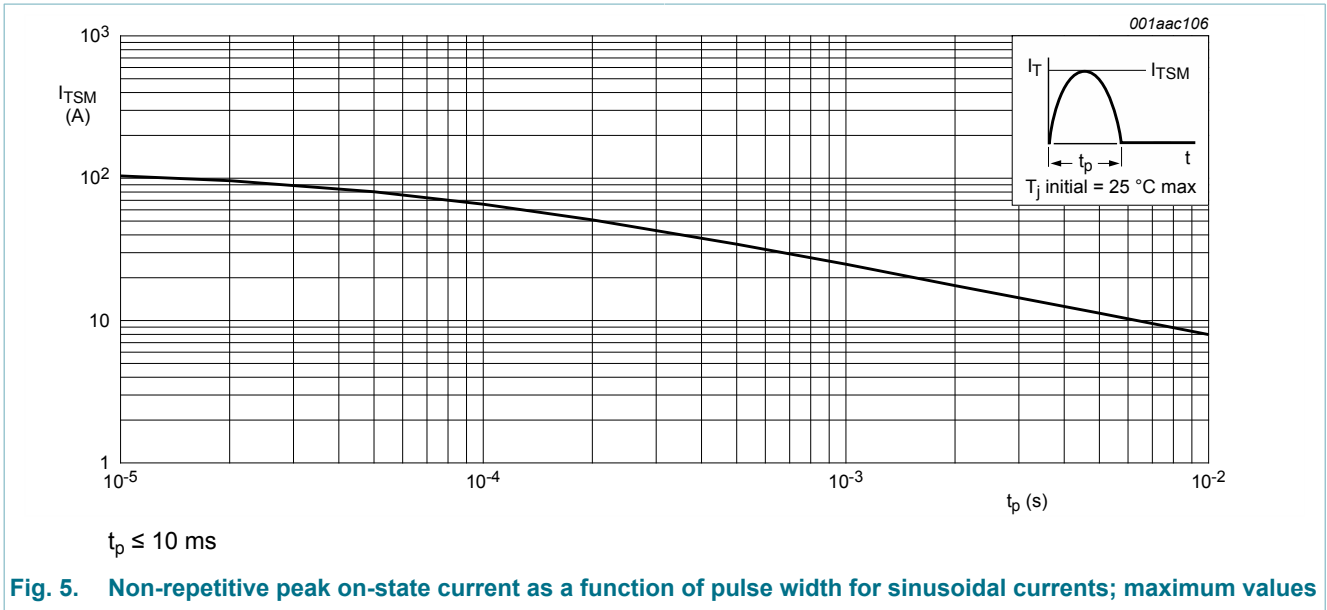


Fig. 3. RMS on-state current as a function of solder point temperature; maximum values



$f = 50 \text{ Hz}$

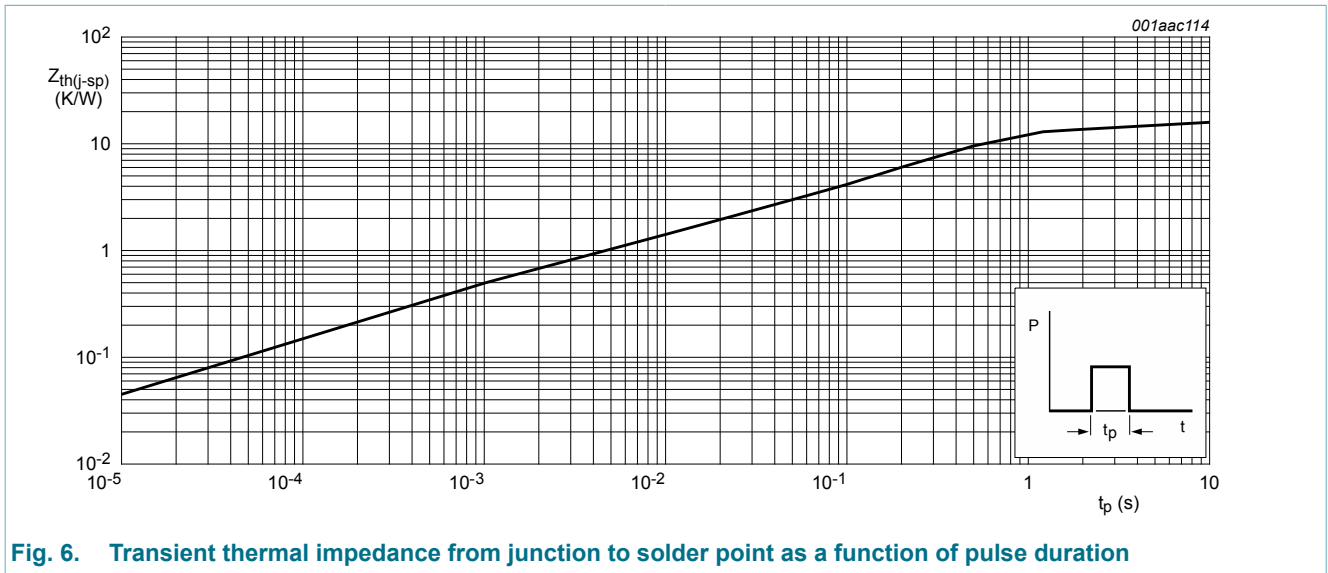
Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

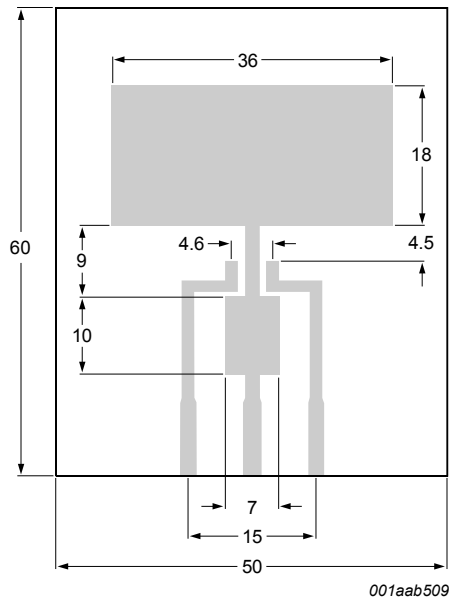


8. Thermal characteristics

Table 5. Thermal characteristics

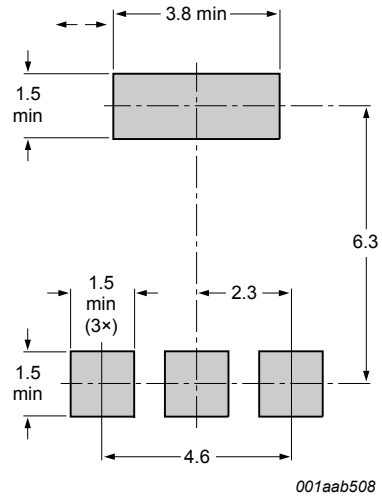
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|--|---|-----|-----|-----|------|
| $R_{th(j-sp)}$ | thermal resistance from junction to solder point | Fig. 6 | - | - | 15 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | printed circuit board mounted; minimum pad area; in free air ; Fig. 7 | - | 70 | - | K/W |
| | | printed circuit board mounted; minimum footprint; in free air; Fig. 8 | - | 156 | - | K/W |





All dimensions are in mm
 Printed circuit board:
 FR4 epoxy glass (1.6 mm thick), copper laminate
 (35 µm thick)

Fig. 7. Printed circuit board pad area: SOT223



All dimensions are in mm

Fig. 8. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|------|-----|------------------------|
| Static characteristics | | | | | | |
| I_{GT} | gate trigger current | $V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 9 | - | 50 | 200 | μA |
| I_L | latching current | $V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 10 | - | 2 | 6 | mA |
| I_H | holding current | $V_D = 12\text{ V}$; $R_{GK} = 1\text{ k}\Omega$; $T_j = 25\text{ °C}$; Fig. 11 | - | 2 | 5 | mA |
| V_T | on-state voltage | $I_T = 1.2\text{ A}$; $T_j = 25\text{ °C}$; Fig. 12 | - | 1.25 | 1.7 | V |
| V_{GT} | gate trigger voltage | $V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 13 | - | 0.5 | 0.8 | V |
| | | $V_D = 200\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 125\text{ °C}$; Fig. 13 | 0.2 | 0.3 | - | V |
| I_D | off-state current | $V_D = 200\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$ | - | 0.05 | 1 | mA |
| I_R | reverse current | $V_R = 200\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$ | - | 0.05 | 1 | mA |
| Dynamic characteristics | | | | | | |
| dV_D/dt | rate of rise of off-state voltage | $V_{DM} = 134\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 14 | 500 | 800 | - | $\text{V}/\mu\text{s}$ |
| | | $V_{DM} = 134\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 14 | - | 25 | - | $\text{V}/\mu\text{s}$ |
| t_{gt} | gate-controlled turn-on time | $I_{TM} = 2\text{ A}$; $V_D = 200\text{ V}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$; $T_j = 25\text{ °C}$ | - | 2 | - | μs |
| t_q | commutated turn-off time | $V_{DM} = 134\text{ V}$; $T_j = 125\text{ °C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}) | - | 100 | - | μs |

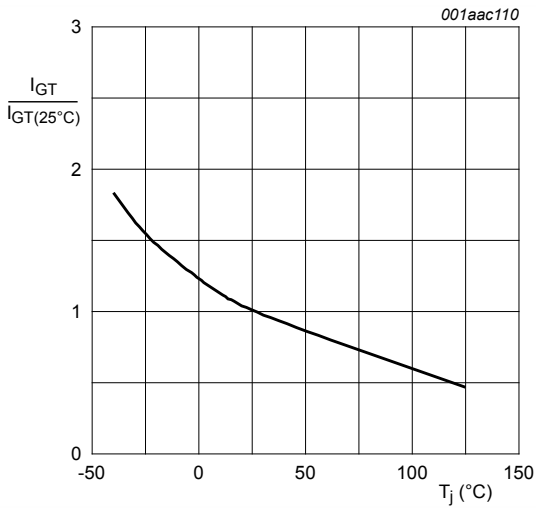
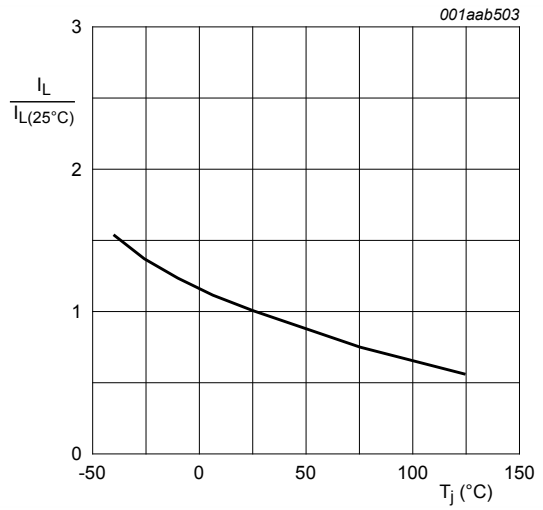
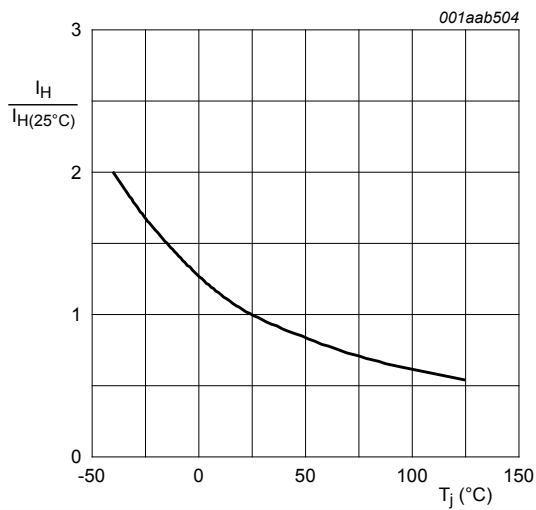


Fig. 9. Normalized gate trigger current as a function of junction temperature



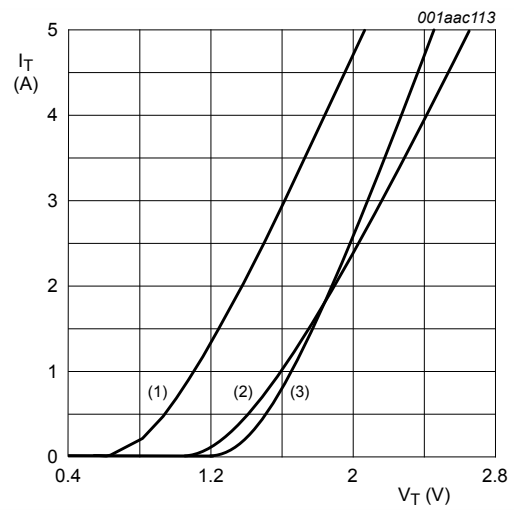
$R_{GK} = 1 \text{ k}\Omega$

Fig. 10. Normalized latching current as a function of junction temperature



$R_{GK} = 1 \text{ k}\Omega$

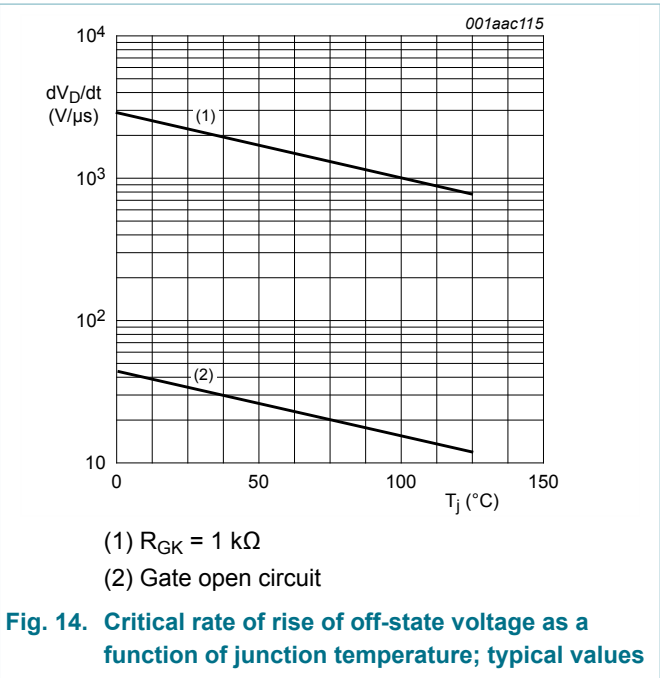
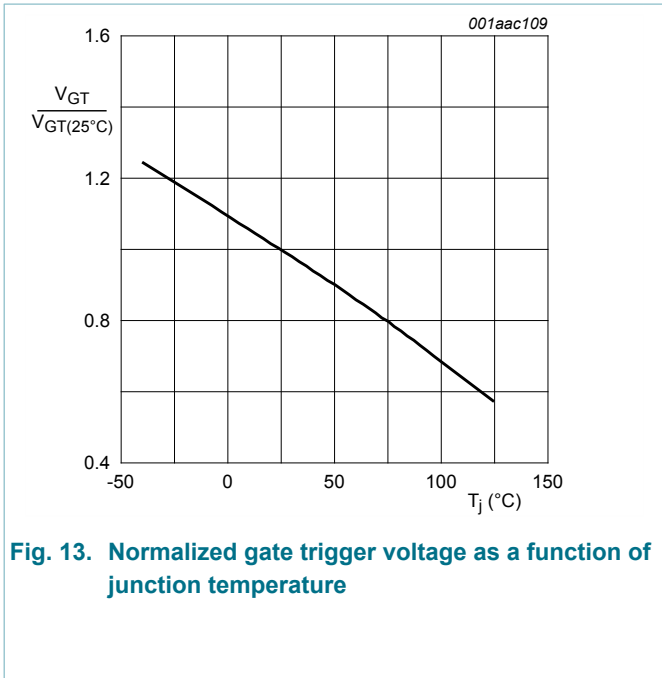
Fig. 11. Normalized holding current as a function of junction temperature



$V_o = 1.0 \text{ V}; R_s = 0.27 \Omega$

- (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
- (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
- (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

Fig. 12. On-state current as a function of on-state voltage



10. Package outline

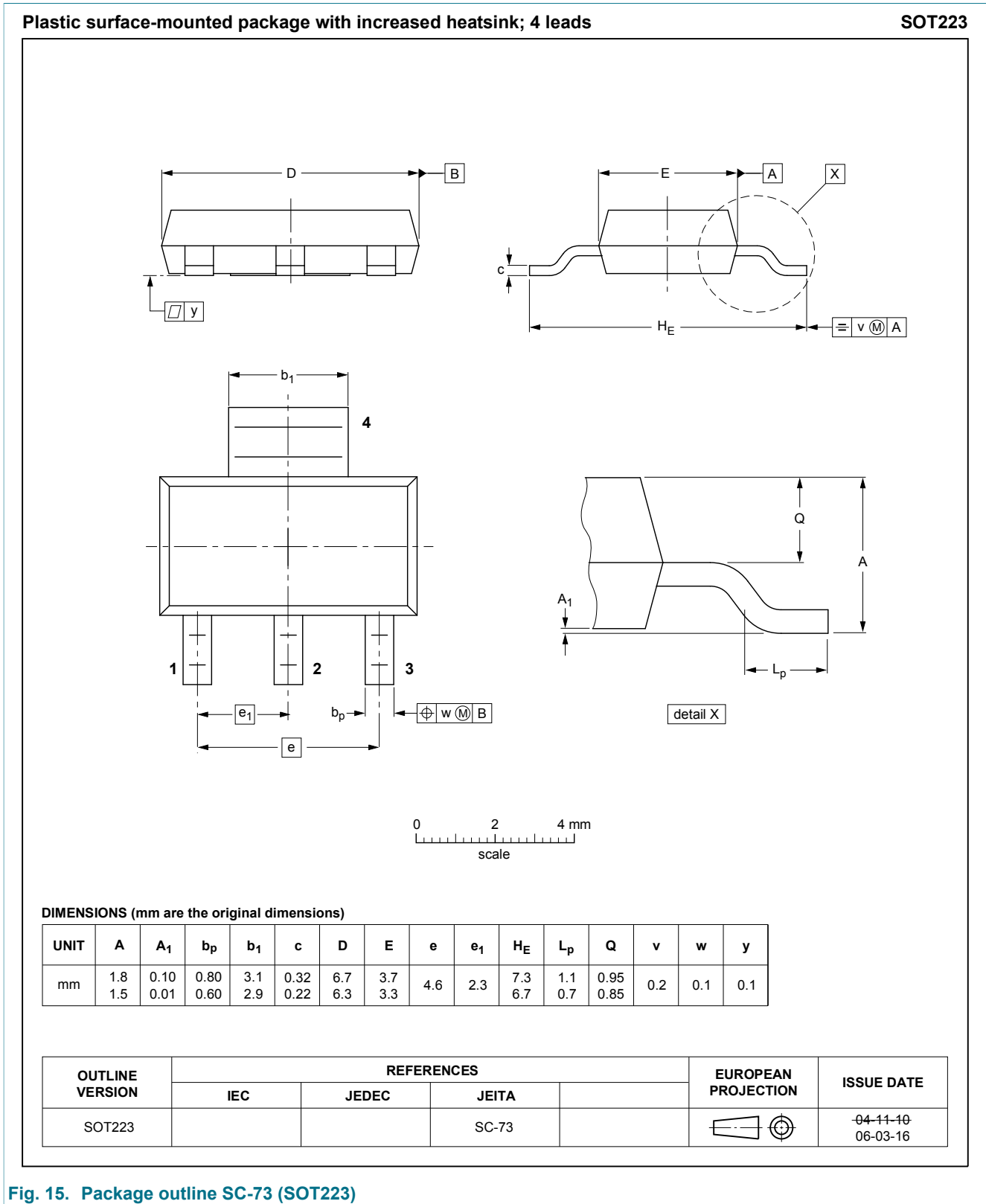


Fig. 15. Package outline SC-73 (SOT223)

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|--------------------------------|--------------------|---|
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12. Contents

| | | |
|------|-------------------------------|----|
| 1 | General description | 1 |
| 2 | Features and benefits | 1 |
| 3 | Applications | 1 |
| 4 | Quick reference data | 1 |
| 5 | Pinning information | 2 |
| 6 | Ordering information | 2 |
| 7 | Limiting values | 3 |
| 8 | Thermal characteristics | 6 |
| 9 | Characteristics | 8 |
| 10 | Package outline | 11 |
| 11 | Legal information | 12 |
| 11.1 | Data sheet status | 12 |
| 11.2 | Definitions | 12 |
| 11.3 | Disclaimers | 12 |
| 11.4 | Trademarks | 13 |

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