RL78/G1C

RENESAS MCU

R01DS0348EJ0001
Rev.0.01
2012.09.20

Integrated USB Controller, True Low Power Platform (as low as 112.5 μA/MHz, and 0.61 μA for RTC + LVD), 2.4 V to 5.5 V Operation, 32 Kbyte Flash, 31 DMIPS at 24 MHz, for All USB Based Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 2.4 V to 5.5 V operation from a single supply
- Stop (RAM retained): 0.23 μA, (LVD enabled): 0.31 μA
- Halt (RTC + LVD): 0.57 μA
- Supports snooze
- Operating: 71 μA/MHz

16-bit RL78 CPU Core
- Delivers 31 DMIPS at maximum operating frequency of 24 MHz
- Instruction Execution: 86% of instructions can be executed in 1 to 2 clock cycles
- CISC Architecture (Harvard) with 3-stage pipeline
- Multiply Signed & Unsigned: 16 x 16 to 32-bit result in 1 clock cycle
- MAC: 16 x 16 to 32-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 1 clock cycle
- 1-wire on-chip debug function

Code Flash Memory
- Density: 32 KB
- Block size: 1 KB
- On-chip single voltage flash memory with protection from block erase/writing
- Self-programming with secure boot swap function and flash shield window function

Data Flash Memory
- Data Flash with background operation
- Data flash size: 2 KB
- Erase Cycles: 1 Million (typ.)
- Erase/programming voltage: 2.4 V to 5.5 V

RAM
- 5.5 KB size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 24 MHz with +/– 1% accuracy over voltage (2.4 V to 5.5 V) and temperature (–20°C to +85°C)
- Pre-configured settings: 48 MHz, 24 MHz (TYP.)

Reset and Supply Management
- Power-on reset (POR) monitor/generator
- Low voltage detection (LVD) with 9 setting options (Interrupt and/or reset function)

USB
- Complying with USB 2.0
- Corresponding to full-speed transfer (12Mbps) and low-speed transfer (1.5Mbps)
- Complying with Battery Charging Specification Revision 1.2
- Supports USB Host controller and USB function controller

Direct Memory Access (DMA) Controller
- Up to 2 fully programmable channels
- Transfer unit: 8- or 16-bit

Multiple Communication Interfaces
- Up to 2 x I^2C master
- Up to 1 x I^2C multi-master
- Up to 2 x CSI (7-, 8-bit)
- Up to 1 x UART (7-, 8-, 9-bit)

Extended-Function Timers
- Multi-function 16-bit timer TAU: Up to 4 channels (remote control output available)
- Real-time clock (RTC): 1 channel (full calendar and alarm function with watch correction function)
- 12-bit interval timer: 1 channel
- 15 kHz watchdog timer: 1 channel (window function)

Rich Analog
- ADC: Up to 9 channels, 8/10-bit resolution, 2.1 μs minimum conversion time
- Internal voltage reference (1.45 V)
- On-chip temperature sensor

Safety Features (IEC or UL 60730 compliance)
- Flash memory CRC calculation
- RAM parity error check
- RAM write protection
- SFR write protection
- Illegal memory access detection
- Clock stop/frequency detection
- ADC self-test
- I/O port read back function (echo)

General Purpose I/O
- 5 V tolerant, high-current (up to 20 mA per pin)
- Open-Drain, Internal Pull-up support

Operating Ambient Temperature
- Standard: –40°C to + 85°C
- Extended: –40°C to + 105°C <under planning>

Package Type and Pin Count
- 32-pin plastic WQFN (5 x 5)
- 32-pin plastic LQFP (7 x 7)
- 48-pin plastic LQFP (fine pitch) (7 x 7)
- 48-pin plastic WQFN (7 x 7)

○ ROM, RAM capacities

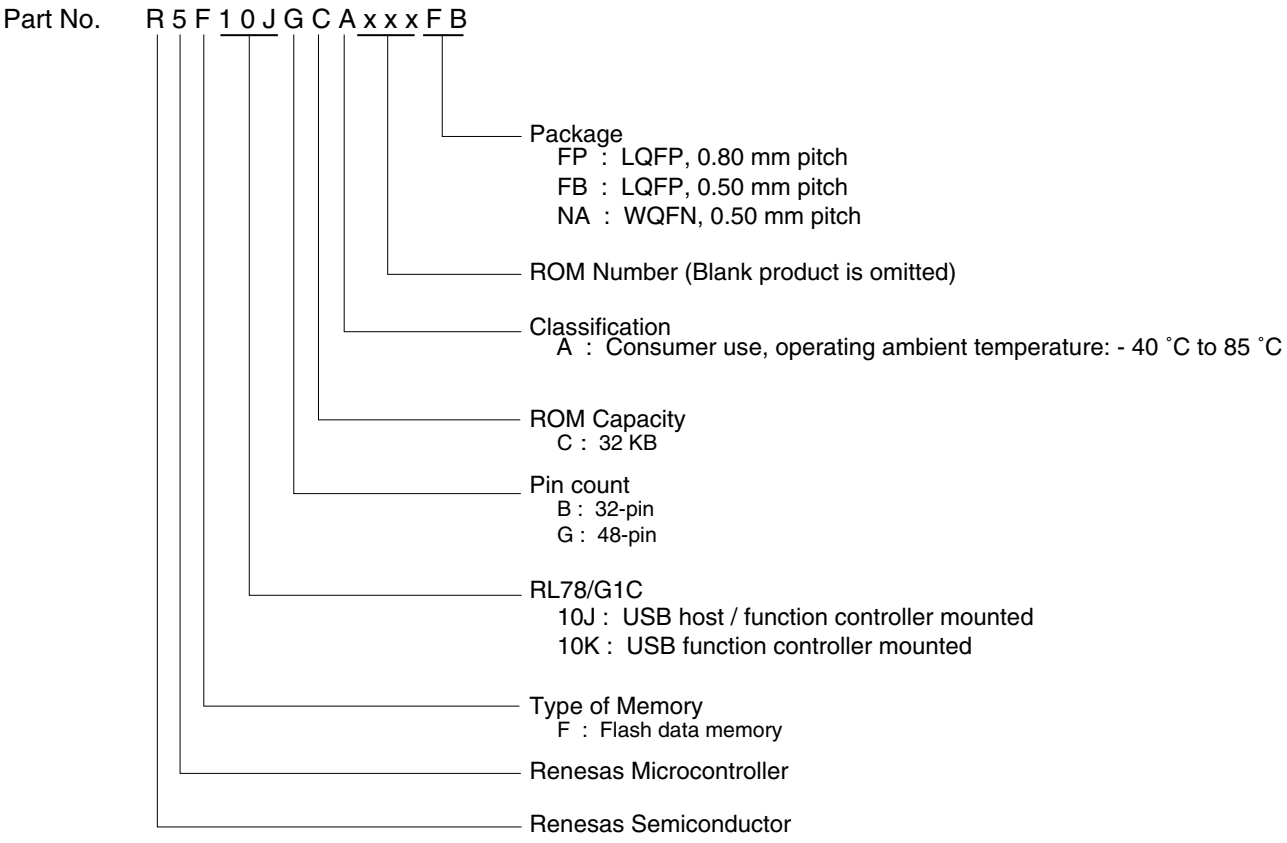
Flash ROM	Data flash	RAM	RL78/G1C	
			32-pin	48-pin
32 KB	2 KB	5.5 KB[Note]	R5F10JBC, R5F10KBC	R5F10JGC, R5F10KGC

Note This is about 4.5 KB when the self-programming function is used.

1.2 Ordering Information

Pin count	Package	USB Function	Part Number
32 pins	32-pin plastic WQFN (5 × 5)	Host/Function controller	R5F10JBCANA
		Function controller only	R5F10KBCANA
	32-pin plastic LQFP (7 × 7)	Host/Function controller	R5F10JBCAFP
		Function controller only	R5F10KBCAFP
48 pins	48-pin plastic LQFP (fine pitch) (7 × 7)	Host/Function controller	R5F10JGCAFB
		Function controller only	R5F10KGCAFB
	48-pin plastic WQFN (7 × 7)	Host/Function controller	R5F10JGCANA
		Function controller only	R5F10KGCANA

Figure 1-1. Part Number, Memory Size, and Package of RL78/G1C



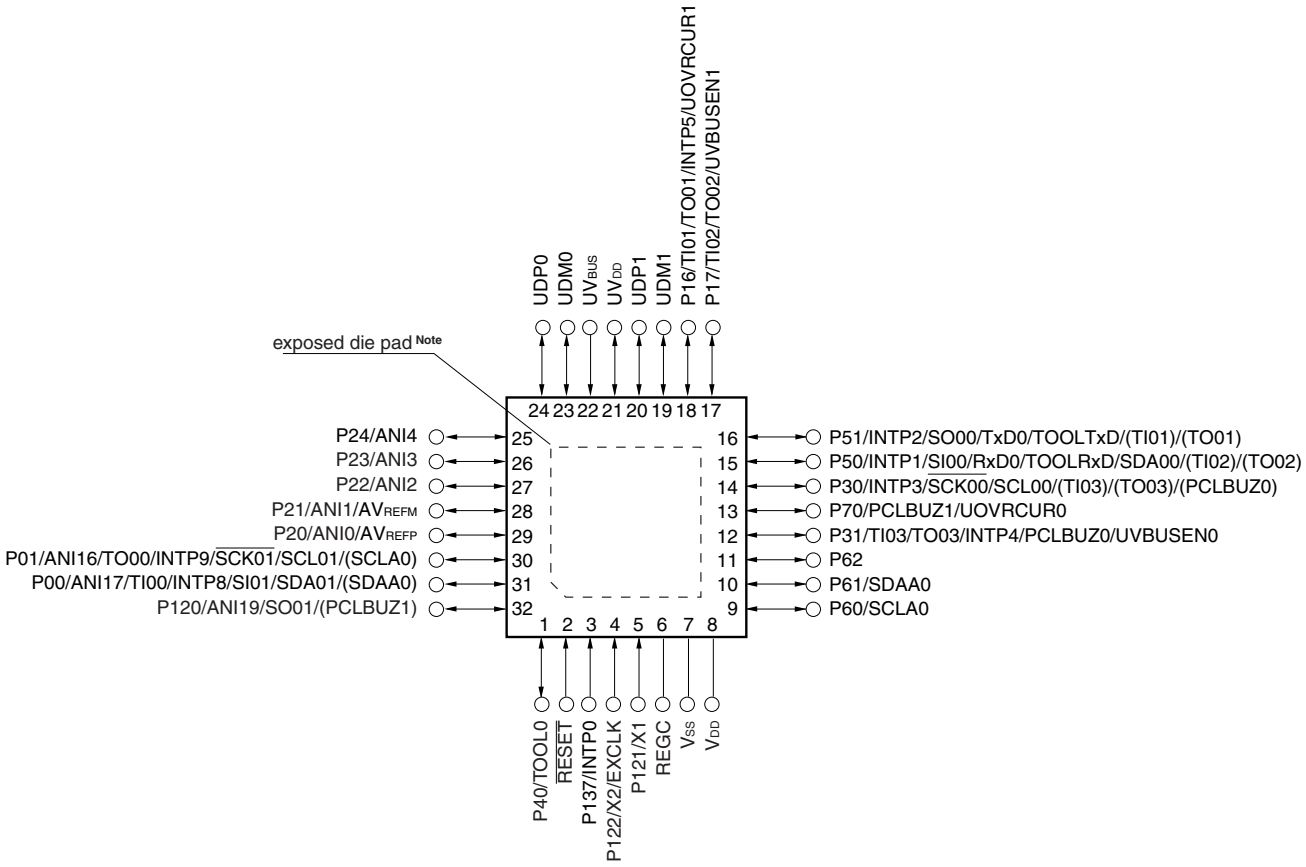
Remark For details about extended-temperature products for industrial applications (operating ambient temperature: –40°C to +105°C), contact a Renesas Electronics Corporation or an authorized Renesas Electronics Corporation distributor.

1.3 Pin Configuration (Top View)

1.3.1 32-pin products

- 32-pin plastic WQFN (5 × 5)
- 32-pin plastic LQFP (7 × 7)

(1) USB function: Host/Function controller (R5F10JBC)



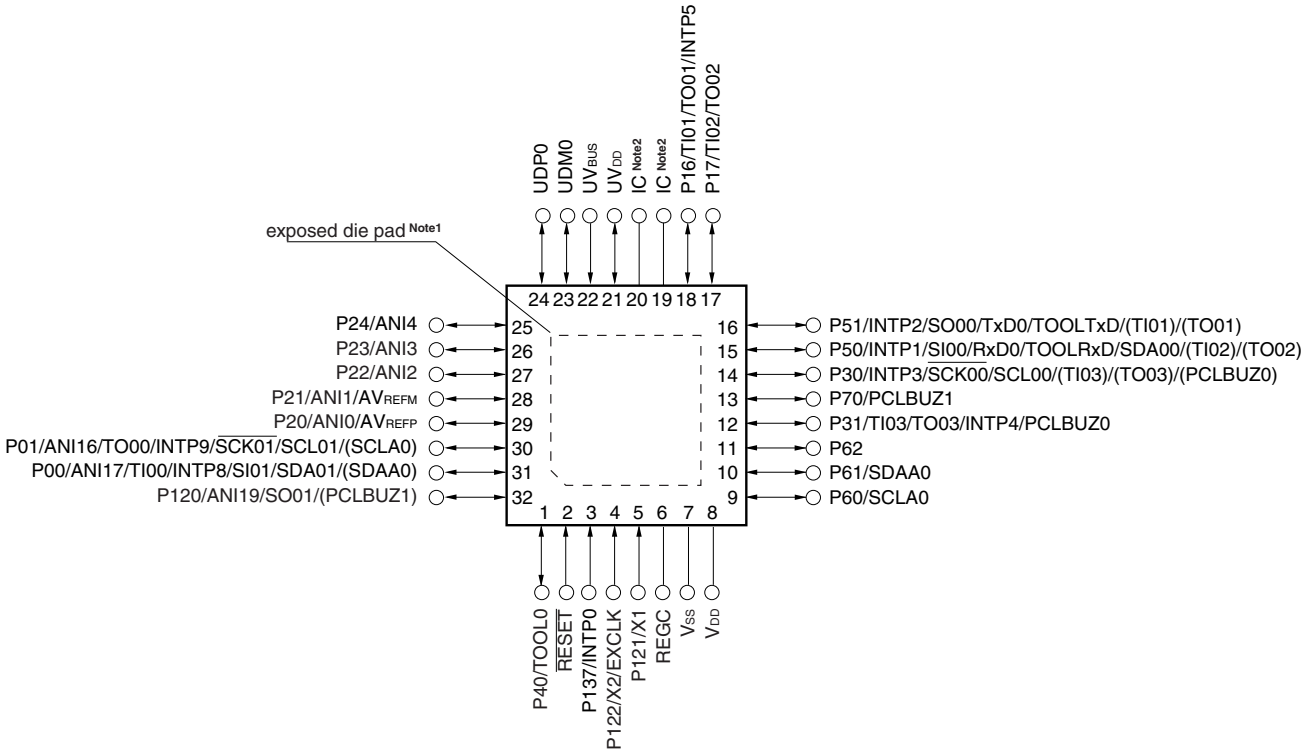
Note In 32-pin plastic WQFN (5 × 5) packages only, the die pad is exposed on the back of the packages.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) USB function: Function controller only (R5F10KBC)



Notes 1. In 32-pin plastic WQFN (5 × 5) packages only, the die pad is exposed on the back of the packages.

2. IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

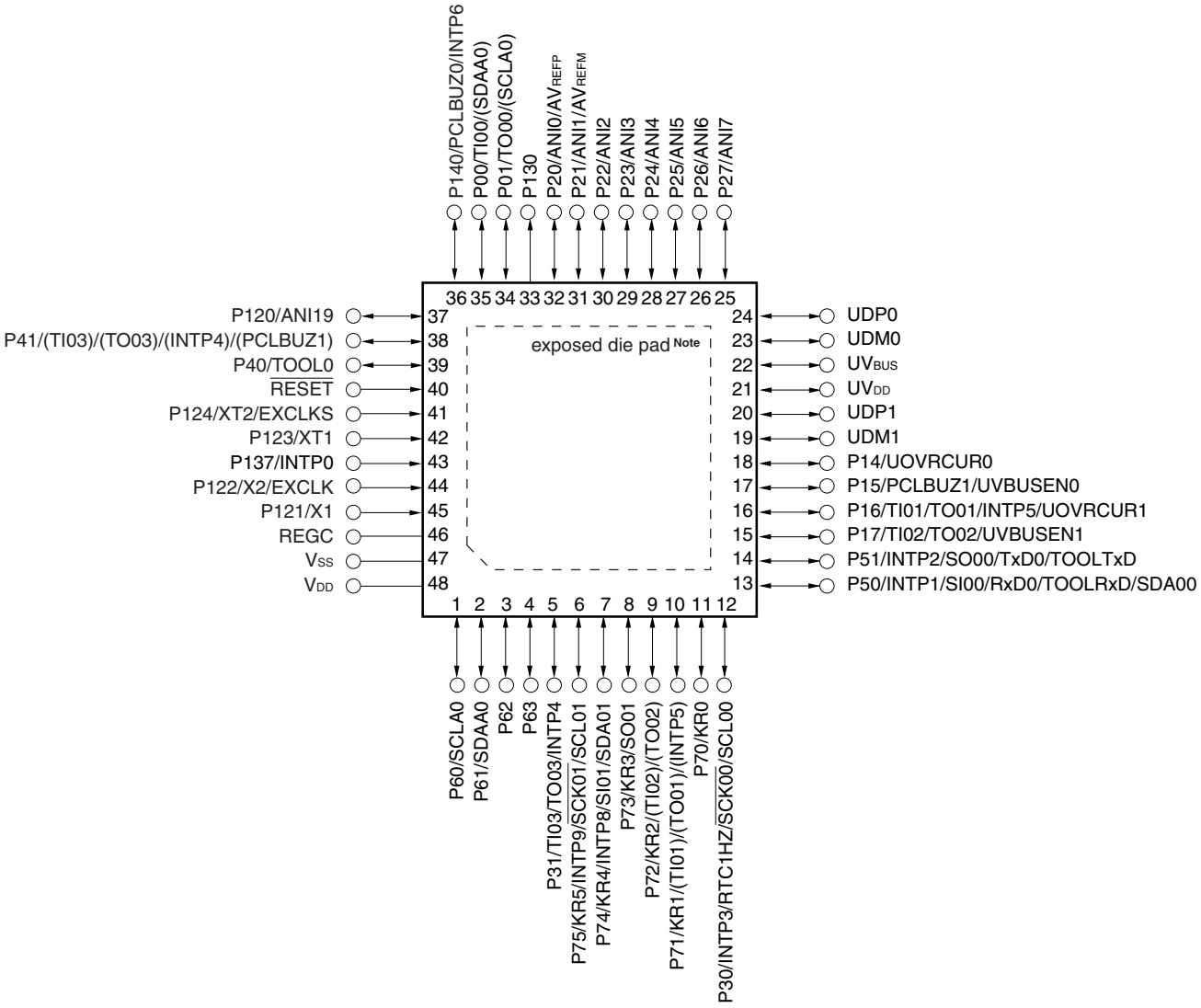
Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 48-pin products

- 48-pin plastic LQFP (fine pitch) (7 × 7)
- 48-pin plastic WQFN (7 × 7)

(1) USB function: Host/Function controller (R5F10JGC)



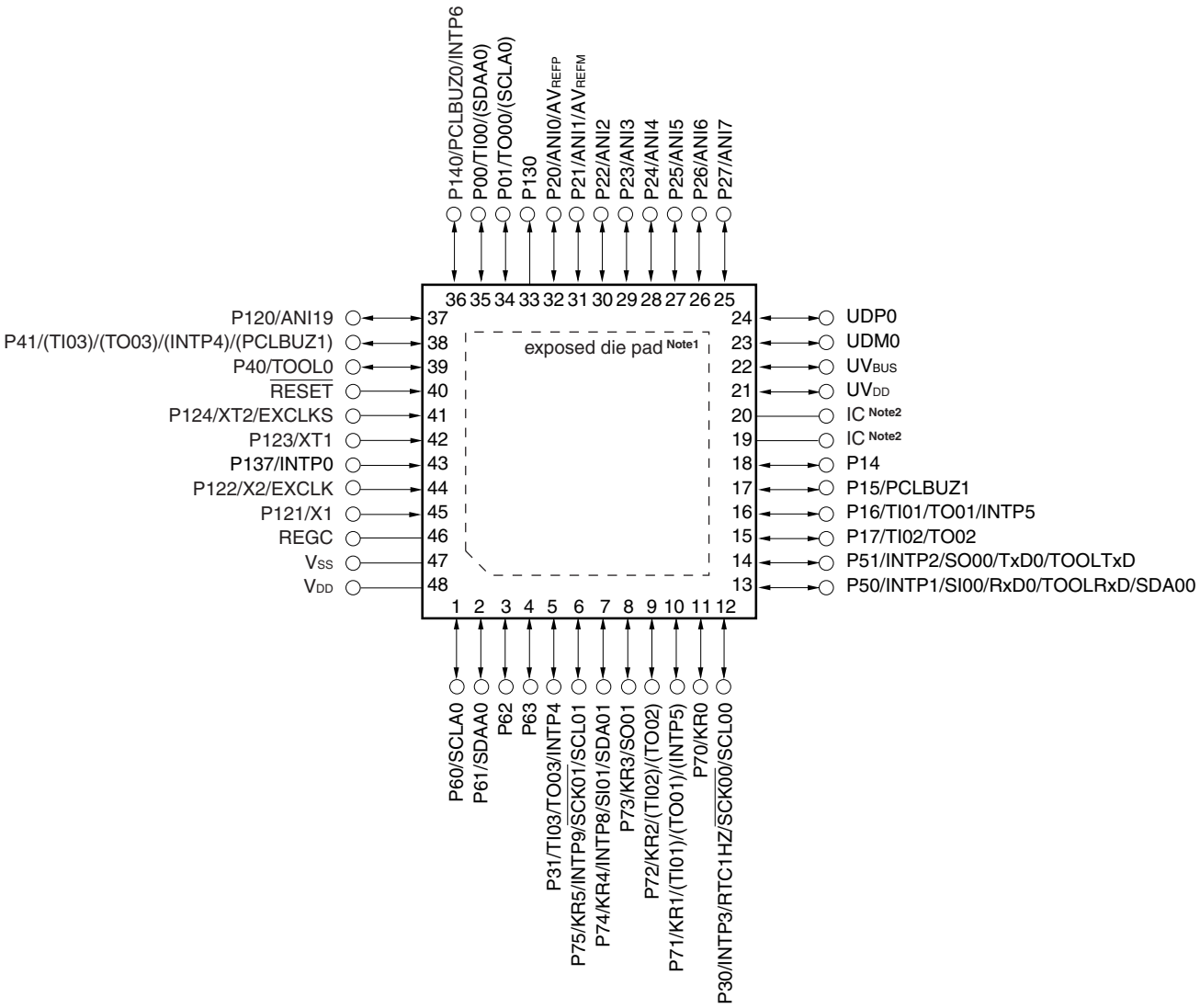
Note In 48-pin plastic WQFN (7 × 7) packages only, the die pad is exposed on the back of the packages.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

(2) USB function: Function controller only (R5F10KGC)



Notes 1. In 48-pin plastic WQFN (7 × 7) packages only, the die pad is exposed on the back of the packages.

2. IC: Internal Connection Pin Leave open.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remarks 1. For pin identification, see **1.4 Pin Identification**.

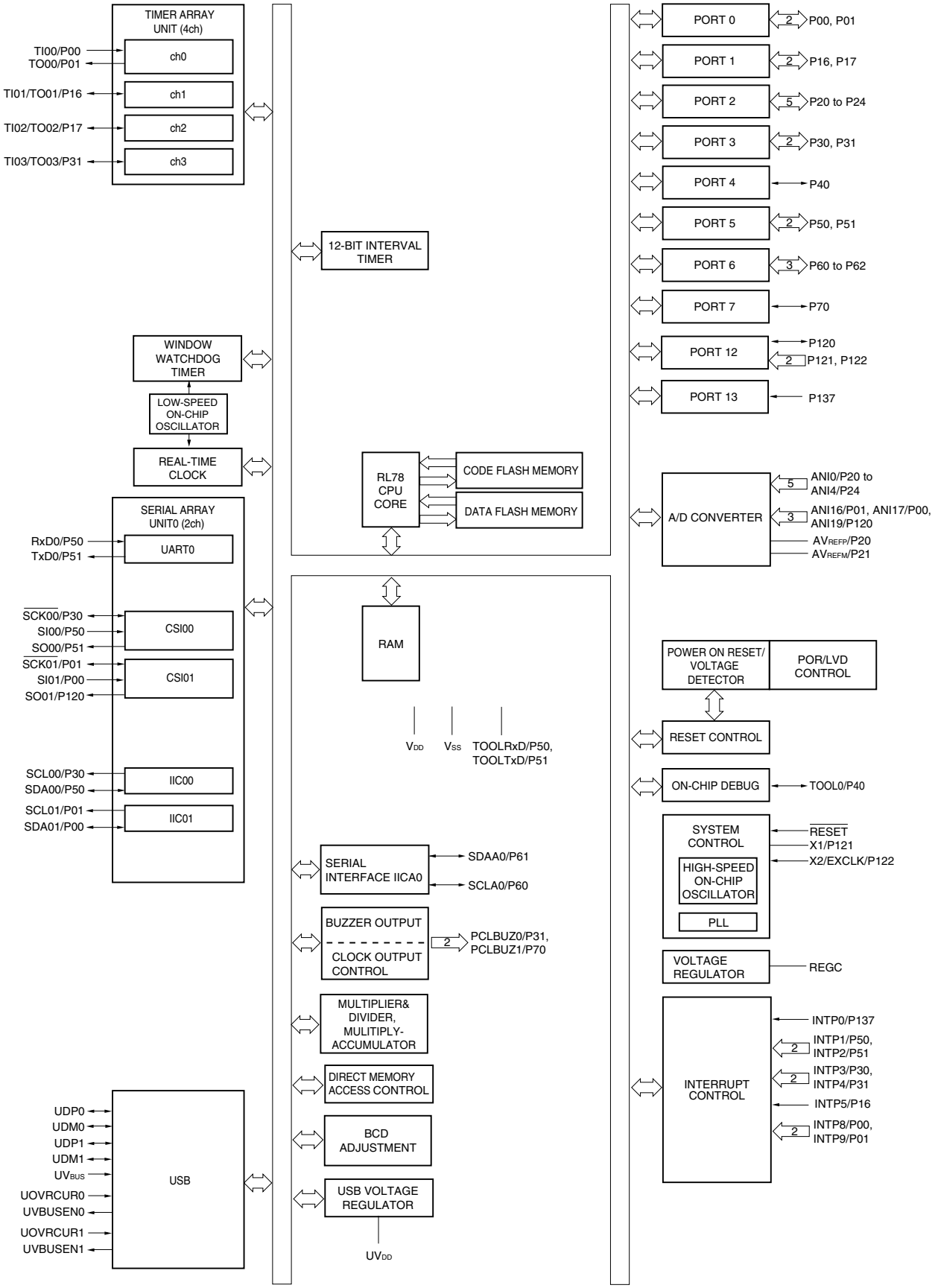
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

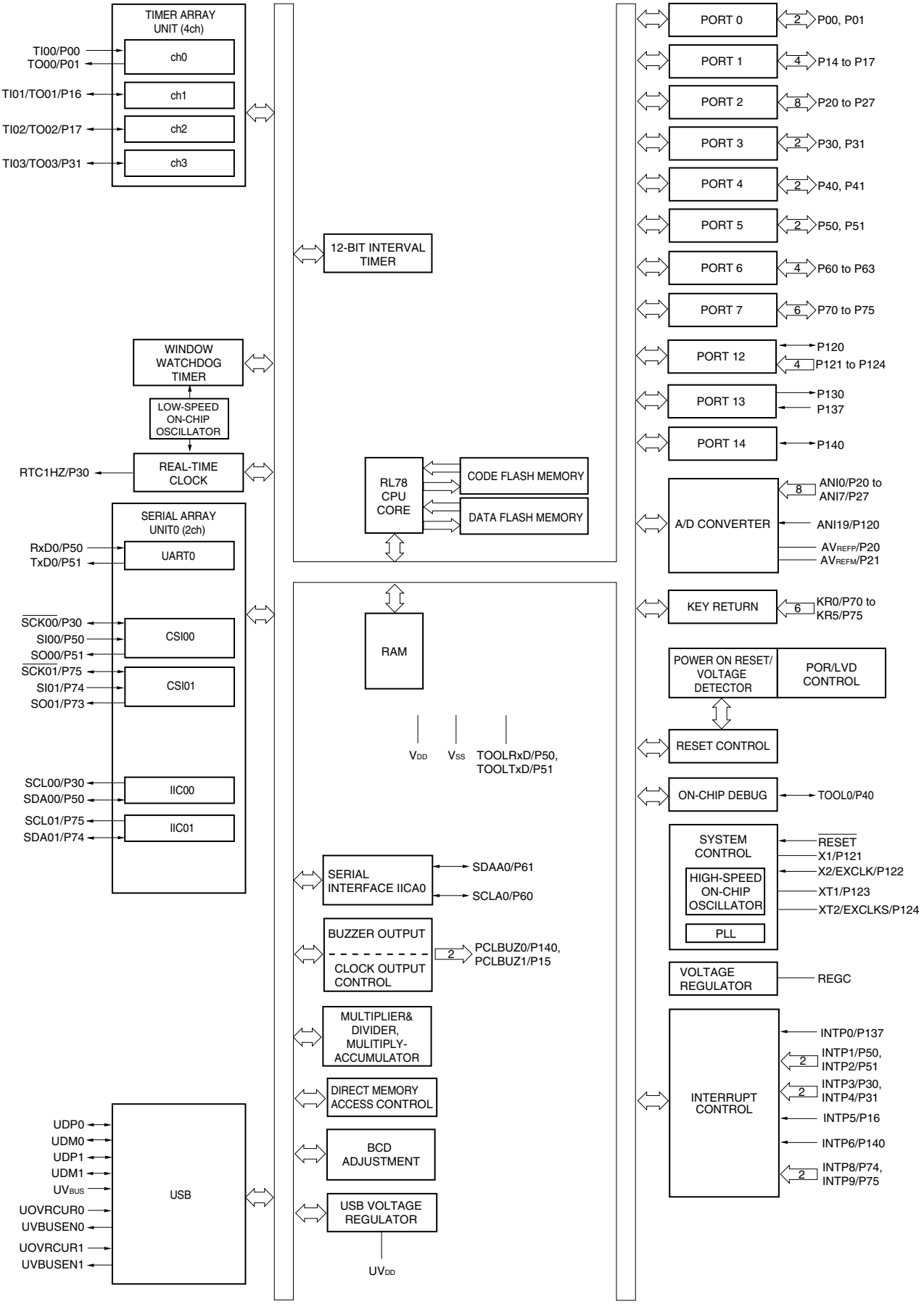
ANI0 to ANI7, ANI16, ANI17, ANI19:	Analog Input
AV_{REFM}:	Analog Reference Voltage Minus
AV_{REFP}:	Analog Reference Voltage Plus
EXCLK:	External Clock Input (Main System Clock)
EXCLKS:	External Clock Input (Sub System Clock)
INTP0 to INTP6, INTP8, INTP9:	External Interrupt Input
KR0 to KR5:	Key Return
P00, P01:	Port 0
P14 to P17:	Port 1
P20 to P27:	Port 2
P30, P31:	Port 3
P40, P41:	Port 4
P50, P51:	Port 5
P60 to P63:	Port 6
P70 to P75:	Port 7
P120 to P124:	Port 12
P130, P137:	Port 13
P140:	Port 14
PCLBUZ0, PCLBUZ1:	Programmable Clock Output/Buzzer Output
REGC:	Regulator Capacitance
$\overline{\text{RESET}}$:	Reset
RTC1HZ:	Real-time Clock Correction Clock (1 Hz) Output
RxD0:	Receive Data
$\overline{\text{SCK00}}$, $\overline{\text{SCK01}}$:	Serial Clock Input/Output
SCLA0, SCL00, SCL01:	Serial Clock Input/Output
SDAA0, SDA00, SDA01:	Serial Data Input/Output
SI00, SI01:	Serial Data Input
SO00, SO01:	Serial Data Output
TI00 to TI03:	Timer Input
TO00 to TO03:	Timer Output
TOOL0:	Data Input/Output for Tool
TOOLRxD, TOOLTxD:	Data Input/Output for External Device
TxD0:	Transmit Data
UDM0, UDM1, UDP0, UDP1:	USB Input/Output
UOVRCUR0, UOVRCUR1:	USB Input
UVBUSEN0, UVBUSEN1:	USB Output
UV_{DD}:	USB Power Supply/USB Regulator Capacitance
UV_{BUS}:	USB Input/USB Power Supply (USB Optional BC)
V_{DD}:	Power Supply
V_{SS}:	Ground
X1, X2:	Crystal Oscillator (Main System Clock)
XT1, XT2:	Crystal Oscillator (Subsystem Clock)

1.5 Block Diagram

1.5.1 32-pin products



1.5.2 48-pin products



1.6 Outline of Functions

(1/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Code flash memory (KB)		32 KB		32 KB	
Data flash memory (KB)		2 KB		2 KB	
RAM (KB)		5.5 KB Note 1		5.5 KB Note 1	
Memory space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V, 1 to16 MHz: V_{DD} = 2.4 to 5.5 V			
	High-speed on-chip oscillator	1 to 24 MHz (V_{DD} = 2.7 to 5.5 V), 1 to 16 MHz (V_{DD} = 2.4 to 5.5 V)			
	PLL clock	6, 12, 24 MHz Note 2 : V_{DD} = 2.4 to 5.5 V			
Subsystem clock		–		XT1 (crystal) oscillation 32.768 kHz (TYP.): V_{DD} = 2.4 to 5.5 V	
Low-speed on-chip oscillator		On-chip oscillation (Watchdog timer/Real-time clock/12-bit interval timer clock) 15 kHz (TYP.): V_{DD} = 2.4 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.04167 μs (High-speed on-chip oscillator: f_{HOCO} = 48 MHz /f_{IH} = 24 MHz operation)			
		0.04167 μs (PLL clock: f_{PLL} = 48 MHz /f_{IH} = 24 MHz Note 2 operation)			
		0.05 μs (High-speed system clock: f_{MX} = 20 MHz operation)			
		–		30.5 μs (Subsystem clock: f_{SUB} = 32.768 kHz operation)	
Instruction set		• Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc.			
I/O port	Total	22		38	
	CMOS I/O	16		28	
	CMOS input	3		5	
	CMOS output	–		1	
	N-ch open-drain I/O (6 V tolerance)	3		4	
Timer	16-bit timer	4 channel			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit Interval timer (IT)	1 channel			
	Timer output	4 channels (PWM output: 3)			
	RTC output	–		1 • 1 Hz (subsystem clock: f_{SUB} = 32.768 kHz)	

Notes 1. In the case of the 5.5 KB, this is about 4.5 KB when the self-programming function is used.

2. In the PLL clock 48 MHz operation, the system clock is 2/4/8 dividing ratio.

(2/2)

Item		32-pin		48-pin	
		R5F10JBC	R5F10KBC	R5F10JGC	R5F10KGC
Clock output/buzzer output		2		2	
		• 2.93 kHz, 5.86 kHz, 11.7 kHz, 1.5 MHz, 3 MHz, 6 MHz, 12 MHz (Main system clock: f_{MAIN} = 24 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation)			
8/10-bit resolution A/D converter		8 channels		9 channels	
Serial interface		CSI: 2 channels/UART: 1 channel/simplified I^2C: 2 channels			
	I^2C bus	1 channel			
USB	Host controller	2 channels	–	2 channels	–
	Function controller	1 channel			
Multiplier and divider/multiply-accumulator		• Multiplier: 16 bits × 16 bits = 32 bits (Unsigned or signed) • Divider: 32 bits ÷ 32 bits = 32 bits (Unsigned) • Multiply-accumulator: 16 bits × 16 bits + 32 bits = 32 bits (Unsigned or signed)			
DMA controller		2 channels			
Vectored interrupt sources	Internal	20		20	
	External	8		10	
Key interrupt		–		6	
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution [Note] • Internal reset by RAM parity error • Internal reset by illegal-memory access			
Power-on-reset circuit		• Power-on-reset: 1.51 ±0.03 V • Power-down-reset: 1.50 ±0.03 V			
Voltage detector		2.45 V to 4.06 V (9 stages)			
On-chip debug function		Provided			
Power supply voltage		V_{DD} = 2.4 to 5.5 V			
Operating ambient temperature		T_A = –40 to +85 °C			

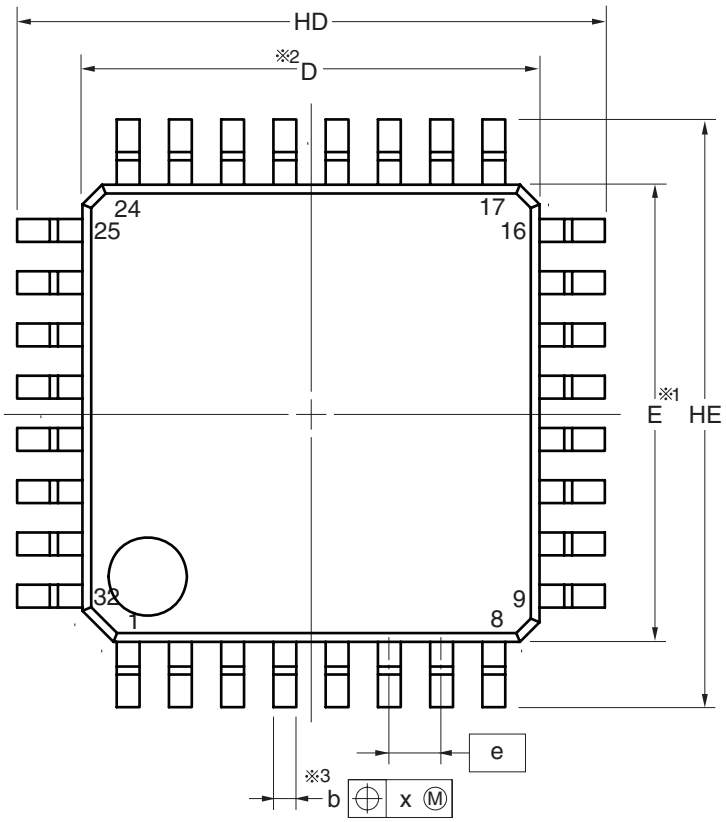
Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. PACKAGE DRAWINGS

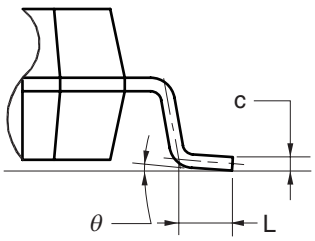
2.1 32-pin Products

R5F10JBCAFP, R5F10KBCAFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



detail of lead end



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

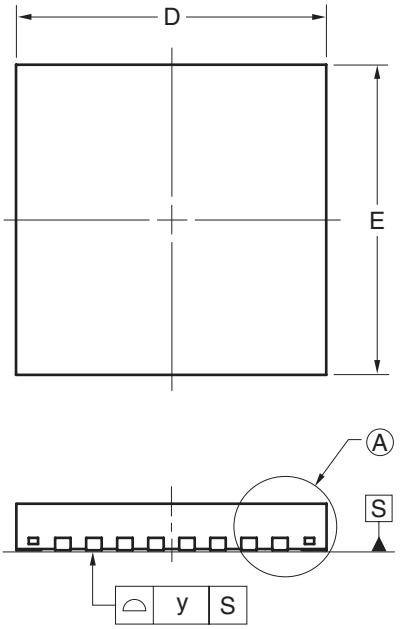
NOTE

1.Dimensions "※1" and "※2" do not include mold flash.

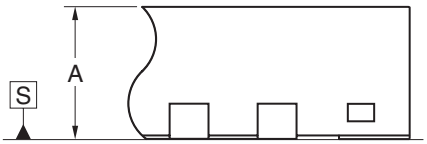
2.Dimension "※3" does not include trim offset.

R5F10JBCANA, R5F10KBCANA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-3	0.06



DETAIL OF Ⓐ PART



(UNIT:mm)

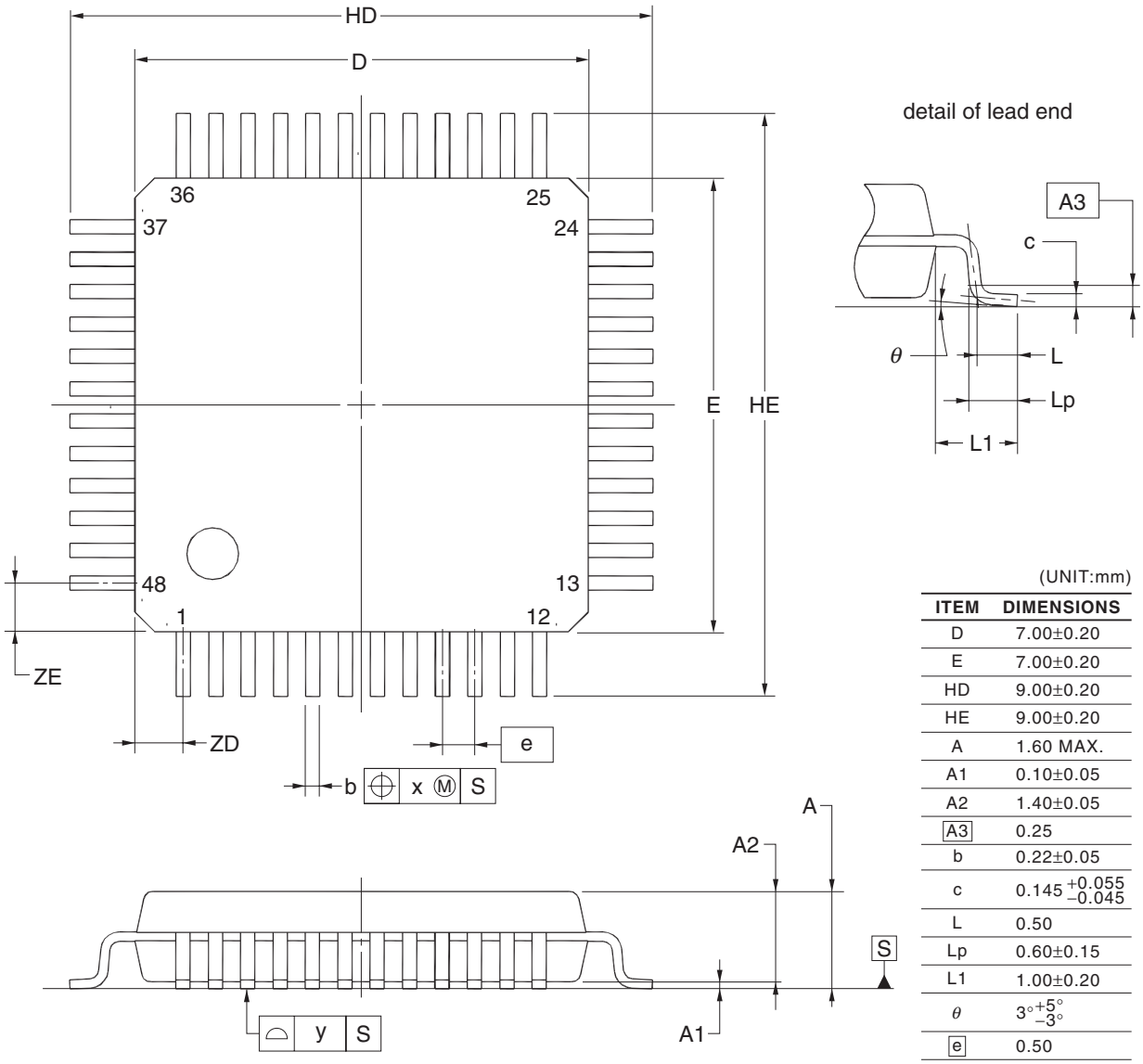
ITEM	DIMENSIONS
D	5.00±0.05
E	5.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	3.45	3.50	3.55	3.45	3.50	3.55

2.2 48-pin Products

R5F10JGCAFB, R5F10KGCAFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP48-7x7-0.50	PLQP0048KF-A	P48GA-50-8EU-1	0.16



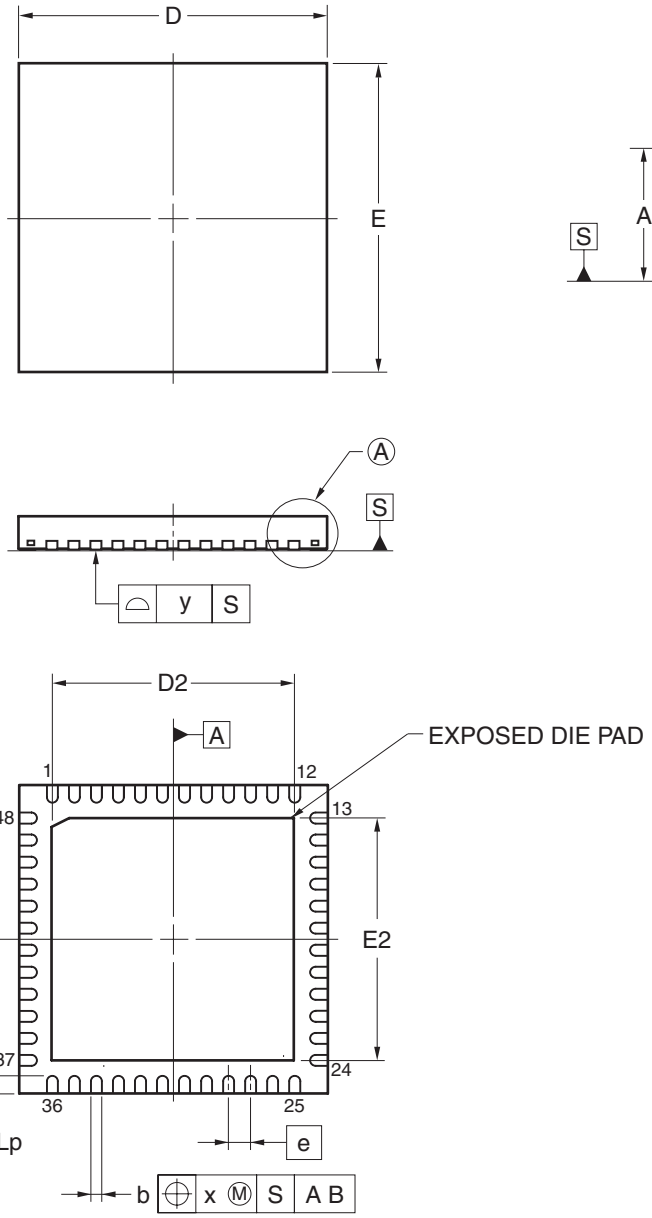
(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.20
E	7.00±0.20
HD	9.00±0.20
HE	9.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	$0.145^{+0.055}_{-0.045}$
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

NOTE
Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F10JGCANA, R5F10KGCANA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	P48K8-50-5B4-4	0.13



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.05
E	7.00±0.05
A	0.75±0.05
b	$0.25^{+0.05}_{-0.07}$
e	0.50
Lp	0.40±0.10
x	0.05
y	0.05

ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

Rev.	Date	Description	
		Page	Summary
0.01	Sep 20, 2012	-	First Edition issued

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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