

# Dual Negative Voltage Ideal Diode-OR Controller and Monitor

## FEATURES

- Controls N-Channel MOSFETs to Replace Power Schottky Diodes
- Low 15mV Forward Voltage Minimizes Dissipation
- Withstands > ±300V Transients
- Fast Turn-Off: <220ns
- Shunt Regulated for High Voltage Applications
- 4.5V Minimum Operation
- Low 350µA Quiescent Current
- 5mA Gate Pull-Up for 60Hz Applications
- High Impedance Drain Pins: <10µA Leakage
- Open Fuse and MOSFET Monitor
- 10-Pin (3mm × 3mm) DFN and MSOP Packages

## APPLICATIONS

- -48V Telecom Power
- Advanced TCA Systems
- Network Routers and Switches
- Computer Systems and Servers

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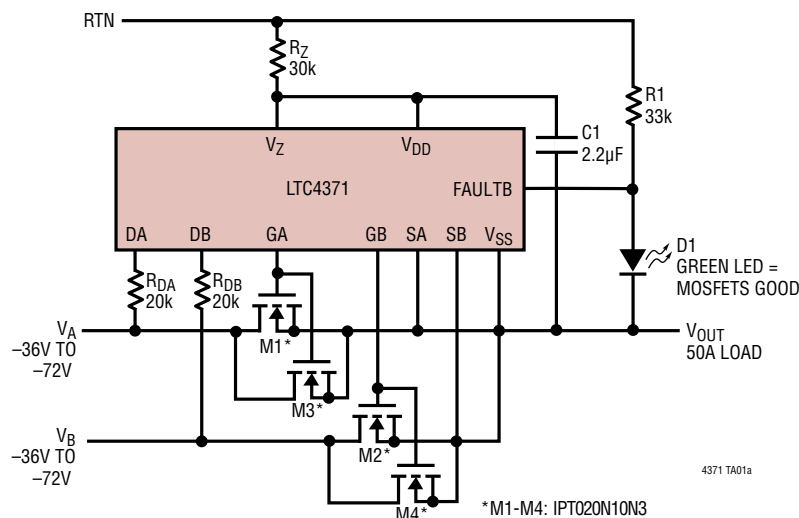
## DESCRIPTION

The LTC4371 is a two-input negative voltage ideal diode-OR controller that drives external N-channel MOSFETs as a low dissipation alternative to Schottky diodes in high power -48V systems. Low power dissipation and voltage loss eliminates the need for heatsinks and reduces PC board area. Power sources can be easily ORed together to increase total system power and reliability.

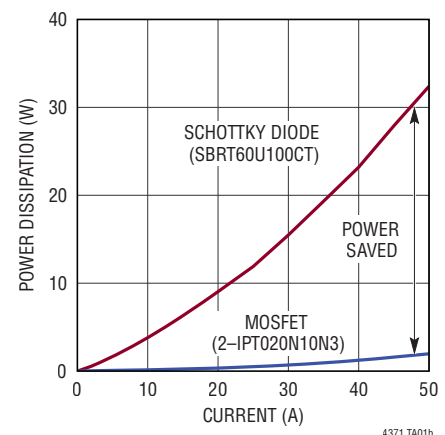
The LTC4371 tolerates ±300V transients such as those experienced during lightning-induced surges and input supply short-circuit events. The internal shunt regulator and low 350µA quiescent current allow the use of a large value dropping resistor to protect the supply pin against high voltage transients, while the high impedance drain pins can be similarly protected by high value series resistors without compromising diode operation.

The 220ns reverse current turn-off is achieved by a powerful 2A gate driver with low propagation delay, thereby minimizing peak reverse current under catastrophic fault conditions. Open MOSFET and fuse faults are indicated at the FAULTB pin, which is capable of sinking 5mA to drive an LED or opto isolator.

## TYPICAL APPLICATION



**-48V/50A Diode-OR  
Power Dissipation vs. Load Current**



# LTC4371

## ABSOLUTE MAXIMUM RATINGS

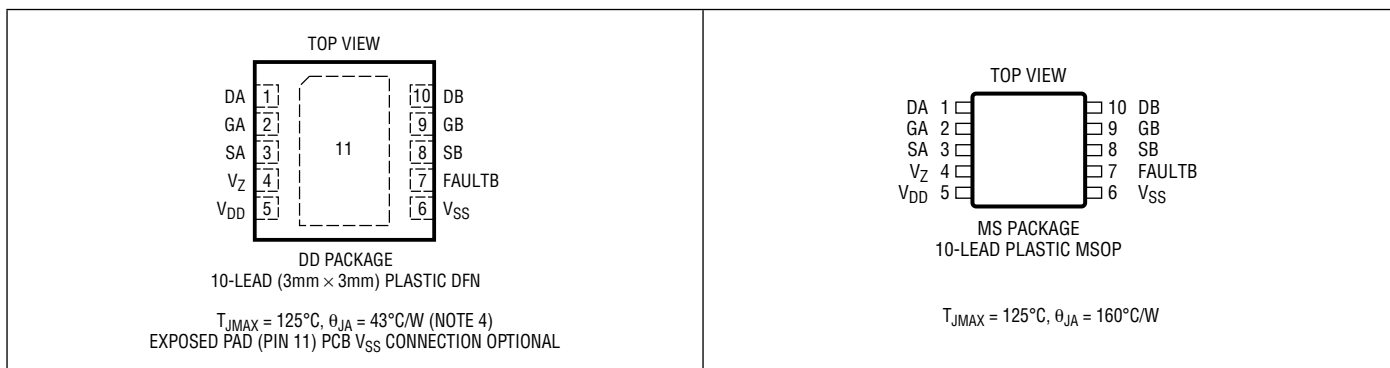
(Notes 1, 2)

Supply Voltage $V_{DD}$ .....	-0.3V to 17V
Input Voltage	
DA, DB (Note 3) .....	-40V to 100V
SA, SB .....	-0.3V to 0.3V
DC Currents	
$V_Z$ .....	20mA
DA, DB .....	$\pm 1$ mA
Single Pulse Current (6ms) DA, DB.....	10mA

Output Voltages

GA, GB.....	-0.3V to $V_{DD}$
FAULTB .....	-0.3V to 17V
Operating Ambient Temperature Range	
LTC4371C .....	0°C to 70°C
LTC4371I .....	-40°C to 85°C
Storage Temperature Range .....	-65°C to 150°C
Lead Temperature (Soldering, 10 sec)	
MS Package.....	300°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LTC4371#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC4371CDD#PBF	LTC4371CDD#TRPBF	LGSD	10-Lead (3mm × 3mm) Plastic DFN	0°C to 70°C
LTC4371IDD#PBF	LTC4371IDD#TRPBF	LGSD	10-Lead (3mm × 3mm) Plastic DFN	-40°C to 85°C
LTC4371CMS#PBF	LTC4371CMS#TRPBF	LTGSF	10-Lead Plastic MSOP	0°C to 70°C
LTC4371IMS#PBF	LTC4371IMS#TRPBF	LTGSF	10-Lead Plastic MSOP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $I_Z = 50\mu\text{A}$ ,  $V_{DD} = 12.4\text{V}$ ,  $SA = SB = V_{SS}$  unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{DD}$	Input Supply Range		● 4.5		16	V
$I_{DD}$	Input Supply Current Normal Operation Gate Fault to $V_{SS}$ , Strong Pull-Up Disabled Gate Fault to $V_{SS}$ , Strong Pull-Up Enabled	$\Delta V_{SD} = \pm 0.1\text{V}$	● 200	300	450	$\mu\text{A}$
		$V_Z = 10.4\text{V}$ , $\Delta V_{SD} = 0.1\text{V}$ , One GATE = $V_{SS}$	● 400	550	750	$\mu\text{A}$
		$I_Z = 50\mu\text{A}$ , $\Delta V_{SD} = 0.1\text{V}$ , One GATE = $V_{SS}$	● 4.5	7	9.5	$\text{mA}$
$V_Z$	Shunt Regulator Voltage	$I_Z = 50\mu\text{A}$	● 11.8	12.4	14	V
$\Delta V_Z$	Shunt Regulator Load Regulation	$I_Z = 50\mu\text{A}$ to $10\text{mA}$	●		600	$\text{mV}$
$V_{Z(PU)}$	$V_Z$ High Threshold to Enable Strong Gate Pull-Up	$V_{DD} = V_Z$ Rising	● 10.7	11.2	11.8	V
$\Delta V_{Z(PU)}$	$V_Z$ High Threshold Hysteresis			0.5		V
$V_{Z(PU)}$	$V_Z$ Low Threshold to Enable Strong Gate Pull-Up	$V_Z$ Falling	● 1.15	1.25	1.35	V
$\Delta V_{SD}$	Source-Drain Forward Servo Voltage		● 5	15	25	$\text{mV}$
$\Delta V_{GATE}$	Gate Drive ( $V_G - V_S$ )	$I_G = 0\mu\text{A}$ , $-1\mu\text{A}$ ; $\Delta V_{SD} = 100\text{mV}$	● $V_{DD} - 0.2$		$V_{DD} + 0.1$	V
$I_{GATE(UP)}$	Gate Pull-Up Current	$\Delta V_{SD} = 100\text{mV}$ , $\Delta V_{GATE} = 5\text{V}$	● -3	-5	-8	$\text{mA}$
$I_{GATE(DN)}$	Gate Pull-Down Current Strong Gate Pull-Down Current	$\Delta V_{SD} = -10\text{mV}$ , $\Delta V_{GATE} = 5\text{V}$	● 7	10	13	$\text{mA}$
		$\Delta V_{SD} = -100\text{mV}$ , $\Delta V_{GATE} = 5\text{V}$	● 1	2	3	A
$t_{OFF}$	Gate Turn-Off Time in Fault Condition	$\Delta V_{SD} = 0.1\text{V}$ Step to $-0.4\text{V}$ , $C_{GATE} = 3.3\text{nF}$ , $\Delta V_{GATE} < 1\text{V}$	●		220	ns
$I_D$	DA, DB Leakage Current MOSFET Off MOSFET Open	$V_D = 80\text{V}$	●		10	$\mu\text{A}$
		$V_D = -40\text{V}$	●		-10	$\mu\text{A}$
$R_D$	DA, DB Resistance	$\Delta V_{SD} = -50\text{mV}$ to $0.1\text{V}$	● 1	2	5	$\text{M}\Omega$
$V_{BVD}$	DA, DB Breakdown Voltage	$I_D = 10\text{mA}$ , $6\text{ms}$	● 100	130	170	V
$I_S$	SA, SB Leakage Current	$V_S = 0\text{V}$	●		$\pm 2$	$\mu\text{A}$
$\Delta V_{SD(FLT)}$	Source-Drain Fault Detection Threshold		● 150	200	225	$\text{mV}$
$V_{FAULTB}$	FAULTB Output Low	$I_{FAULTB} = 5\text{mA}$	●		0.4	V
$I_{FAULTB}$	FAULTB Leakage Current	$V_{FAULTB} = 16\text{V}$	●		$\pm 1$	$\mu\text{A}$

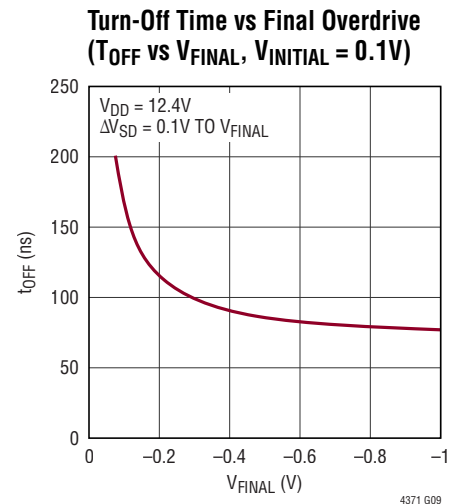
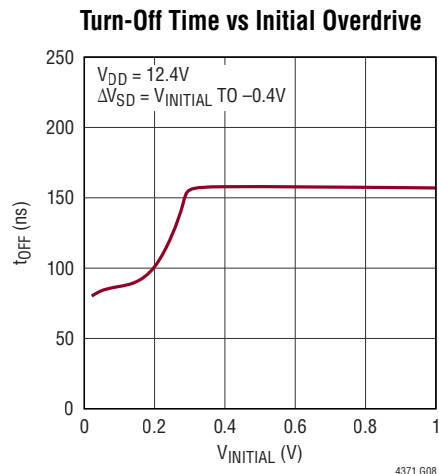
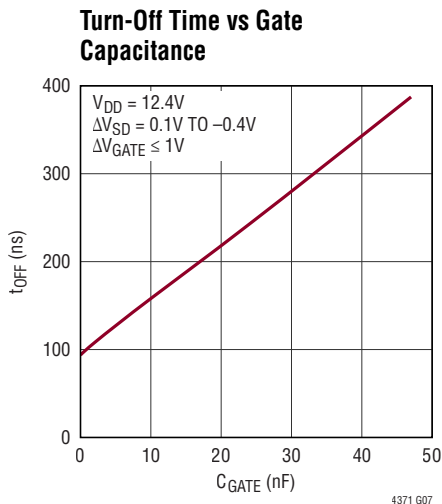
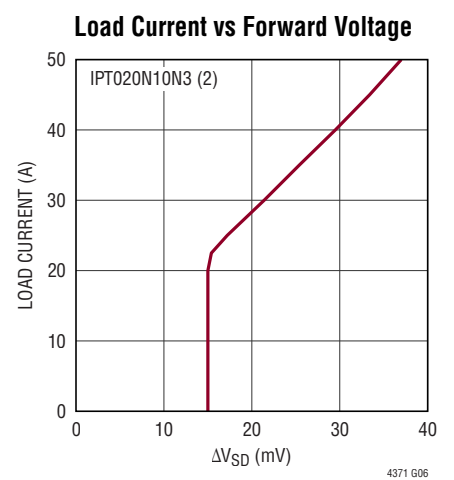
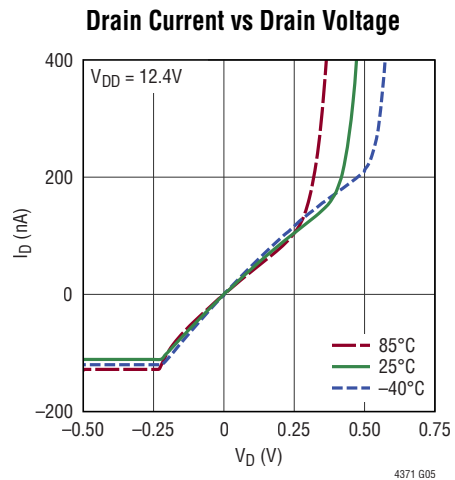
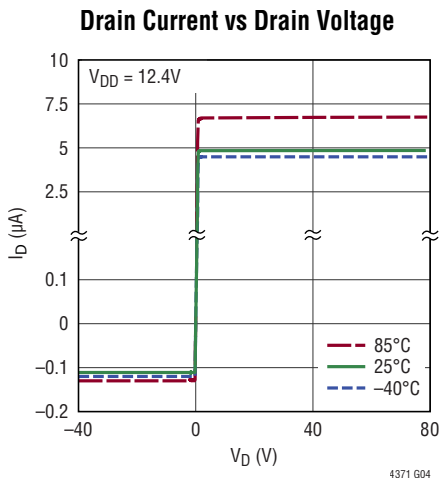
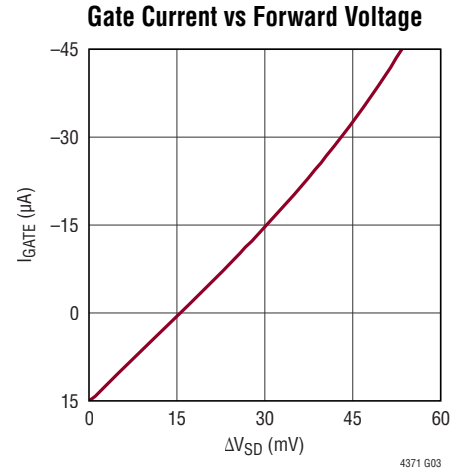
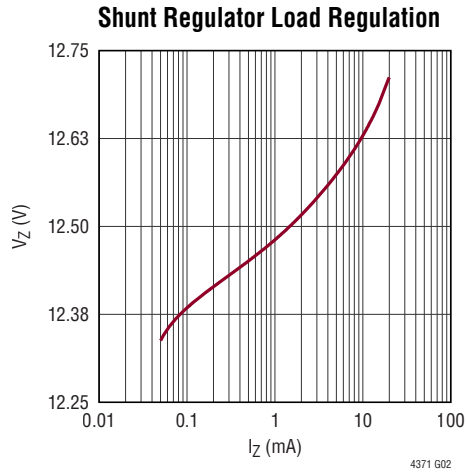
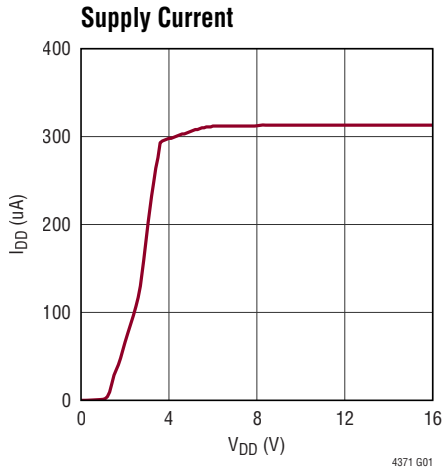
**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into pins are positive; all voltages are referenced to  $V_{SS}$  unless otherwise specified.

**Note 3:** An internal clamp limits the DA and DB pins to a minimum of  $100\text{V}$  above  $V_{SS}$  and  $-40\text{V}$  below  $V_{SS}$ . This pin can be safely tied to higher voltages through a resistance that limits the current below  $1\text{mA}$  DC or  $10\text{mA}$  for a  $6\text{ms}$  transient. Driving this pin with current beyond the clamp may damage the device.

**Note 4:** Thermal resistance is specified with exposed pad soldered to a 3-inch by 4.5-inch, four layer FR4 board. If exposed pad is not soldered  $\theta_{JA} = 93^\circ\text{C/W}$ .

## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.



## PIN FUNCTIONS

**DA, DB (Pins 1 and 10):** Drain Voltage Kelvin Sense Inputs. DA and DB connect to the drains of the N-channel MOSFETs. The voltage sensed by SA – DA and SB – DB is used to control the gate drive and hence the  $\Delta V_{SD}$  drop across the MOSFETs, and it is also used for fault detection. For accurate Kelvin sensing of  $\Delta V_{SD}$ , connect these pins as closely as possible to the MOSFET drains. An external resistor protects the DA and DB pins from transients exceeding 100V. If the LTC4371 is used in a single channel application, DA and DB may be joined together and operated in parallel; otherwise connect the unused drain pin to  $V_{SS}$ .

**Exposed Pad (Pin 11 – DD Package Only):** Exposed pad may be left open or connected to  $V_{SS}$ .

**FAULTB (Pin 7):** Fault Output. Open drain output that pulls low to indicate that one or both of the external MOSFETs have failed open. FAULTB can sink up to 5mA to drive an opto isolator or LED. The maximum allowable pull-up voltage is 17V. Connect to  $V_{SS}$  if unused.

**GA, GB (Pins 2 and 9):** Gate Drive Outputs. GA and GB operate between  $V_{SS}$  and  $V_{DD}$  to control their associated MOSFET gates and emulate the behavior of a diode. For  $\Delta V_{SD} > 15\text{mV}$ , the gate pin drives the MOSFET on, while  $\Delta V_{SD} < 15\text{mV}$  produces the opposite effect. With a large positive  $\Delta V_{SD}$ , the gate pin pulls up with a strong 5mA source, while large negative  $\Delta V_{SD}$  activates a 2A pull-down with a maximum propagation delay of 220ns. If the LTC4371 is used in a single channel application, the gate pins may be joined together and operated in parallel to realize a two-fold increase in gate drive strength; otherwise the unused gate pin may be left open.

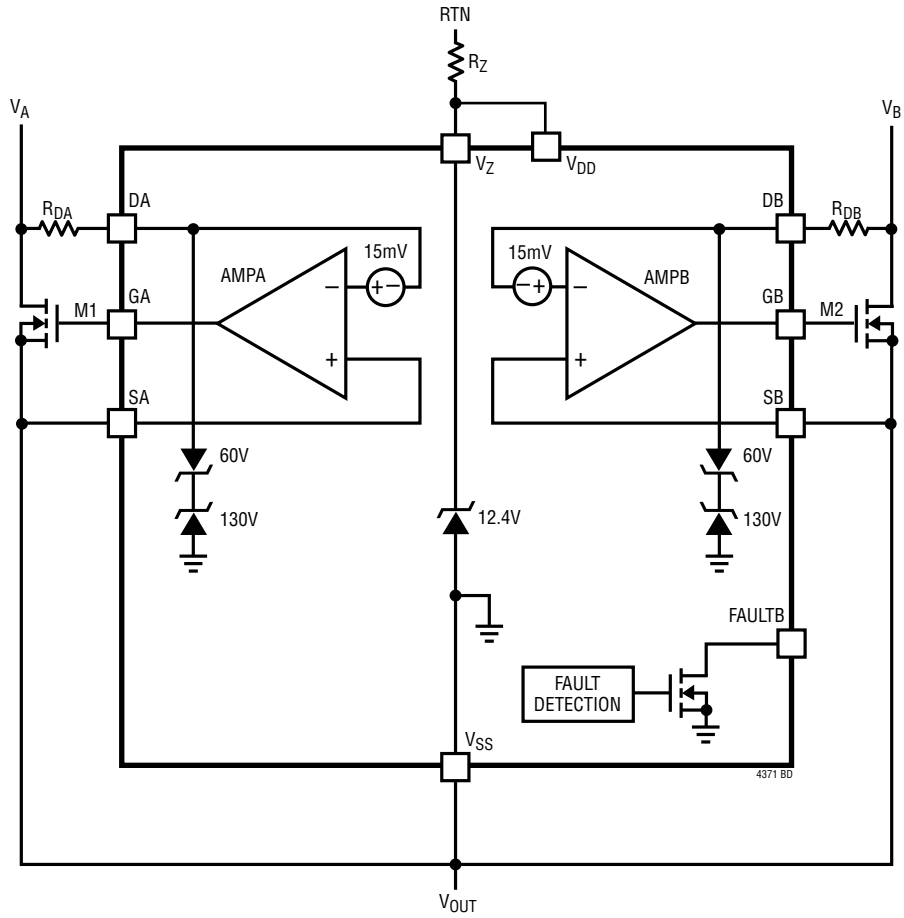
**SA, SB (Pins 3 and 8):** Source Voltage Kelvin Sense Inputs. SA and SB connect to the sources of the N-channel MOSFETs. The voltage sensed by SA – DA and SB – DB is used to control the gate drive and hence the  $\Delta V_{SD}$  drop across the MOSFETs, and it is also used for fault detection. For accurate Kelvin sensing of  $\Delta V_{SD}$ , connect these pins as close as possible to the MOSFET sources. If the LTC4371 is used in a single channel application, SA and SB may be joined together and operated in parallel; otherwise connect the unused source pin to  $V_{SS}$ .

**$V_{DD}$  (Pin 5):** Positive Supply Voltage Input. Supply  $V_{DD}$  directly from 4.5V to 16V, or in shunt regulated applications connect directly or through a buffer transistor biased by  $V_Z$ . When connected directly to  $V_Z$ , bypass  $V_{DD}$  with 2.2 $\mu\text{F}$  to  $V_{SS}$ . Maximum gate drive voltage is limited to  $V_{DD}$ .

**$V_{SS}$  (Pin 6):** Device Substrate and Negative Supply Voltage.  $V_{SS}$  connects to  $V_{OUT}$  at the joined sources of the N-channel MOSFETs.

**$V_Z$  (Pin 4):** Shunt Regulator Supply Input. This pin serves as a shunt regulator for the  $V_{DD}$  pin or as a regulator reference, and operates with a bias of 50 $\mu\text{A}$  to 10mA. Bypass with at least 100nF when used as a reference, and 2.2 $\mu\text{F}$  when connected to the  $V_{DD}$  pin. If unused, connect  $V_Z$  to  $V_{SS}$ . See “Strong Gate Pull-Up” in the Applications Information for details on the relationship between the  $V_Z$  pin voltage and gate pin drive strength.

**BLOCK DIAGRAM**



## OPERATION

The LTC4371 controls N-channel MOSFETs to emulate two ideal diodes (see Block Diagram). By sensing the MOSFET's source-to-drain voltage drop, amplifiers AMPA and AMPB control the gate of their respective external MOSFET to act as an ideal diode with a 15mV forward ( $\Delta V_{SD}$ ) drop. With low load currents, the amplifier regulates the MOSFET gate near its threshold to maintain a forward drop of 15mV. As load current increases, the gate voltage is driven higher to maintain a drop of 15mV. For very large load currents where the MOSFET gate is driven fully on, the forward drop rises linearly with current according to  $R_{DS(ON)} \cdot I_{LOAD}$ . If the forward drop is less than 15mV, or if  $\Delta V_{SD}$  reverses, the amplifier turns the MOSFET off and the load current transfers to the other channel.

When the power supply voltages are nearly equal, this regulation technique ensures that the load current is smoothly shared between the supplies without oscillation. The current balance depends on the  $R_{DS(ON)}$  of the MOSFETs and the output resistance of the supplies.

In the case of supply failure, such as supply  $V_A$ , while conducting most or all of the load current is shorted to return, a large reverse current flows from return through M1 to any load capacitance and through M2 to supply  $V_B$ . AMPA detects the current reversal and turns off M1 in less than 220ns. Fast turn-off prevents reverse current from rising to a damaging level.

The remaining supply  $V_B$  delivers load current through the body diode of M2, until the gate is driven on. With 700mV forward drop across M2, AMPB responds quickly and drives the gate with 5mA pull-up current, limiting the body diode conduction time to under 100 $\mu$ s. This minimizes power dissipation arising from switchover and

is especially important in 60Hz AC applications. As the forward drop reduces, a weaker output stage takes over and regulates the forward drop, within the limitations of  $R_{DS(ON)}$ , to 15mV.

The LTC4371 can be powered in  $-4.5V$  to  $-16V$  applications by connecting  $V_{DD}$  directly to the power supply return. In higher voltage applications or to guard against input transients,  $V_Z$  and  $V_{DD}$  can be connected together and powered from return through a bias resistor,  $R_Z$ . For repetitive 5mA gate pull-up current,  $V_{DD}$  can be driven by a buffer biased by  $V_Z$ . The  $V_Z$  pin is shunt regulated to 12.4V with respect to  $V_{SS}$  with 50 $\mu$ A minimum bias, and is capable of sinking up to 10mA.

The LTC4371 is designed to withstand high voltage transients exceeding  $\pm 300V$ , such as those experienced during lightning-induced surges and input supply short circuit events, without damage. 130V internal clamps protect drain pins DA and DB against positive spikes. External resistors  $R_{DA}$  and  $R_{DB}$  are necessary to limit the peak clamp current to less than 10mA.

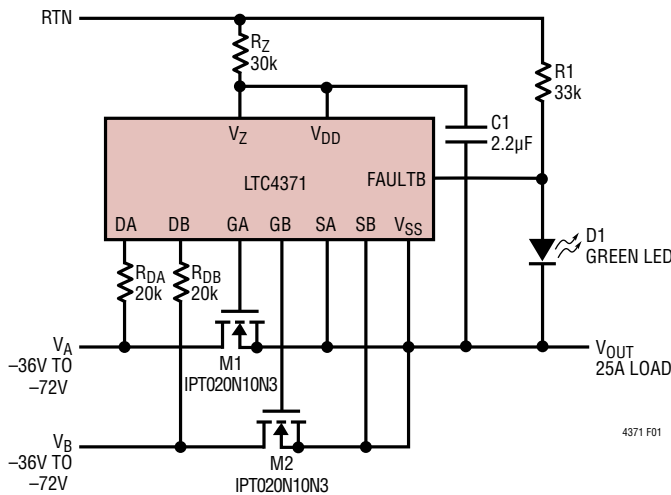
In an application circuit, negative spikes are clamped by the MOSFET's body diode to  $V_{OUT}$ , such that the drain pin never sees more than  $-700mV$  with respect to  $V_{SS}$ . A safely clamped negative transient on one input manifests itself as a positive transient on the second input and as an increased voltage from RTN to  $V_{OUT}$ . The bias resistor,  $R_Z$ , limits the current into the  $V_Z$  shunt regulator to less than 10mA.

A Fault Detection circuit monitors MOSFET  $\Delta V_{SD}$ ; FAULTB pulls low if  $\Delta V_{SD}$  of either channel exceeds 200mV while the gate is driven fully on. This is an indication of an open circuit MOSFET and can be configured for fuse monitoring by moving the drain pin connection to the input side of the fuse.

## APPLICATIONS INFORMATION

High availability systems employ parallel connected power supplies or battery feeds to achieve redundancy and enhance system reliability. Schottky diodes are a popular means of ORing these supplies together at the point of load.

The chief disadvantage of Schottky diodes is their significant forward voltage drop and resulting power and efficiency loss. This drop reduces the available supply voltage and dissipates significant power. The LTC4371 solves these problems by using an N-channel MOSFET as a low loss pass element to emulate the behavior of a diode (see Figure 1).



**Figure 1. -36V to -72V/25A Ideal Diode-OR Controller**

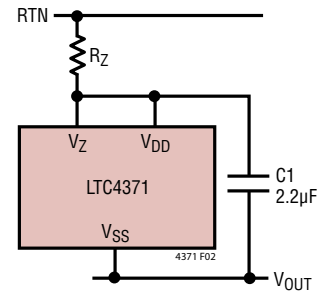
The MOSFET is turned on when power passes in the forward direction (positive current flow from source to drain), allowing for a low voltage drop from load to supply. In the reverse direction, the MOSFET is turned off to block current flow. By these means, the MOSFET is made to approach the function and performance of an ideal diode. The MOSFET voltage drop,  $\Delta V_{SD}$ , is sensed by the DA and SA, or DB and SB pins.

### Powering $V_{DD}$

The LTC4371 is fundamentally a low voltage device operating over a range of 4.5V to 16V at the  $V_{DD}$  pin, with respect to  $V_{SS}$ . The gate amplifiers are powered from the  $V_{DD}$  pin and pull-up to within 300mV of  $V_{DD}$ .

In low voltage applications such as -5V or -12V, the  $V_{DD}$  pin can be powered directly from return, with  $V_{SS}$  connected to  $V_{OUT}$ .

An internal 12.4V shunt regulator at the  $V_Z$  pin provides a means of operating the LTC4371 from higher voltage supplies. It regulates over a range of 50µA to 10mA. In the simplest configuration shown in Figure 2,  $V_{DD}$  is connected directly to  $V_Z$  and biased by resistor  $R_Z$  from the return. A 2.2µF decoupling capacitor is required to stabilize the  $V_Z$  shunt regulator, and to momentarily provide the 5mA fast pull-up current at the gate pins as needed.



**Figure 2. Simplest Solution:  $V_{DD}$  Connected Directly to  $V_Z$**

Bias resistor  $R_Z$  is chosen to bias the shunt regulator and provide the maximum  $V_{DD}$  current at the expected minimum input voltage according to:

$$R_Z < \frac{V_{IN(MIN)} - V_{Z(MIN)}}{I_{DD(MAX)} + 50\mu A} \quad (1)$$

Maximum bias resistor dissipation is calculated from:

$$P_{D(RZ)} = \frac{(V_{IN(MAX)} - V_{Z(MIN)})^2}{R_Z} \quad (2)$$

The maximum shunt regulator current must not exceed 10mA such that:

$$R_Z > \frac{V_{IN(MAX)} - V_{Z(MIN)}}{10mA} \quad (3)$$

In -48V applications a single 1206 size 30kΩ resistor is adequate to power the LTC4371. In the application shown in Figure 1, at 100V (a commonly specified maximum transient condition) peak dissipation in  $R_Z$  just exceeds 250mW, while the maximum  $V_Z$  current is slightly less than 3mA.

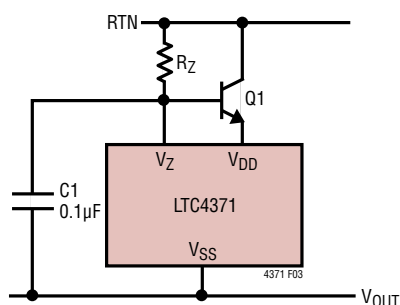
Dissipation rises in certain applications so that a larger package or multiple series units are necessary to implement  $R_Z$ . Examples include AC applications where the gate drivers demand additional current to supply repetitive



## APPLICATIONS INFORMATION

pulses from the 5mA fast pull-up, applications where the input operating voltage exceeds 72V and applications with a wide range of input voltage, particularly those where the minimum input voltage approaches the operating voltage of the LTC4371. A wide input voltage range may also result in a situation where the maximum  $V_Z$  current calculated in Equation 3 exceeds 10mA. For these cases an NPN transistor can be used to buffer the shunt regulator and power  $V_{DD}$ , as shown in Figure 3. Equation 1 becomes:

$$R_Z < \frac{V_{IN(MIN)} - V_{Z(MIN)}}{50\mu A + \frac{I_{DD(MAX)}}{\beta}} \quad (4)$$



**Figure 3.  $V_{DD}$  Connected to  $V_Z$  with NPN for Repetitive 5mA Gate Pull-Up Current**

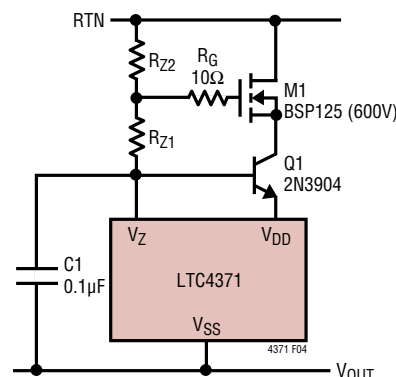
where  $50\mu A$  represents the minimum  $V_Z$  shunt regulator operating current and  $\beta$  is  $Q1$ 's DC current gain.

The maximum power dissipation in  $R_Z$  and the maximum  $V_Z$  current are calculated from Equations 2 and 3. Dissipation in emitter follower  $Q1$  is given by:

$$P_{D(Q1)} = (V_{IN(MAX)} + V_{BE} - V_{Z(MIN)}) \cdot I_{DD(MAX)} \quad (5)$$

In buffered applications, bypass  $V_Z$  with a 100nF capacitor to  $V_{SS}$ . Bypassing  $V_{DD}$  is unnecessary.

For applications at very high voltages, beyond 300V, small high voltage MOSFETs are more readily available than bipolar devices and the circuit of Figure 4 is preferred.  $R_Z$ , calculated using Equation 4, is split into two parts,  $R_{Z1}$  and  $R_{Z2}$ .  $R_{Z1}$  is sized to produce a 3V drop when operating at  $V_{IN(MIN)}$ .



**Figure 4. MOSFET Cascode for High Voltage > 250V Applications with 5mA Gate Pull-Up Current**

$R_Z$  (or  $R_{Z2}$ ) may be split into multiple segments in order to achieve the desired standoff voltage or dissipation. Whereas 1206 size resistors are commonly rated for 200V working and 400V peak, pad spacing and circuit board design rules may limit the working rating to as little as 100V.

In Figure 3, the voltage drop and power dissipation of  $Q1$  may be augmented by the use of one or more resistors in series with the collector. The same applies for  $M1$  in Figure 4.

For all applications  $R_Z$  (or  $R_{Z1} + R_{Z2}$ ) must limit the maximum  $V_Z$  current to less than 10mA, as calculated using Equation 3. If voltage transients are anticipated,  $V_{IN(MAX)}$  becomes the peak transient voltage. Transient requirements may force the use of Figure 3 or Figure 4 instead of Figure 2. The peak  $V_Z$  current may also be reduced to less than 10mA by filtering, e.g. split  $R_Z$  (or  $R_{Z2}$ ) into two equal parts and connect a bypass capacitor from the central node to  $V_{SS}$ .

### Strong Gate Pull-Up

For fast turn-on, a strong 5mA driver pulls up on the gate when the MOSFET forward drop ( $\Delta V_{SD}$ ) is large. In simple shunt-regulated applications such as shown in Figure 2, the bias resistor  $R_Z$  may be incapable of supplying 5mA. In this case, a  $2.2\mu F$  bypass capacitor is required to momentarily provide the strong pull-up current to fully charge the MOSFET gate. In normal operation the 5mA drive is not a DC condition, as it flows only long enough to deliver gate charge to the MOSFET. The amount of

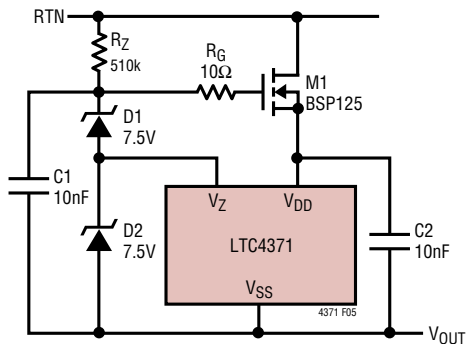
## APPLICATIONS INFORMATION

charge is approximately equal to the total gate charge,  $Q_g$ , as specified on the MOSFET's data sheet.

If there is a fault wherein the MOSFET gate is shorted to  $V_{SS}$  and  $\Delta V_{SD}$  is large, the 5mA pull-up becomes a continuous load on  $V_{DD}$ . The extra  $V_{DD}$  current overwhelms  $R_Z$  and discharges the 2.2 $\mu$ F bypass capacitor. When  $V_Z$  falls to the  $V_{Z(PU\_EN)}$  threshold of 10.7V, the 5mA pull-up current on both channels is disabled. The 5mA pull-up is enabled when  $V_Z$  recovers to 11.2V. This feature prevents a shorted gate pin from collapsing  $V_{DD}$  and, aside from disabling the 5mA pull-up, interfering with the operation of the second channel when using the configuration shown in Figure 2.

In applications such as Figure 3 and 4, if the  $V_{DD}$  supply is designed to deliver > 5mA, no  $V_{DD}$  bypassing is required. Note that a shorted gate will demand a continuous current of 5mA whenever  $\Delta V_{SD}$  is large.

The 5mA pull-up is enabled when  $V_Z$  is biased to >11.8V in its normal shunt regulator mode, or when  $V_Z$  is <1.15V. Connecting  $V_Z$  to  $V_{SS}$  permanently enables the 5mA gate pull-up. If  $V_Z$  is not used as a shunt regulator, the 5mA pull-up can be disabled by biasing  $V_Z$  to voltage between 1.35V and 10.4V (with respect to  $V_{SS}$ ) as shown in Figure 5.



**Figure 5. MOSFET Follower for High Voltage > 250V Applications with 5mA Gate Pull-Up Current Disabled**

### MOSFET Selection

The LTC4371 drives N-channel MOSFETs to conduct the load current. The important features of the MOSFETs are threshold voltage,  $V_{GS(TH)}$ ; maximum drain-source voltage,  $BV_{DSS}$ ; and on-resistance,  $R_{DS(ON)}$ .

Full gate drive for the MOSFETs ( $\Delta V_{GATE}$ ) is  $V_{DD} + 100mV/-200mV$ . When used in shunt regulated circuits such as shown in Figure 2, full gate drive lies in

the range of 11.6V to 14.1V, compatible with standard 10V-specified MOSFETs. In low voltage applications, such as where the  $V_{DD}$  pin is directly powered from less than 10V, the gate drive is compatible with logic-level and sub logic-level MOSFETs.

The drain-source breakdown rating,  $BV_{DSS}$ , must be greater than or equal to the highest input supply voltage. If an input is shorted, the full supply voltage of the opposing channel will appear across the MOSFET of the shorted channel. Avalanche may occur during input short circuits and lightning induced surges if the peak transient voltage exceeds  $BV_{DSS}$  with respect to  $V_{OUT}$ .

The LTC4371 attempts to servo the forward drop across the MOSFET ( $\Delta V_{SD}$ ) to 15mV by controlling the gate, and flags a fault if the drop exceeds 200mV when the MOSFET is driven fully on. Thus an upper bound for  $R_{DS(ON)}$  is set by:

$$R_{DS(ON)} < \frac{\Delta V_{SD(FLT)}}{I_{LOAD(MAX)}} \quad (6)$$

Where  $\Delta V_{SD(FLT)}$  is 150mV minimum.

Further,  $R_{DS(ON)}$  must be small enough to conduct the maximum load current without excessive MOSFET dissipation, which is calculated from:

$$P_{D(MOSFET)} = I_{LOAD(MAX)}^2 \cdot R_{DS(ON)} \quad (7)$$

The definition of “excessive” is provided by the circuit designer based on package and circuit board thermal constraints.

### Loop Stability

The gate amplifiers are compensated by the input capacitance of the external MOSFETs. No further compensation components are necessary except in the case of very small MOSFETs. If  $C_{ISS}$  is less than 500pF, add a 1nF capacitor across the MOSFET gate and source terminals.

### High Voltage Transient Protection

Although the LTC4371 drain pins, DA and DB are designed to handle voltages ranging from -40V to 100V with respect to  $V_{SS}$ , they may be subjected to much higher voltages, even in -48V systems. DA and DB are directly exposed to

## APPLICATIONS INFORMATION

all voltages appearing at the input. Spikes and transients may arise from various conditions including lightning induced surges, electrostatic discharge, switching of adjacent loads, and input short circuits.

The dynamic behavior of an active ideal diode entering reverse bias is most accurately characterized by a delay, followed by a period of reverse recovery. During the delay phase some reverse current is built up, limited by parasitic resistance and inductance. During the reverse recovery phase, energy stored in the parasitic inductance is transferred to other elements in the circuit.

Current slew rates during reverse recovery may reach  $100\text{A}/\mu\text{s}$  or higher. High slew rates coupled with parasitic inductance in series with the input and output can cause destructive transients to appear at the drain, source and  $V_{SS}$  pins of the LTC4371 during reverse recovery.

A zero impedance short circuit directly across the input and return is especially troublesome because it permits the highest possible reverse current to build up during the delay phase. When the MOSFET finally interrupts the reverse current, the MOSFET drain and the LTC4371 drain pins experience a positive-going voltage spike, while the MOSFET source and the LTC4371 source and  $V_{SS}$  pins spike in the negative direction. To protect the circuit biasing  $V_{DD}$ , clamp or bypass  $V_{OUT}$  as close as possible to the junction of the MOSFET sources and  $V_{SS}$  and the point where the  $V_{DD}$  bias circuit connects to return.

The positive spike at the input is clamped to  $BV_{DSS}$  relative to  $V_{OUT}$  by MOSFET avalanche.  $BV_{DSS}$  is inadequate protection for the DA and DB pins, as shall be discussed later. Although the energy stored in parasitic inductance during input short circuit faults is at least two orders of magnitude smaller than the avalanche energy rating of most MOSFETs, the peak current may exceed the avalanche current rating of the MOSFET. In this case and if positive-going transient energy from other external sources exceeds the MOSFET's avalanche energy rating, add TVS clamps across each MOSFET as shown in Figure 6.

Externally applied input transients in the negative direction are clamped by the body diodes of the MOSFETs to  $-700\text{mV}$  with respect to  $V_{OUT}$ , if not connected directly through  $R_{DS(ON)}$  to  $V_{OUT}$ , and pose no particular hazard for the DA and DB pins. Negative input transients couple directly to the output which increases the RTN to  $V_{OUT}$  voltage. Although the shunt resistor,  $R_Z$ , limits the current into  $V_Z$  to a safe level of less than  $10\text{mA}$ , an output capacitor or TVS clamp may be required to protect downstream circuitry from negative input transients.

$100\text{V } BV_{DSS(MIN)}$  MOSFETs are commonly used in  $-48\text{V}$  applications, but  $BV_{DSS(MAX)}$  is not guaranteed and cannot be relied upon to protect the DA and DB pins from exceeding their absolute maximum rating of  $100\text{V}$ . Nevertheless, the  $100\text{V}$  absolute maximum rating for DA and DB may be safely exceeded if certain precautions are taken. The internal  $130\text{V}$  clamps shown in the Block Diagram tolerate

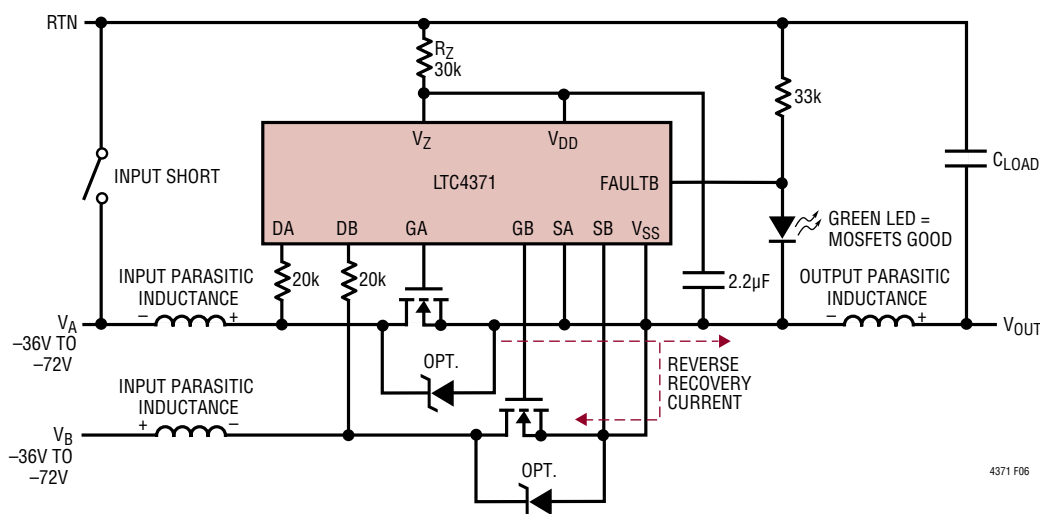


Figure 6. Input Short Circuit Parasitics and Protection Against High Voltage Transients

## APPLICATIONS INFORMATION

up to 10mA for 6ms in breakdown. For protection against transients exceeding 100V, add series resistors  $R_{DA}$  and  $R_{DB}$  according to:

$$R_{DA}, R_{DB} > \frac{V_{IN(PK)} - V_{BVD(MIN)}}{10mA} \quad (8)$$

where  $V_{IN(PK)}$  is the peak input voltage measured with respect to  $V_{SS}$ , and  $V_{BVD(MIN)}$  is the minimum drain pin breakdown voltage (100V).

Because their presence incurs no particular performance penalty, a minimum value of 20k $\Omega$  is prudent and protects the DA and DB pins against transients up to 300V, as shown in Figure 7. A practical limit for  $R_{DA}$  and  $R_{DB}$  is 100k $\Omega$ , beyond which their resistance interferes with the operation of the gate amplifier. Some speed penalty is incurred for values greater than 20k $\Omega$ , as shown in Figure 8. If the speed penalty is unacceptable, add a resistor and capacitor across  $R_{DA}$  and  $R_{DB}$  as shown in Figure 9 to restore the response time.

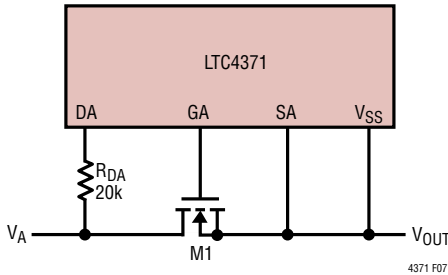


Figure 7. 300V Drain Pin Protection

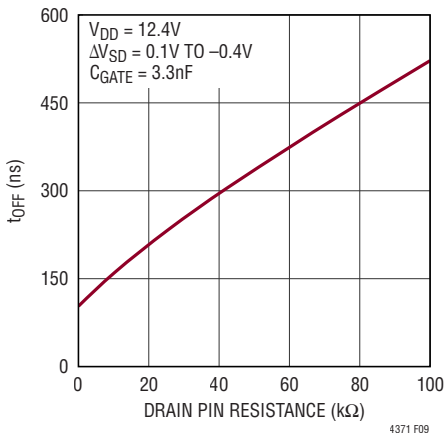


Figure 8. Reverse Response Time vs. Drain Pin Resistance

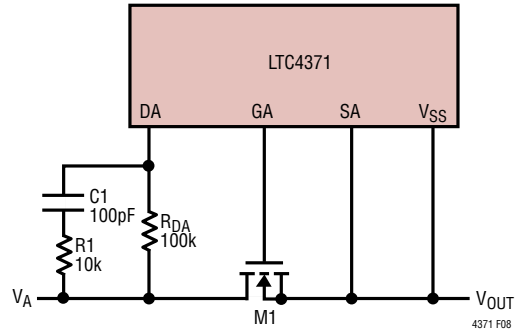


Figure 9. High Voltage Drain Pin Protection with C1 and R1 Maintaining Fast Turn-Off Time

### High Voltage DC Applications

An extra blocking device is necessary to protect the DA and DB pins in applications where the DC input voltage exceeds 100V. Even in -48V applications the equivalent DC input voltage may exceed 100V, as a result of a reverse connected supply feed that can impress up to double the maximum operating voltage across the inputs.

Because the 130V DA and DB pin clamps are limited to clamping short-term spikes, some other means of limiting the maximum applied voltage is necessary in DC applications. The N-channel cascode shown in Figure 10 extends the DC input operating voltage to 600V. It safely clamps the drain pin to about 2V less than  $V_Z$ , yet introduces only 500 $\Omega$  series resistance when the input is in the vicinity of  $V_{OUT}$ ; fast turn-off time is maintained.

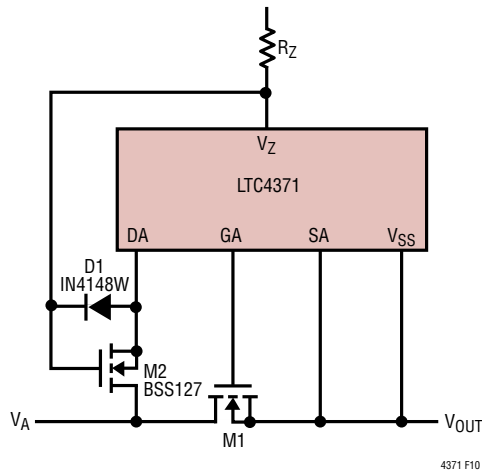


Figure 10. Drain Protection for Applications Up to -600V

## APPLICATIONS INFORMATION

### Fuse and Open MOSFET Detection

The LTC4371 monitors  $\Delta V_{SD}$  of each channel as measured across SA – DA and SB – DB. If  $\Delta V_{SD}$  of either channel exceeds 200mV and the associated gate pin is driven fully on, FAULTB pulls low to indicate a fault. Conditions leading to high  $\Delta V_{SD}$  include excessive load current ( $I_{LOAD} \times R_{DS(ON)} > 200mV$ ), an open circuit MOSFET or an open fuse placed in series with the MOSFET. A high  $\Delta V_{SD}$  fault is detected on only the highest voltage input supply, i.e. the path that should be supplying power is, as a result of one of the aforementioned conditions, unable to do so. Temporary conditions, such as the initial 700mV drop experienced when an input first rises to the point of supplying current but before the gate has been driven on, are masked since the gate must also be high for fault detection.

The  $\Delta V_{SD}$  monitor can be used to detect open fuses, as shown in Figure 11. An open fuse gives the same signature as an open MOSFET:  $\Delta V_{SD}$  increases beyond 200mV when the affected input surpasses the opposing channel.

The connection shown in Figure 11 introduces a new problem: an open fuse and open MOSFET exposes the DA and DB pins to high negative voltage with respect to  $V_{SS}$ . Diodes D1 and D2 clamp the DA, DB pins from exceeding the absolute maximum of –40V with respect to  $V_{SS}$ .

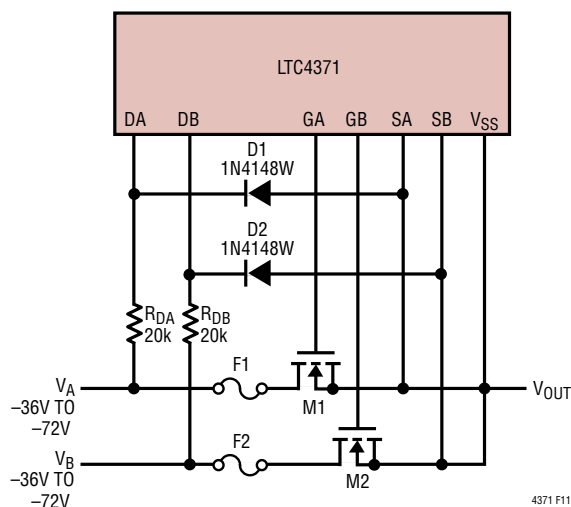
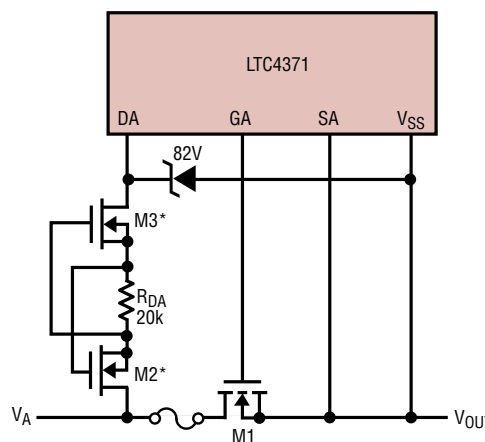


Figure 11. Fuse and Open MOSFET Detection

Figure 12 shows a protection method that extends DA and DB pin operation to  $\pm 600V$ . The drain pins are clamped by an 82V Zener diode. As shown, the DA pin is clamped at 82V with respect to  $V_{SS}$  in the positive direction, and 700mV below  $V_{SS}$  in the negative direction. When a high input voltage of either polarity is present, back-to-back depletion mode N-channel MOSFETs limit the current in the Zener diode to  $V_{GS(TH)}/R_{DA}$  ( $100\mu A$  for  $R_{DA} = 20k\Omega$ ), a value that is indefinitely sustainable.



\*M2, M3: BSP135 (600V) DEPLETION NMOS

4371 F12

Figure 12. Back-to-Back Drain Pin Limiter for  $\pm 600V$

### FAULTB Pin

The open drain FAULTB pin pulls low when the  $\Delta V_{SD}$  of either channel exceeds 200mV, while its gate is driven fully on. FAULTB can sink 5mA to drive an LED for visual indication, or an opto isolator to communicate across an isolation barrier. The FAULTB pin voltage is limited to 17V absolute maximum with respect to  $V_{SS}$  in the high state and cannot be pulled up to return except in low voltage applications.

In Figure 13, the FAULTB pin is used to shunt current away from a green LED; the LED indicates (illuminates when) no fault condition is present. The operating voltage is limited at the low end by the minimum acceptable LED current, and at the high end by the FAULTB pin’s 5mA capability.

Figure 14 shows a simple implementation driving a red LED; the LED indicates a fault condition is present. While this simple configuration works well in –48V applications, the maximum operating voltage is limited to 100V, the LED

## APPLICATIONS INFORMATION

current varies widely with operating voltage, and dissipation in the 20kΩ resistor reaches ≈250mW at 72V input. These shortcomings are eliminated by the slightly more complex circuit shown in Figure 15. A cascode shields the FAULTB pin from the high input voltage and dissipates no power under normal conditions, while the LED current remains constant regardless of input voltage when indicating a fault. At 600V, cascode dissipation reaches 600mW maximum.

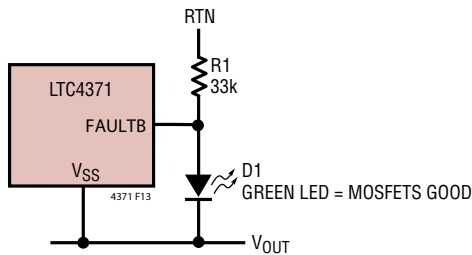


Figure 13. FAULTB Drives a Green LED in Shunt Mode

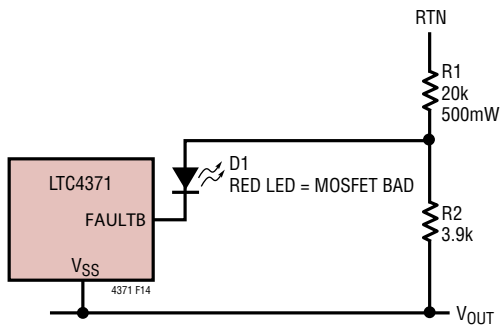


Figure 14. FAULTB Drives a Red LED in Series Mode

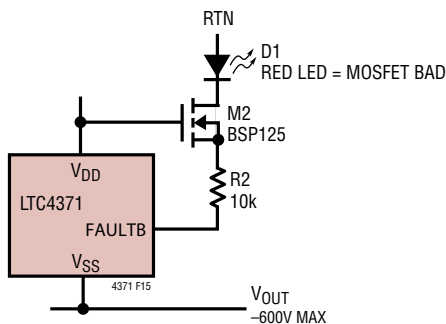


Figure 15. FAULTB Driving an LED in a High Voltage Application

## Layout Considerations

A sample layout for the LTC4371 DFN package and PG-HSOF-8 MOSFET package is shown in Figure 16.

The  $V_{DD}$  bypass capacitor C1 provides AC current to the device; place it as close to  $V_{DD}$  and  $V_{SS}$  pins as possible. Connect the gate amplifier input pins, DA, DB, SA and SB, directly to the MOSFETs' drain and source terminals using Kelvin connections for good accuracy. Place the MOSFET sources as close together as possible, with  $V_{SS}$  connecting at their intersection.

Keep the traces to the MOSFET drains and common source wide and short. A good rule-of-thumb for minimizing self-heating effects in the copper traces is to allow at least 1-inch trace width per 50 amperes, for a surface layer of 1-ounce copper. This current density corresponds to a self-heating effect of about 1.3W per square inch. The traces associated with the power path through the MOSFETs must have low resistance to maintain good efficiency and low drop. The resistance of 1-ounce copper is approximately  $500\mu\Omega$  per square.

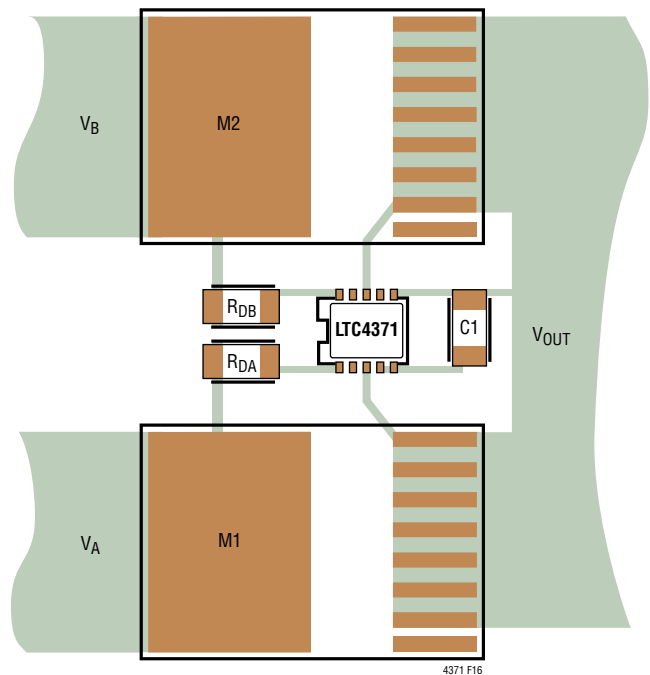


Figure 16. Recommended PCB Layout for M1, M2 and C1

## APPLICATIONS INFORMATION

### Design Example

The following design example demonstrates the calculations involved for selecting external components. Consider a  $-48\text{V}$  application with a  $-36\text{V}$  to  $-72\text{V}$  operating range,  $200\text{V}$  peak transient and  $25\text{A}$  maximum load current (see Figure 17).

The simplest configuration is chosen to power  $V_{DD}$ , since this arrangement easily handles the operating conditions found in a  $-48\text{V}$  telecom power system. The bias resistor,  $R_Z$ , is calculated from Equation 1:

$$R_Z < \frac{36\text{V} - 11.8\text{V}}{750\mu\text{A}} = 32.2\text{k}\Omega \quad (9)$$

The nearest lower 5% value is  $30\text{k}\Omega$ .

The worst case power dissipation in  $R_Z$ :

$$P_{D(RZ)} = \frac{(72\text{V} - 11.8\text{V})^2}{30\text{k}} = 166\text{mW} \quad (10)$$

A  $30\text{k}\Omega$   $0.25\text{W}$  resistor is selected for  $R_Z$ . The maximum  $V_Z$  current is confirmed from Equation 3 as a safe value of  $2\text{mA}$ . A  $-200\text{V}$  transient pushes this to  $6.3\text{mA}$ , safely below the maximum allowable  $V_Z$  current of  $10\text{mA}$ .

Next, choose the N-channel MOSFET. The  $100\text{V}$ ,  $\text{IPT020N10N3}$  in a  $\text{PG-HSOF-8}$  package with  $R_{DS(ON)} = 2\text{m}\Omega$  (max) offers a good solution.

The maximum voltage drop across the MOSFET is:

$$\Delta V_{SD} = 25\text{A} \cdot 2\text{m}\Omega = 50\text{mV} \quad (11)$$

which is well below the  $150\text{mV}$  minimum  $\Delta V_{SD}$  fault threshold.

From Equation 7, the maximum power dissipation in the MOSFET is:

$$P_{D(\text{MOSFET})} = 25\text{A}^2 \cdot 2\text{m}\Omega = 1.25\text{W} \quad (12)$$

a reasonable value for the proposed package.

The minimum recommended value of  $20\text{k}\Omega$  is chosen for  $R_{DA}$  and  $R_{DB}$ .  $20\text{k}\Omega$  protects the DA and DB pins to  $300\text{V}$ .

The LED, D1, requires at least  $1\text{mA}$  of current to turn on fully; therefore,  $R_1$  is set to  $33\text{k}$  to accommodate the minimum input supply voltage of  $-36\text{V}$ . The maximum current is  $2\text{mA}$  at  $-72\text{V}$ , but excursions to  $200\text{V}$  give  $6\text{mA}$ , slightly beyond the FAULTB pin's  $5\text{mA}$  capability. This means that if there is a fault present, a brief glitch might cause a "no fault" indication during a  $200\text{V}$  transient. Since D1 is a visual indicator, we'll accept the remote chance of a dim flash in exchange for the simple circuit solution.

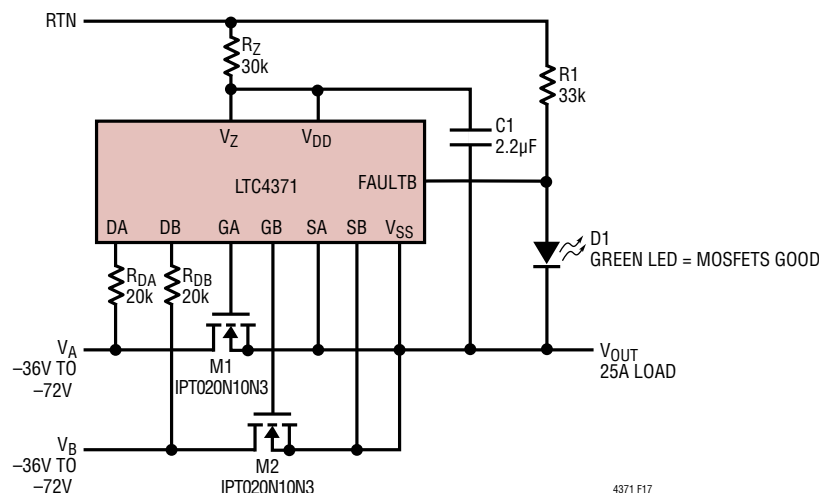


Figure 17.  $-36\text{V}$  to  $-72\text{V}/25\text{A}$  Ideal Diode-OR

## APPLICATIONS INFORMATION

As a second design example, consider modifying the circuit of Figure 17 to handle 300V transients and to drive a red LED, which illuminates when a fault is present (see Figure 18).  $R_{DA}$  and  $R_{DB}$  are sized to handle transients to 300V, so no change in their value is necessary. Modifications are necessary to drive the red LED.

A PZTA42, a 300V NPN with a minimum  $\beta = 20$  is chosen to supply both the LED and the  $V_{DD}$  pin. With a maxi-

imum  $I_{DD}$  of 9.5mA (LTC4371) + 1mA (LED) = 10.5mA, Equation 4 gives:

$$I_{BASE} = \frac{10.5mA}{20} = 525\mu A \quad (13)$$

$$R_Z < \frac{36V - 11.8V}{50\mu A + \frac{10mA}{20}} = 44k$$

The nearest lower 5% value is 43k.

To produce 1mA LED current with variations in the circuit,  $R_1$  is chosen to be 8.2k.

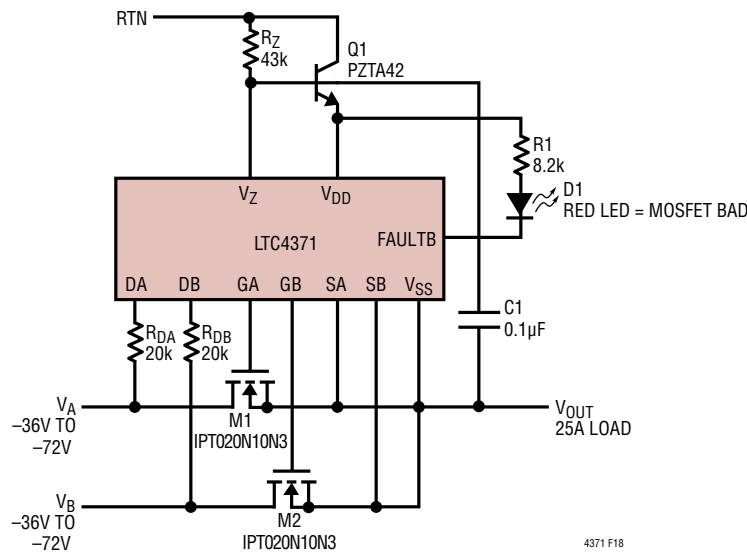


Figure 18. -36V to -72V/25A Ideal Diode-OR



TYPICAL APPLICATIONS

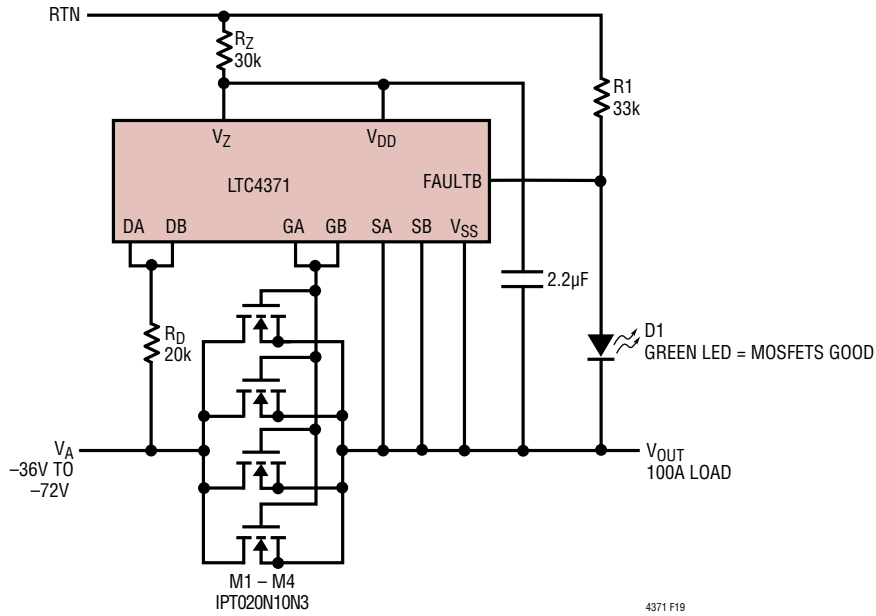


Figure 19. -36V to -72V Single Channel Parallel Application with 2x Gate Drive

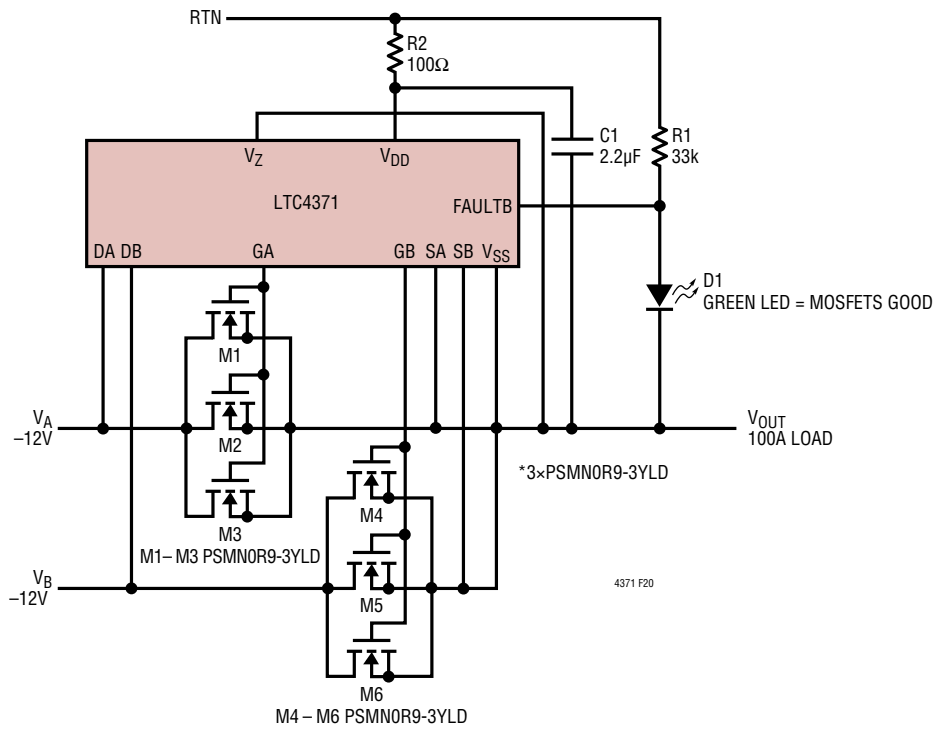


Figure 20. -12V/100A Application with 5mA Gate Pull-Up Enabled

TYPICAL APPLICATIONS

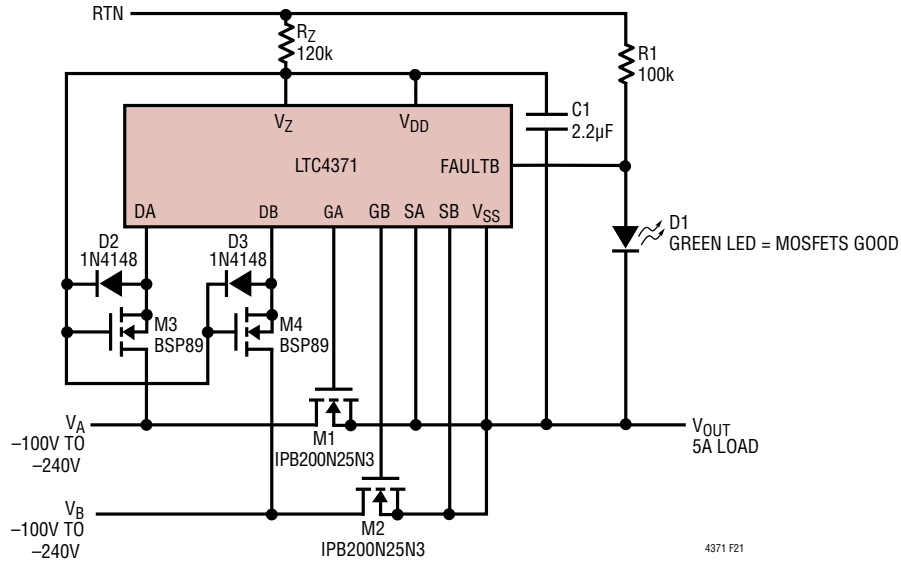


Figure 21. -100V to -240V/5A Ideal Diode-OR Controller

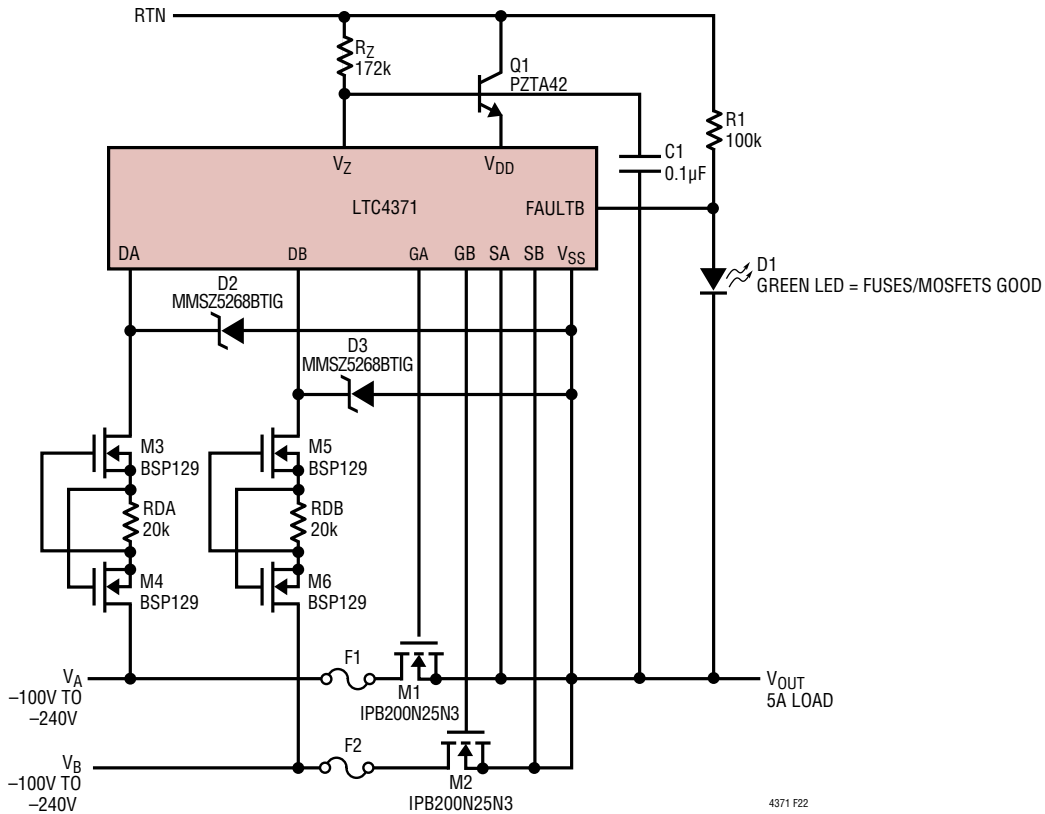


Figure 22. -100V to -240V/5A Ideal Diode-OR Controller with Open Fuse and MOSFET Detection

TYPICAL APPLICATIONS

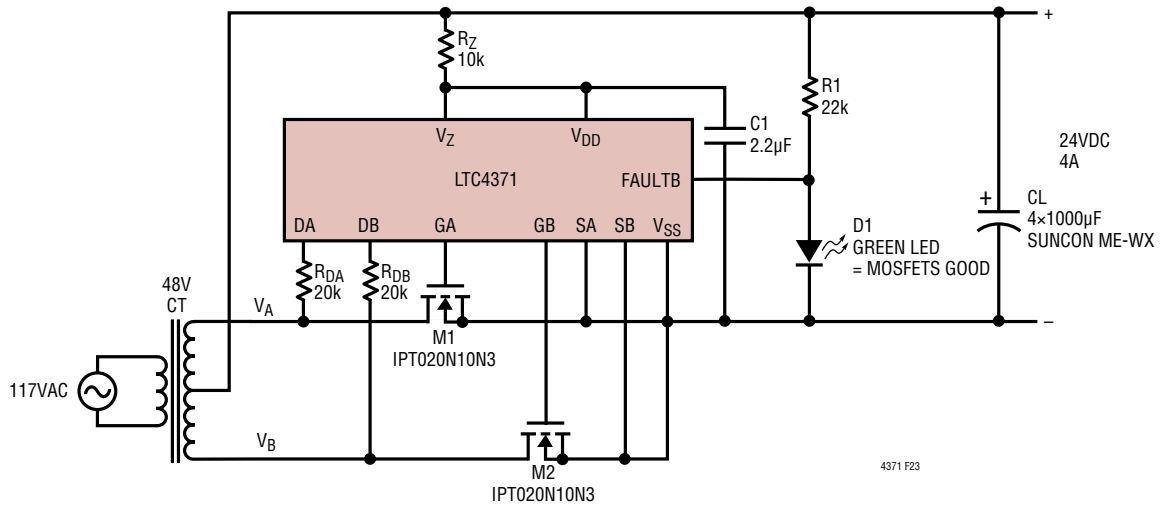
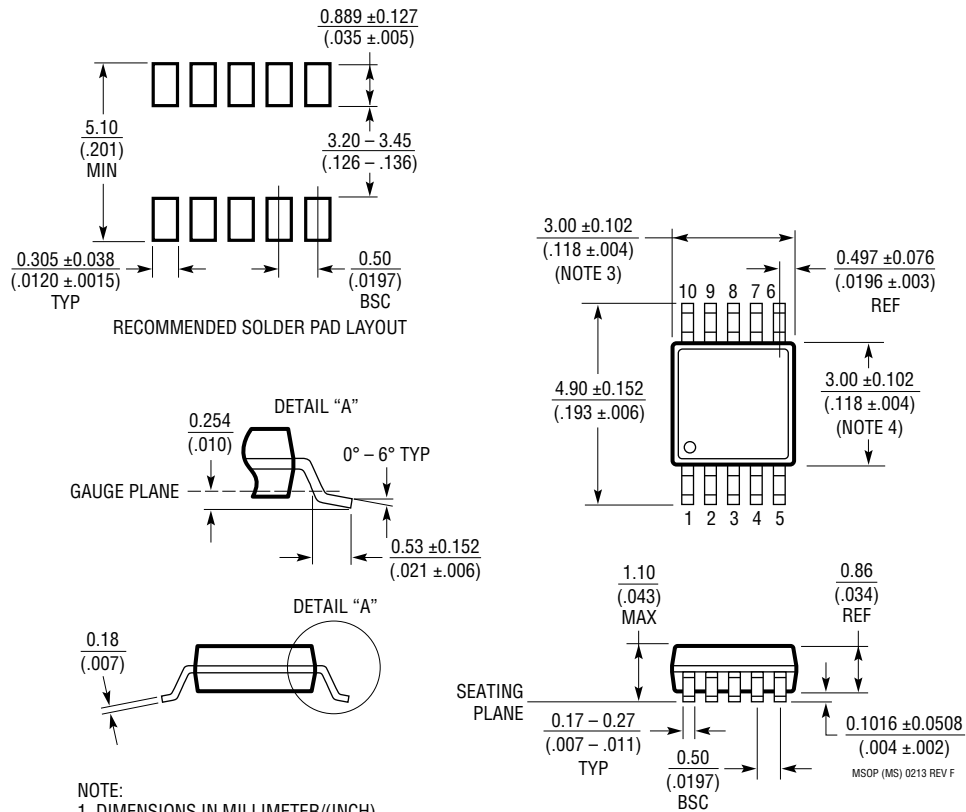


Figure 23. Full Wave Center Tap Rectifier

## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/4371#packaging> for the most recent package drawings.

### MS Package 10-Lead Plastic MSOP (Reference LTC DWG # 05-08-1661 Rev F)



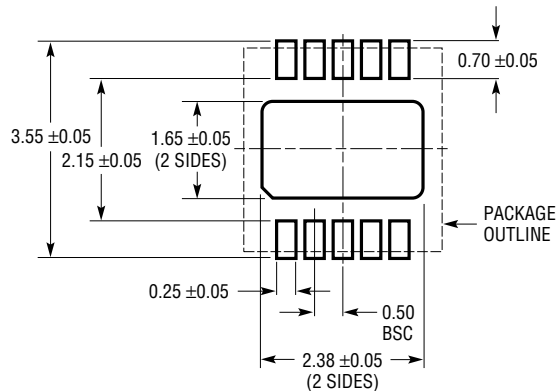
**NOTE:**

1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.  
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.  
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

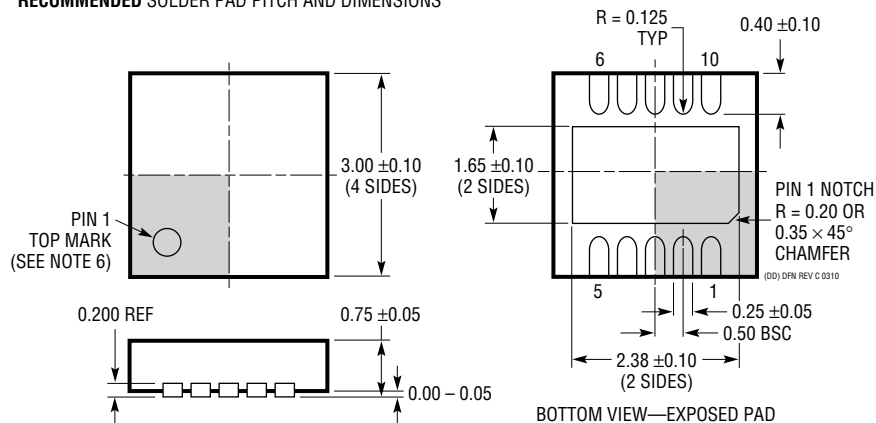
## PACKAGE DESCRIPTION

Please refer to <http://www.linear.com/product/4371#packaging> for the most recent package drawings.

### DD Package 10-Lead Plastic DFN (3mm × 3mm) (Reference LTC DWG # 05-08-1699 Rev C)



#### RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

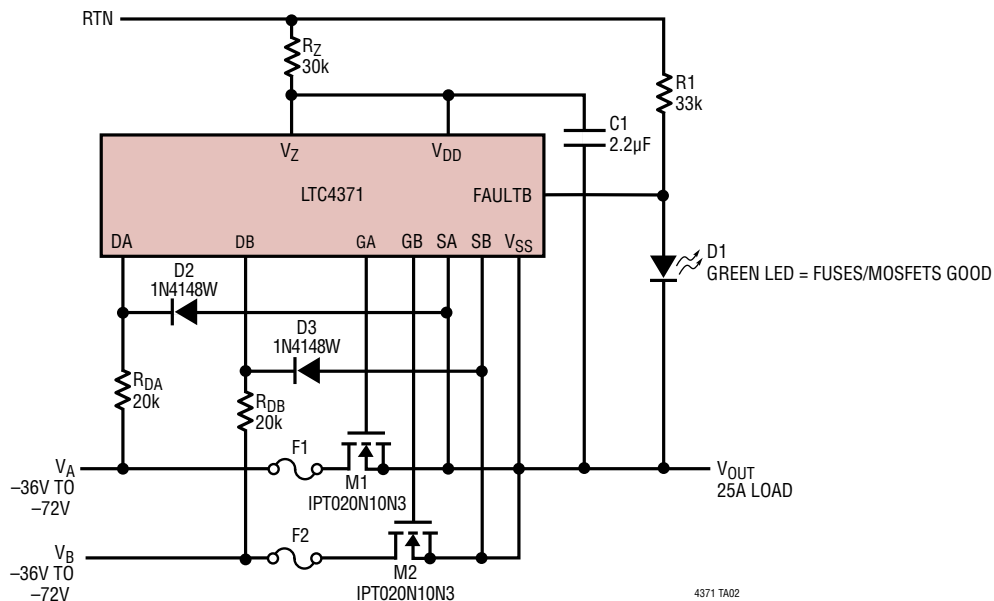


#### NOTE:

- DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
- DRAWING NOT TO SCALE
- ALL DIMENSIONS ARE IN MILLIMETERS
- DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
- EXPOSED PAD SHALL BE SOLDER PLATED
- SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

## TYPICAL APPLICATION

### -48V Ideal Diode-OR with Fuse and Open MOSFET Detection



## RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
<a href="#">LTC4354</a>	Negative Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 1.2µs Turn-Off, -80V Operation
<a href="#">LTC4355</a>	Positive Voltage Diode-OR Controller and Monitor	Controls Two N-Channel MOSFETs, 0.4µs Turn-Off, 80V Operation
<a href="#">LTC4357</a>	Positive Voltage Ideal Diode Controller	Controls Single N-Channel MOSFET, 0.5µs Turn-Off, 80V Operation
<a href="#">LT<sup>®</sup>4250</a>	-48V Hot Swap Controller	Active Current Limiting, Supplies from -20V to -80V
<a href="#">LTC4251/LTC4251-1/ LTC4251-2</a>	-48V Hot Swap Controllers in SOT-23	Fast Active Current Limiting, Supplies from -15V
<a href="#">LTC4252-1/LTC4252-2/ LTC4252-A1/LTC4252-A2</a>	-48V Hot Swap Controllers in MS8/MS10	Fast Active Current Limiting, Supplies from -15V, Drain Accelerated Response
<a href="#">LTC4261/LTC4261-2</a>	Negative Voltage Hot Swap Controllers with ADC and I <sup>2</sup> C Monitoring	10-Bit ADC, Floating Topology, Adjustable Inrush

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[MAX9959DCCQ+D](#) [MAX1932ETC+T](#) [MAX1856EUB+T](#) [STNRG011TR](#) [IRPS5401MXI03TRP](#) [S6AE102A0DGN1B200](#)  
[MMPF0100FDAEP](#) [MCZ33903DS5EK](#) [S6AE101A0DGNAB200](#) [NCP6924CFCHT1G](#) [MAX17117ETJ+](#) [L9916](#) [L9915-CB](#)  
[MCZ33905DS3EK](#) [MMPF0100FCANES](#) [MMPF0100FBANES](#) [WM8325GEFL/V](#) [MCZ33903DP5EK](#) [MCZ33905DS5EK](#)  
[MCZ33903DD5EK](#) [ADN8835ACPZ-R7](#) [MCZ33903DP5EKR2](#) [MCZ33903DD3EK](#) [MMPF0100FAAZES](#) [SLG7NT4198V](#) [MIC5164YMM](#)  
[P9180-00NHGI](#) [NCP6914AFCAT1G](#) [TLE9261QX](#) [TEA1998TS/1H](#) [MAX881REUB+T](#) [TLE9262QX](#) [TLE8880TN](#) [MAX8520ETP+T](#)  
[SLG7NT4083V](#) [ADP1031ACPZ-1-R7](#) [ADP1031ACPZ-2-R7](#) [ADP1031ACPZ-3-R7](#) [ADP1031ACPZ-4-R7](#) [ADP1031ACPZ-5-R7](#) [L9788TR](#)  
[STPMIC1APQR](#) [STPMIC1BPQR](#)