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April 1st, 2010
Renesas Electronics Corporation

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Rev.1.10
Nov. 01, 2005

1. Overview

The M32C/80 Group microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/80 Group is available in 100-pin plastic molded LQFP/QFP package.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

The M32C/80 Group is ROMless device.
Use the M32C/80 Group in microprocessor mode after reset.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Table 1.1 lists performance overview of the M32C/80 Group.

Table 1.1 M32C/80 Group Performance

Item		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, V_{CC1}=4.2 to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, V_{CC1}=3.0 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode, Microprocessor mode
	Memory Space	16 Mbytes
	Memory Capacity	See Table 1.2
Peripheral function	I/O Port	47 I/O pins (when using 16-bit bus) and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O Communication Function	2 channels
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus(1), I^2C Bus(2)
	A/D Converter	10-bit A/D converter: 1 circuit, 10 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, operation and chain transfer function
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	34 internal sources and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main Clock oscillation circuit (*), Sub clock oscillation circuit (*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor
	Oscillation Stop Detect Function	Main clock oscillation stop detect circuit
Electrical Charact-eristics	Supply Voltage	V_{CC1}=4.2 to 5.5 V, V_{CC2}=3.0 to V_{CC1} (f(BCLK)=32 MHz) V_{CC1}=3.0 to 5.5 V, V_{CC2}=3.0 to V_{CC1} (f(BCLK)=24 MHz)
	Power Consumption	22 mA (V_{CC1}=V_{CC2}=5 V, f(BCLK)=32 MHz) 17 mA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=24 MHz) 10 µA (V_{CC1}=V_{CC2}=3.3 V, f(BCLK)=32 kHz, in wait mode)
Operating AmbientTemperature		–20 to 85°C, –40 to 85°C(optional)
Package		100-pin plastic molded LQFP/QFP

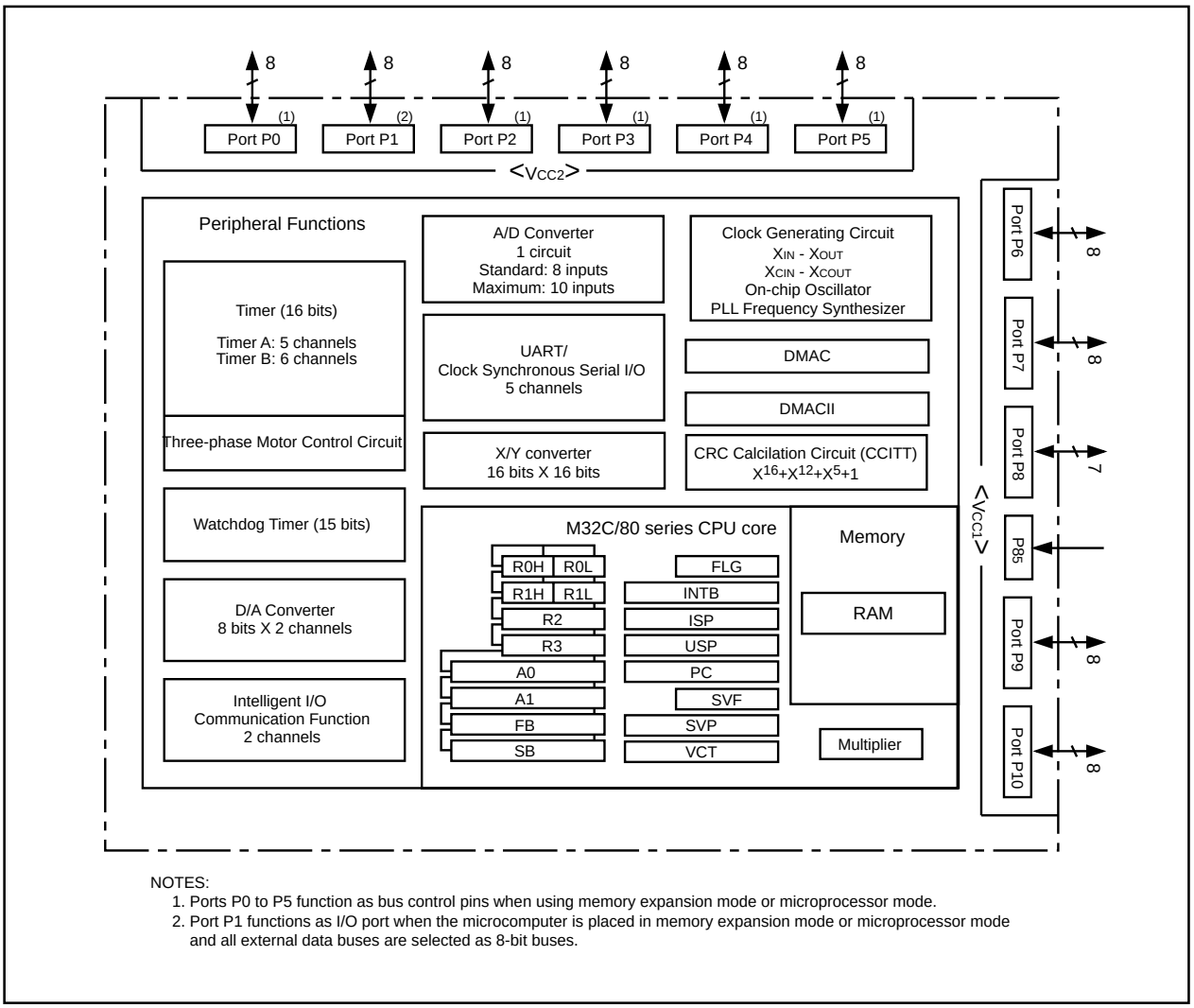
NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I^2C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/80 Group microcomputer.



NOTES:
1. Ports P0 to P5 function as bus control pins when using memory expansion mode or microprocessor mode.
2. Port P1 functions as I/O port when the microcomputer is placed in memory expansion mode or microprocessor mode and all external data buses are selected as 8-bit buses.

Figure 1.1 M32C/80 Group Block Diagram

1.4 Product Information

Table 1.2 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.2 M32C/80 Group **As of November, 2005**

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30800SAGP	PLQP0100KB-A (100P6Q-A)	–	8K	ROMless
M30800SAFP	PRQP0100JB-A (100P6S-A)			
M30800SAGP-BL	PLQP0100KB-A (100P6Q-A)			ROMless with on-chip boot loader
M30800SAFP-BL	PRQP0100JB-A (100P6S-A)			

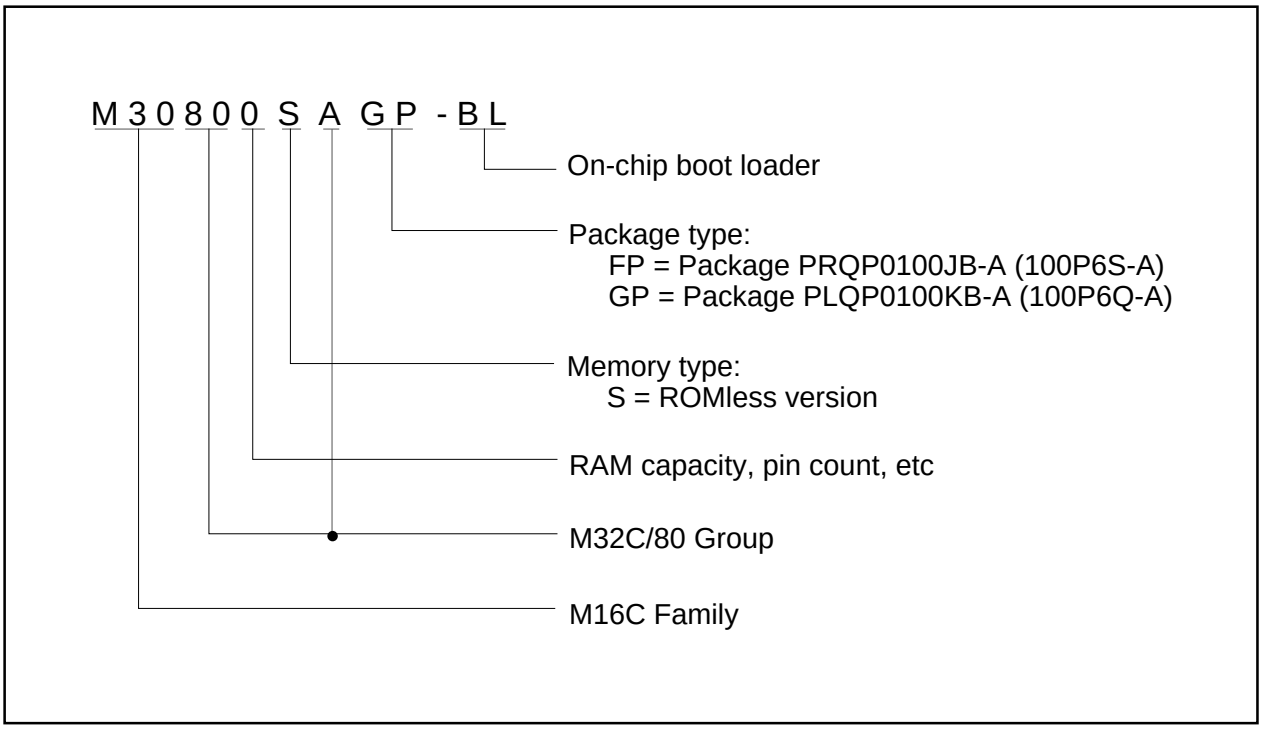
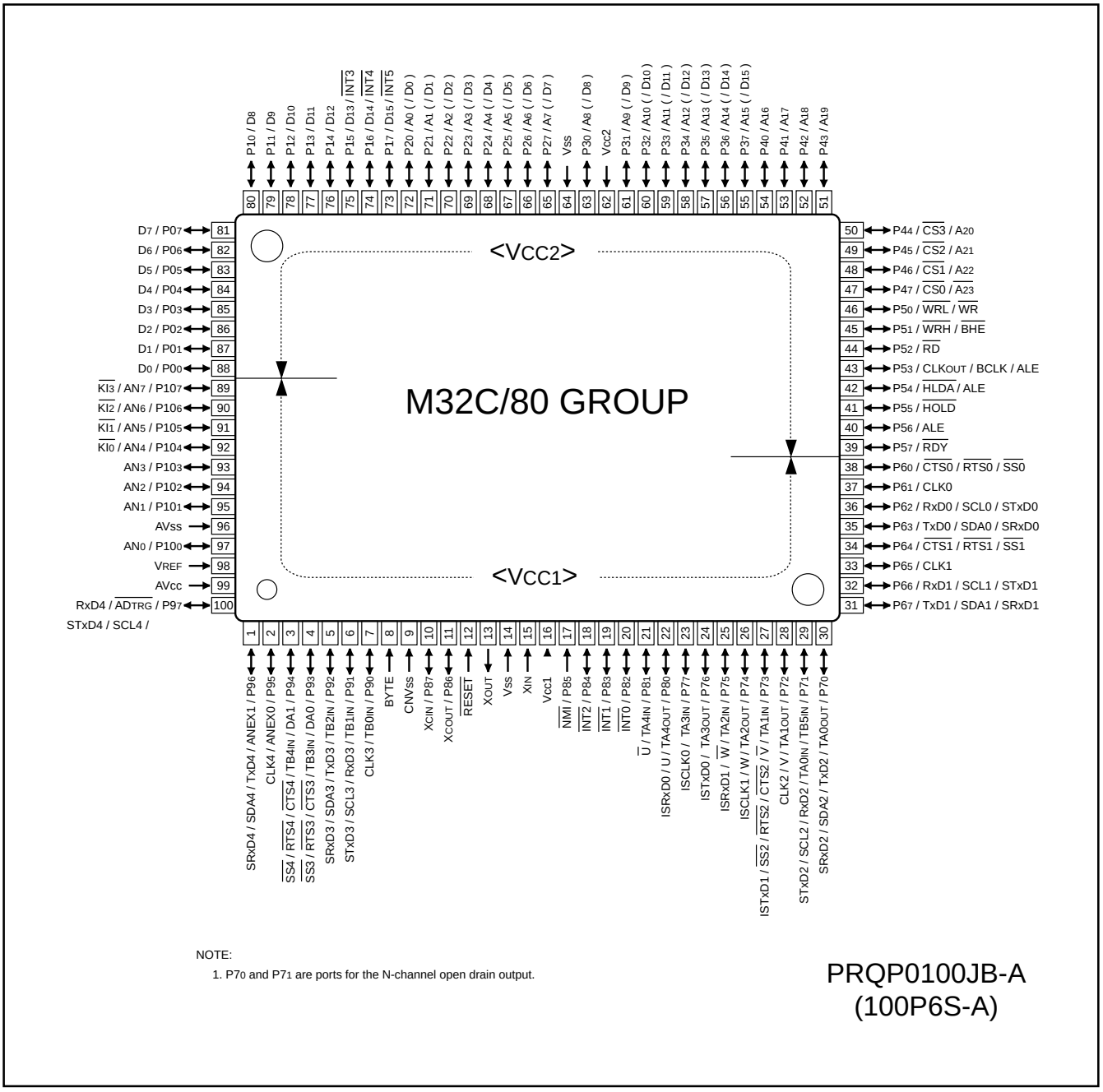


Figure 1.2 Product Numbering System

1.5 Pin Assignment

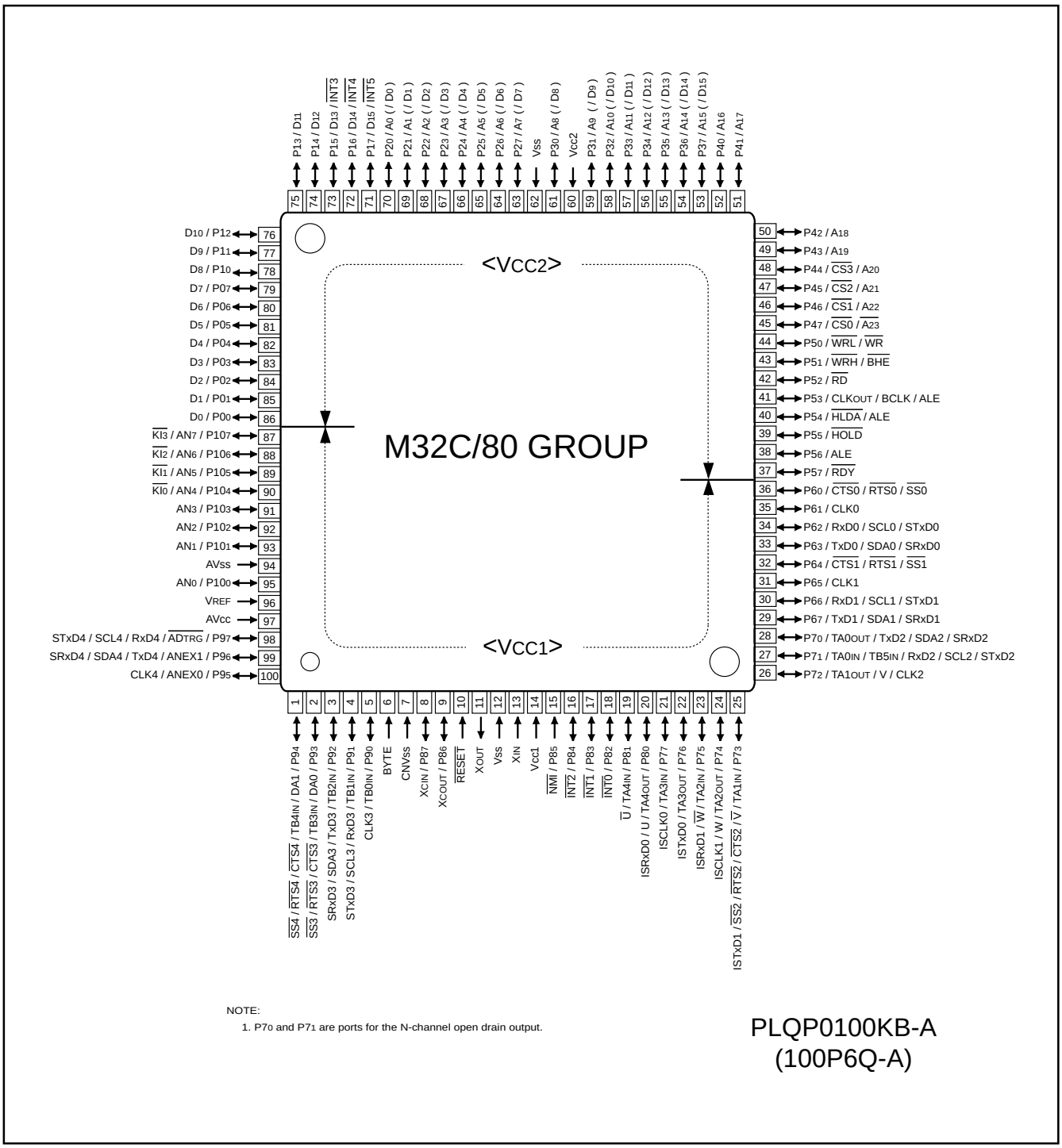
Figures 1.3 and 1.4 show pin assignments (top view).



NOTE:
1. P70 and P71 are ports for the N-channel open drain output.

PRQP0100JB-A
(100P6S-A)

Figure 1.3 Pin Assignment



NOTE:
1. P70 and P71 are ports for the N-channel open drain output.

PLQP0100KB-A
(100P6Q-A)

Figure 1.4 Pin Assignment

Table 1.3 Pin Characteristics

Package Pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	Intelligent I/O pins
FP	GP								
1	99		P9$_6$			TxD4/SDA4/SRxD4	ANEX1		
2	100		P9$_5$			CLK4	ANEX0		
3	1		P9$_4$		TB4$_{IN}$	$\overline{CTS4}$/$\overline{RTS4}$/$\overline{SS4}$	DA1		
4	2		P9$_3$		TB3$_{IN}$	$\overline{CTS3}$/$\overline{RTS3}$/$\overline{SS3}$	DA0		
5	3		P9$_2$		TB2$_{IN}$	TxD3/SDA3/SRxD3			
6	4		P9$_1$		TB1$_{IN}$	RxD3/SCL3/STxD3			
7	5		P9$_0$		TB0$_{IN}$	CLK3			
8	6	BYTE							
9	7	CNV$_{SS}$							
10	8	X$_{CIN}$	P8$_7$						
11	9	X$_{COUT}$	P8$_6$						
12	10	$\overline{RESET}$							
13	11	X$_{OUT}$							
14	12	V$_{SS}$							
15	13	X$_{IN}$							
16	14	V$_{CC1}$							
17	15		P8$_5$	$\overline{NMI}$					
18	16		P8$_4$	$\overline{INT2}$					
19	17		P8$_3$	$\overline{INT1}$					
20	18		P8$_2$	$\overline{INT0}$					
21	19		P8$_1$		TA4$_{IN}$/$\overline{U}$				
22	20		P8$_0$		TA4$_{OUT}$/U				ISRxD0
23	21		P7$_7$		TA3$_{IN}$				ISCLK0
24	22		P7$_6$		TA3$_{OUT}$				ISTxD0
25	23		P7$_5$		TA2$_{IN}$/$\overline{W}$				ISRxD1
26	24		P7$_4$		TA2$_{OUT}$/W				ISCLK1
27	25		P7$_3$		TA1$_{IN}$/$\overline{V}$	$\overline{CTS2}$/$\overline{RTS2}$/$\overline{SS2}$			ISTxD1
28	26		P7$_2$		TA1$_{OUT}$/V	CLK2			
29	27		P7$_1$		TB5$_{IN}$/TA0$_{IN}$	RxD2/SCL2/STxD2			
30	28		P7$_0$		TA0$_{OUT}$	TxD2/SDA2/SRxD2			
31	29		P6$_7$			TxD1/SDA1/SRxD1			
32	30		P6$_6$			RxD1/SCL1/STxD1			
33	31		P6$_5$			CLK1			
34	32		P6$_4$			$\overline{CTS1}$/$\overline{RTS1}$/$\overline{SS1}$			
35	33		P6$_3$			TxD0/SDA0/SRxD0			
36	34		P6$_2$			RxD0/SCL0/STxD0			
37	35		P6$_1$			CLK0			
38	36		P6$_0$			$\overline{CTS0}$/$\overline{RTS0}$/$\overline{SS0}$			
39	37		P5$_7$					$\overline{RDY}$	
40	38		P5$_6$					ALE	
41	39		P5$_5$					$\overline{HOLD}$	
42	40		P5$_4$					$\overline{HLDA}$/ALE	
43	41		P5$_3$					CLK$_{OUT}$/BCLK/ALE	
44	42		P5$_2$					$\overline{RD}$	
45	43		P5$_1$					$\overline{WRH}$/$\overline{BHE}$	
46	44		P5$_0$					$\overline{WRL}$/$\overline{WR}$	
47	45		P4$_7$					$\overline{CS0}$/A$_{23}$	
48	46		P4$_6$					$\overline{CS1}$/A$_{22}$	
49	47		P4$_5$					$\overline{CS2}$/A$_{21}$	
50	48		P4$_4$					$\overline{CS3}$/A$_{20}$	

Table 1.3 Pin Characteristics (Continued)

Package pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	Intelligent I/O pins
FP	GP								
51	49		$P4_3$					A_{19}	
52	50		$P4_2$					A_{18}	
53	51		$P4_1$					A_{17}	
54	52		$P4_0$					A_{16}	
55	53		$P3_7$					A_{15}(/D_{15})	
56	54		$P3_6$					A_{14}(/D_{14})	
57	55		$P3_5$					A_{13}(/D_{13})	
58	56		$P3_4$					A_{12}(/D_{12})	
59	57		$P3_3$					A_{11}(/D_{11})	
60	58		$P3_2$					A_{10}(/D_{10})	
61	59		$P3_1$					A_9(/D_9)	
62	60	V_{CC2}							
63	61		$P3_0$					A_8(/D_8)	
64	62	V_{SS}							
65	63		$P2_7$					A_7(/D_7)	
66	64		$P2_6$					A_6(/D_6)	
67	65		$P2_5$					A_5(/D_5)	
68	66		$P2_4$					A_4(/D_4)	
69	67		$P2_3$					A_3(/D_3)	
70	68		$P2_2$					A_2(/D_2)	
71	69		$P2_1$					A_1(/D_1)	
72	70		$P2_0$					A_0(/D_0)	
73	71		$P1_7$	$\overline{INT5}$				D_{15}	
74	72		$P1_6$	$\overline{INT4}$				D_{14}	
75	73		$P1_5$	$\overline{INT3}$				D_{13}	
76	74		$P1_4$					D_{12}	
77	75		$P1_3$					D_{11}	
78	76		$P1_2$					D_{10}	
79	77		$P1_1$					D_9	
80	78		$P1_0$					D_8	
81	79		$P0_7$					D_7	
82	80		$P0_6$					D_6	
83	81		$P0_5$					D_5	
84	82		$P0_4$					D_4	
85	83		$P0_3$					D_3	
86	84		$P0_2$					D_2	
87	85		$P0_1$					D_1	
88	86		$P0_0$					D_0	
89	87		$P10_7$	$\overline{KI_3}$			AN_7		
90	88		$P10_6$	$\overline{KI_2}$			AN_6		
91	89		$P10_5$	$\overline{KI_1}$			AN_5		
92	90		$P10_4$	$\overline{KI_0}$			AN_4		
93	91		$P10_3$				AN_3		
94	92		$P10_2$				AN_2		
95	93		$P10_1$				AN_1		
96	94	AV_{SS}							
97	95		$P10_0$				AN_0		
98	96						V_{REF}		
99	97	AV_{CC}							
100	98		$P9_7$			RxD4/SCL4/STxD4	$\overline{ADTRG}$		

1.6 Pin Description

Table 1.4 Pin Description

Signal name	Pin name	I/O type	Supply voltage	Description
Power supply	V_{CC1}, V_{CC2} V_{SS}	I	-	Apply 3.0 to 5.5 V to both V_{CC1} and V_{CC2} pins. Apply 0 V to the V_{SS} pin. $V_{CC1} \geq V_{CC2}$(1)
Analog power supply input	AVCC AVSS	I	V_{CC1}	Supplies power for the A/D converter. Connect the AVCC pin to V_{CC1} and the AVSS pin to V_{SS}
Reset input	$\overline{RESET}$	I	V_{CC1}	The microcomputer is in a reset state when "L" is applied to the $\overline{RESET}$ pin
CNVSS	CNVSS	I	V_{CC1}	Connect this pin to V_{CC1}
External data bus width select input	BYTE	I	V_{CC1}	Switches the data bus in external memory space 3. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one.
Bus control pins	D_0 to D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) while accessing an external memory space with separate bus
	D_8 to D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) while accessing an external memory space with 16-bit separate bus
	A_0 to A_{22}	O	V_{CC2}	Outputs address bits (A_0 to A_{22})
	$\overline{A23}$	O	V_{CC2}	Outputs inversed address bit A23
	A_0/D_0 to A_7/D_7	I/O	V_{CC2}	Inputs and outputs data (D_0 to D_7) and outputs 8 low-order address bits (A_0 to A_7) by time-sharing while accessing an external memory space with multiplexed bus
	A_8/D_8 to A_{15}/D_{15}	I/O	V_{CC2}	Inputs and outputs data (D_8 to D_{15}) and outputs 8 middle-order address bits (A_8 to A_{15}) by time-sharing while accessing an external memory space with multiplexed bus
	$\overline{CS0}$ to $\overline{CS3}$	O	V_{CC2}	Output $\overline{CS0}$ to $\overline{CS3}$ that are chip-select signals specifying an external space
	$\overline{WRL}/\overline{WR}$ $\overline{WRH}/\overline{BHE}$ $\overline{RD}$	O	V_{CC2}	Outputs $\overline{WRL}$, $\overline{WRH}$, ($\overline{WR}$, $\overline{BHE}$) and $\overline{RD}$ signals. $\overline{WRL}$ and $\overline{WRH}$ can be switched with $\overline{WR}$ and $\overline{BHE}$ by program ■ $\overline{WRL}$, $\overline{WRH}$ and $\overline{RD}$ are selected: If external data bus is 16 bits wide, data is writtenn to an even address when $\overline{WRL}$ is held "L". Data is written to an odd address when $\overline{WRH}$ is held "L". Data is read when $\overline{RD}$ is held "L". ■ $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ are selected Data is written to external memory space when $\overline{WR}$ is held "L". Data is read when $\overline{RD}$ is held "L". An odd address is accessed when $\overline{BHE}$ is held "L". Select $\overline{WR}$, $\overline{BHE}$ and $\overline{RD}$ for an external 8-bit data bus
	ALE	O	V_{CC2}	ALE is a signal latching address
	$\overline{HOLD}$	I	V_{CC2}	The microcomputer is placed in a hold state while the $\overline{HOLD}$ pin is held "L"
	$\overline{HLDA}$	O	V_{CC2}	Outputs an "L" siganl while the microcomputer is placed in a hold state
	$\overline{RDY}$	I	V_{CC2}	Bus is placed in a wait state while the RDY pin is held "L"

I: Input O: Output I/O: Input and output

NOTE:

1. In this manual, hereafter, V_{CC} refers to V_{CC1} unless otherwise noted.

Table 1.4 Pin Description (Continued)

Signal name	Pin name	I/O type	Supply voltage	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, input the clock from XIN and leave XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, input the clock from XCIN and leave XCOUT open
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs BCLK signal
Clock output	CLKOUT	O	VCC2	Outputs clock having thesame frequency as fC, f8, or f32
$\overline{INT}$ interrupt input	$\overline{INT0}$ to $\overline{INT2}$	I	VCC1	Input pins for the $\overline{INT}$ interrupt
	$\overline{INT3}$ to $\overline{INT5}$		VCC2	
$\overline{NMI}$ interrupt input	$\overline{NMI}$	I	VCC1	Input pin for the $\overline{NMI}$ interrupt
Key input interrupt	$\overline{KI0}$ to $\overline{KI3}$	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase motor control output	U, $\overline{U}$, V, $\overline{V}$, W, $\overline{W}$	O	VCC1	output pins for the three-phase motor control timer
Serial I/O	$\overline{CTS0}$ to $\overline{CTS4}$	I	VCC1	Input pins for data transmission control
	$\overline{RTS0}$ to $\overline{RTS4}$	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I^2C mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O special function	STxD0 to STxD4	I	VCC1	Outputs serial data when slave mode is selected (SDA2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	Inputs serial data when slave mode is selected
	$\overline{SS0}$ to $\overline{SS4}$	I	VCC1	Input pins to control serial I/O special function

I: Input O: Output I/O: Input and output

Table 1.5 Pin Description (Continued)

Signal name	Pin name	I/O type	Supply voltage	Description
Reference voltage input	V_{REF}	I	-	Applies reference voltage for the A/D converter and D/A converter
A/D converter	AN_0 to AN_7	I	V_{CC1}	Analog input pins for the A/D converter
	$\overline{ADTRG}$	I	V_{CC1}	Input pin for an external A/D trigger
	ANEX0	I/O	V_{CC1}	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	V_{CC1}	Extended analog input pin for the A/D converter
D/A converter	DA0, DA1	O	V_{CC1}	Output pin for the D/A converter
Intelligent I/O communication function	ISCLK0	I/O	V_{CC1}	Inputs and outputs clock for the intelligent I/O communication fucntion
	ISCLK1			
	ISTxD0	O	V_{CC1}	Outputs data for the intelligent I/O communication fucntion
	ISTxD1			
	ISRxD0	I	V_{CC1}	Inputs data for the intelligent I/O communication fucntion
	ISRxD1			
I/O port	$P0_0$ to $P0_7$(1) $P1_0$ to $P1_7$(2) $P2_0$ to $P2_7$(1) $P3_0$ to $P3_7$(1) $P4_0$ to $P4_7$(1) $P5_0$ to $P5_7$(1)	I/O	V_{CC2}	I/O ports fro CMOS. Each port can be programmed for nput or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	$P6_0$ to $P6_7$ $P7_0$ to $P7_7$ $P9_0$ to $P9_7$ $P10_0$ to $P10_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0 ($P7_0$ and $P7_1$ are ports for the N-channel open drain output.)
	$P8_0$ to $P8_4$, $P8_6$, $P8_7$	I/O	V_{CC1}	I/O ports having equivalent functions to P0
	$P8_5$	I	V_{CC1}	Shares a pin with $\overline{NMI}$. $\overline{NMI}$ input state can be got by reading $P8_5$

I: Input O: Output I/O: Input and output

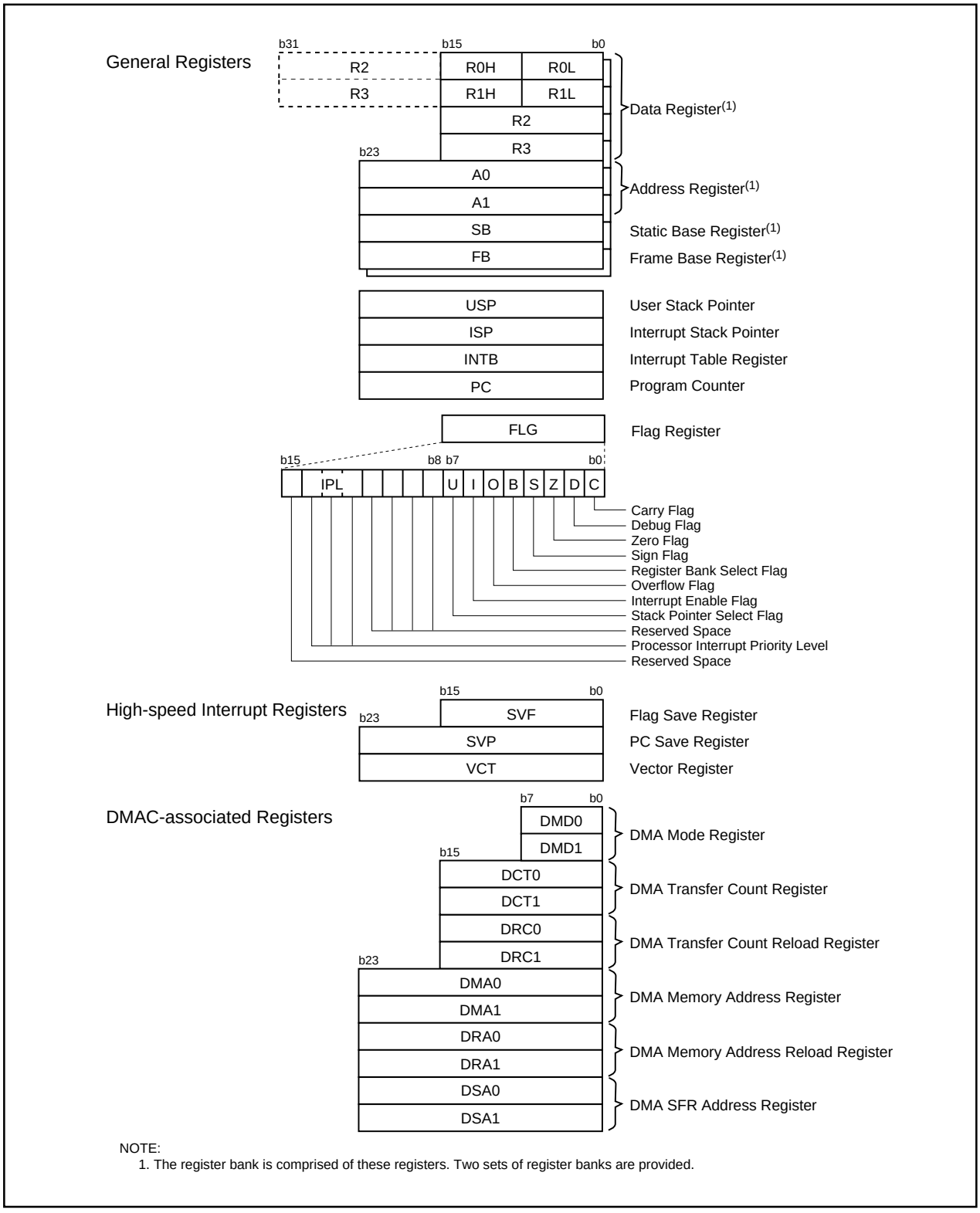
NOTES:

1. Ports P0 to P5 function as bus control pins when using memory expansion mode or microprocessor mode. They cannot be used as I/O ports.
2. Port P1 functions as I/O port when the microcomputer is placed in memory expansion mode or microprocessor mode and all external data buses are selected as 8-bit buses.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.



NOTE:
1. The register bank is comprised of these registers. Two sets of register banks are provided.

Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.
Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".
The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/80 Group.

The M32C/80 Group provides 16-Mbyte address space addressed from 000000$_{16}$ to FFFFFF$_{16}$.

The fixed interrupt vectors are allocated from address FFFFDC$_{16}$ to FFFFFF$_{16}$. It stores the starting address of each interrupt routine.

The internal RAM is allocated from address 000400$_{16}$ to higher. For example, a 8-Kbyte internal RAM is allocated from address 000400$_{16}$ to 0023FF$_{16}$. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFRs, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers, is allocated from address 000000$_{16}$ to 0003FF$_{16}$. All blank spaces within SFRs are reserved and cannot be accessed by users.

The special page vector table is addressed from FFFE00$_{16}$ to FFFFDB$_{16}$. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details.

In microprocessor mode, some spaces are reserved and cannot be accessed by users.

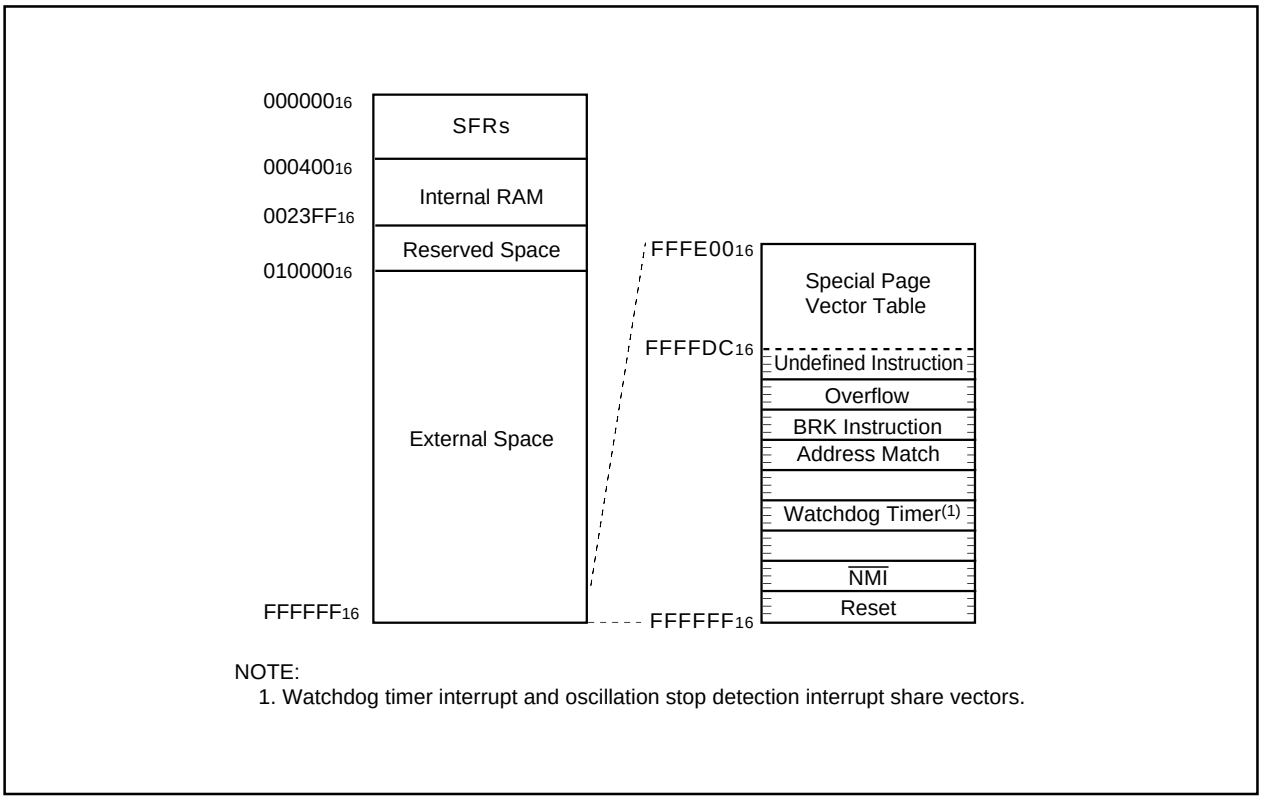


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
000016			
000116			
000216			
000316			
000416	Processor Mode Register(1)	PM0	0000 00112(CNVss pin ="H")
000516	Processor Mode Register 1	PM1	0016
000616	System Clock Control Register 0	CM0	0000 10002
000716	System Clock Control Register 1	CM1	0010 00002
000816			
000916	Address Match Interrupt Enable Register	AIER	0016
000A16	Protect Register	PRCR	XXXX 00002
000B16	External Data Bus Width Control Register	DS	XXXX 10002(BYTE pin ="L") XXXX 00002(BYTE pin ="H")
000C16	Main Clock Division Register	MCD	XXX0 10002
000D16	Oscillation Stop Detection Register	CM2	0016
000E16	Watchdog Timer Start Register	WDTS	XX16
000F16	Watchdog Timer Control Register	WDC	000X XXXX2
001016 001116 001216	Address Match Interrupt Register 0	RMAD0	00000016
001316	Processor Mode Register 2	PM2	0016
001416 001516 001616	Address Match Interrupt Register 1	RMAD1	00000016
001716			
001816 001916 001A16	Address Match Interrupt Register 2	RMAD2	00000016
001B16			
001C16 001D16 001E16	Address Match Interrupt Register 3	RMAD3	00000016
001F16			
002016			
002116			
002216			
002316			
002416			
002516			
002616	PLL Control Register 0	PLC0	0001 X0102
002716	PLL Control Register 1	PLC1	000X 00002
002816 002916 002A16	Address Match Interrupt Register 4	RMAD4	00000016
002B16			
002C16 002D16 002E16	Address Match Interrupt Register 5	RMAD5	00000016
002F16			

X: Indeterminate
Blank spaces are reserved. No access is allowed.
NOTE:
1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0030₁₆			
0031₁₆			
0032₁₆			
0033₁₆			
0034₁₆			
0035₁₆			
0036₁₆			
0037₁₆			
0038₁₆ 0039₁₆ 003A₁₆	Address Match Interrupt Register 6	RMAD6	000000₁₆
003B₁₆			
003C₁₆ 003D₁₆ 003E₁₆	Address Match Interrupt Register 7	RMAD7	000000₁₆
003F₁₆			
0040₁₆			
0041₁₆			
0042₁₆			
0043₁₆			
0044₁₆			
0045₁₆			
0046₁₆			
0047₁₆			
0048₁₆	External Space Wait Control Register 0	EWCR0	X0X0 0011₂
0049₁₆	External Space Wait Control Register 1	EWCR1	X0X0 0011₂
004A₁₆	External Space Wait Control Register 2	EWCR2	X0X0 0011₂
004B₁₆	External Space Wait Control Register 3	EWCR3	X0X0 0011₂
004C₁₆			
004D₁₆			
004E₁₆			
004F₁₆			
0050₁₆			
0051₁₆			
0052₁₆			
0053₁₆			
0054₁₆			
0055₁₆			
0056₁₆			
0057₁₆			
0058₁₆			
0059₁₆			
005A₁₆			
005B₁₆			
005C₁₆			
005D₁₆			
005E₁₆			
005F₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
006016			
006116			
006216			
006316			
006416			
006516			
006616			
006716			
006816	DMA0 Interrupt Control Register	DM0IC	XXXX X0002
006916	Timer B5 Interrupt Control Register	TB5IC	XXXX X0002
006A16	DMA2 Interrupt Control Register	DM2IC	XXXX X0002
006B16	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X0002
006C16	Timer A0 Interrupt Control Register	TA0IC	XXXX X0002
006D16	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X0002
006E16	Timer A2 Interrupt Control Register	TA2IC	XXXX X0002
006F16	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X0002
007016	Timer A4 Interrupt Control Register	TA4IC	XXXX X0002
007116	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X0002
007216	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X0002
007316	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X0002
007416	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X0002
007516	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X0002
007616	Timer B1 Interrupt Control Register	TB1IC	XXXX X0002
007716	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X0002
007816	Timer B3 Interrupt Control Register	TB3IC	XXXX X0002
007916	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X0002
007A16	INT5 Interrupt Control Register	INT5IC	XX00 X0002
007B16			
007C16	INT3 Interrupt Control Register	INT3IC	XX00 X0002
007D16			
007E16	INT1 Interrupt Control Register	INT1IC	XX00 X0002
007F16			
008016			
008116			
008216			
008316			
008416			
008516			
008616			
008716			
008816	DMA1 Interrupt Control Register	DM1IC	XXXX X0002
008916	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X0002
008A16	DMA3 Interrupt Control Register	DM3IC	XXXX X0002
008B16	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X0002
008C16	Timer A1 Interrupt Control Register	TA1IC	XXXX X0002
008D16	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X0002
008E16	Timer A3 Interrupt Control Register	TA3IC	XXXX X0002
008F16	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X0002

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
009016	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X0002
009116	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X0002
009216	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X0002
009316	Key Input Interrupt Control Register	KUPIC	XXXX X0002
009416	Timer B0 Interrupt Control Register	TB0IC	XXXX X0002
009516	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X0002
009616	Timer B2 Interrupt Control Register	TB2IC	XXXX X0002
009716	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X0002
009816	Timer B4 Interrupt Control Register	TB4IC	XXXX X0002
009916			
009A16	INT4 Interrupt Control Register	INT4IC	XX00 X0002
009B16			
009C16	INT2 Interrupt Control Register	INT2IC	XX00 X0002
009D16			
009E16	INT0 Interrupt Control Register	INT0IC	XX00 X0002
009F16	Exit Priority Control Register	RLVL	XXXX 00002
00A016	Interrupt Request Register 0	IIO0IR	0000 000X2
00A116	Interrupt Request Register 1	IIO1IR	0000 000X2
00A216	Interrupt Request Register 2	IIO2IR	0000 000X2
00A316	Interrupt Request Register 3	IIO3IR	0000 000X2
00A416	Interrupt Request Register 4	IIO4IR	0000 000X2
00A516			
00A616			
00A716			
00A816			
00A916			
00AA16			
00AB16			
00AC16			
00AD16			
00AE16			
00AF16			
00B016	Interrupt Enable Register 0	IIO0IE	0016
00B116	Interrupt Enable Register 1	IIO1IE	0016
00B216	Interrupt Enable Register 2	IIO2IE	0016
00B316	Interrupt Enable Register 3	IIO3IE	0016
00B416	Interrupt Enable Register 4	IIO4IE	0016
00B516			
00B616			
00B716			
00B816			
00B916			
00BA16			
00BB16			
00BC16			
00BD16			
00BE16			
00BF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0$_{16}$			
00C1$_{16}$			
00C2$_{16}$			
00C3$_{16}$			
00C4$_{16}$			
00C5$_{16}$			
00C6$_{16}$			
00C7$_{16}$			
00C8$_{16}$			
00C9$_{16}$			
00CA$_{16}$			
00CB$_{16}$			
00CC$_{16}$			
00CD$_{16}$			
00CE$_{16}$			
00CF$_{16}$			
00D0$_{16}$			
00D1$_{16}$			
00D2$_{16}$			
00D3$_{16}$			
00D4$_{16}$			
00D5$_{16}$			
00D6$_{16}$			
00D7$_{16}$			
00D8$_{16}$			
00D9$_{16}$			
00DA$_{16}$			
00DB$_{16}$			
00DC$_{16}$			
00DD$_{16}$			
00DE$_{16}$			
00DF$_{16}$			
00E0$_{16}$			
00E1$_{16}$			
00E2$_{16}$			
00E3$_{16}$			
00E4$_{16}$			
00E5$_{16}$			
00E6$_{16}$			
00E7$_{16}$			
00E8$_{16}$ 00E9$_{16}$	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX$_2$ XXX0 XXXX$_2$
00EA$_{16}$	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX$_{16}$
00EB$_{16}$			
00EC$_{16}$	Receive Input Register 0	G0RI	XX$_{16}$
00ED$_{16}$	SI/O Communication Mode Register 0	G0MR	00$_{16}$
00EE$_{16}$	Transmit Output Register 0	G0TO	XX$_{16}$
00EF$_{16}$	SI/O Communication Control Register 0	G0CR	0000 X011$_2$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00F0$_{16}$	Data Compare Register 00	G0CMP0	XX$_{16}$
00F1$_{16}$	Data Compare Register 01	G0CMP1	XX$_{16}$
00F2$_{16}$	Data Compare Register 02	G0CMP2	XX$_{16}$
00F3$_{16}$	Data Compare Register 03	G0CMP3	XX$_{16}$
00F4$_{16}$	Data Mask Register 00	G0MSK0	XX$_{16}$
00F5$_{16}$	Data Mask Register 01	G0MSK1	XX$_{16}$
00F6$_{16}$	Communication Clock Select Register	CCS	XXXX 0000$_2$
00F7$_{16}$			
00F8$_{16}$ 00F9$_{16}$	Receive CRC Code Register 0	G0RCRC	XX$_{16}$ XX$_{16}$
00FA$_{16}$ 00FB$_{16}$	Transmit CRC Code Register 0	G0TCRC	00$_{16}$ 00$_{16}$
00FC$_{16}$	SI/O Expansion Mode Register 0	G0EMR	00$_{16}$
00FD$_{16}$	SI/O Expansion Receive Control Register 0	G0ERC	00$_{16}$
00FE$_{16}$	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00$_{16}$
00FF$_{16}$	SI/O Expansion Transmit Control Register 0	G0ETC	0000 0XXX$_2$
0100$_{16}$			
0101$_{16}$			
0102$_{16}$			
0103$_{16}$			
0104$_{16}$			
0105$_{16}$			
0106$_{16}$			
0107$_{16}$			
0108$_{16}$			
0109$_{16}$			
010A$_{16}$			
010B$_{16}$			
010C$_{16}$			
010D$_{16}$			
010E$_{16}$			
010F$_{16}$			
0110$_{16}$			
0111$_{16}$			
0112$_{16}$			
0113$_{16}$			
0114$_{16}$			
0115$_{16}$			
0116$_{16}$			
0117$_{16}$			
0118$_{16}$			
0119$_{16}$			
011A$_{16}$			
011B$_{16}$			
011C$_{16}$			
011D$_{16}$			
011E$_{16}$			
011F$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
012016 012116			
012216			
012316			
012416			
012516			
012616			
012716			
012816 012916	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX2 XXX0 XXXX2
012A16	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX16
012B16			
012C16	Receive Input Register 1	G1RI	XX16
012D16	SI/O Communication Mode Register 1	G1MR	0016
012E16	Transmit Output Register 1	G1TO	XX16
012F16	SI/O Communication Control Register 1	G1CR	0000 X0112
013016	Data Compare Register 10	G1CMP0	XX16
013116	Data Compare Register 11	G1CMP1	XX16
013216	Data Compare Register 12	G1CMP2	XX16
013316	Data Compare Register 13	G1CMP3	XX16
013416	Data Mask Register 10	G1MSK0	XX16
013516	Data Mask Register 11	G1MSK1	XX16
013616			
013716			
013816 013916	Receive CRC Code Register 1	G1RCRC	XX16 XX16
013A16 013B16	Transmit CRC Code Register 1	G1TCRC	0016 0016
013C16	SI/O Expansion Mode Register 1	G1EMR	0016
013D16	SI/O Expansion Receive Control Register 1	G1ERC	0016
013E16	SI/O Special Communication Interrupt Detection Register 1	G1IRF	0016
013F16	SI/O Expansion Transmit Control Register 1	G1ETC	0000 0XXX2
014016			
014116			
014216			
014316			
014416			
014516			
014616			
014716			
014816			
014916			
014A16			
014B16			
014C16			
014D16 to 02AF16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02B116			
02B216			
02B316			
02B416			
02B516			
02B616			
02B716			
02B816			
02B916			
02BA16			
02BB16			
02BC16			
02BD16			
02BE16			
02BF16			
02C016 02C116	X0 Register Y0 Register	X0R,Y0R	XX16 XX16
02C216 02C316	X1 Register Y1 Register	X1R,Y1R	XX16 XX16
02C416 02C516	X2 Register Y2 Register	X2R,Y2R	XX16 XX16
02C616 02C716	X3 Register Y3 Register	X3R,Y3R	XX16 XX16
02C816 02C916	X4 Register Y4 Register	X4R,Y4R	XX16 XX16
02CA16 02CB16	X5 Register Y5 Register	X5R,Y5R	XX16 XX16
02CC16 02CD16	X6 Register Y6 Register	X6R,Y6R	XX16 XX16
02CE16 02CF16	X7 Register Y7 Register	X7R,Y7R	XX16 XX16
02D016 02D116	X8 Register Y8 Register	X8R,Y8R	XX16 XX16
02D216 02D316	X9 Register Y9 Register	X9R,Y9R	XX16 XX16
02D416 02D516	X10 Register Y10 Register	X10R,Y10R	XX16 XX16
02D616 02D716	X11 Register Y11 Register	X11R,Y11R	XX16 XX16
02D816 02D916	X12 Register Y12 Register	X12R,Y12R	XX16 XX16
02DA16 02DB16	X13 Register Y13 Register	X13R,Y13R	XX16 XX16
02DC16 02DD16	X14 Register Y14 Register	X14R,Y14R	XX16 XX16
02DE16 02DF16	X15 Register Y15 Register	X15R,Y15R	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02E016	X/Y Control Register	XYC	XXXX XX002
02E116			
02E216			
02E316			
02E416	UART1 Special Mode Register 4	U1SMR4	0016
02E516	UART1 Special Mode Register 3	U1SMR3	0016
02E616	UART1 Special Mode Register 2	U1SMR2	0016
02E716	UART1 Special Mode Register	U1SMR	0016
02E816	UART1 Transmit/Receive Mode Register	U1MR	0016
02E916	UART1 Bit Rate Register	U1BRG	XX16
02EA16	UART1 Transmit Buffer Register	U1TB	XX16
02EB16			XX16
02EC16	UART1 Transmit/Receive Control Register 0	U1C0	0000 10002
02ED16	UART1 Transmit/Receive Control Register 1	U1C1	0000 00102
02EE16	UART1 Receive Buffer Register	U1RB	XX16
02EF16			XX16
02F016			
02F116			
02F216			
02F316			
02F416	UART4 Special Mode Register 4	U4SMR4	0016
02F516	UART4 Special Mode Register 3	U4SMR3	0016
02F616	UART4 Special Mode Register 2	U4SMR2	0016
02F716	UART4 Special Mode Register	U4SMR	0016
02F816	UART4 Transmit/Receive Mode Register	U4MR	0016
02F916	UART4 Bit Rate Register	U4BRG	XX16
02FA16	UART4 Transmit Buffer Register	U4TB	XX16
02FB16			XX16
02FC16	UART4 Transmit/Receive Control Register 0	U4C0	0000 10002
02FD16	UART4 Transmit/Receive Control Register 1	U4C1	0000 00102
02FE16	UART4 Receive Buffer Register	U4RB	XX16
02FF16			XX16
030016	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX2
030116			
030216	Timer A1-1 Register	TA11	XX16
030316			XX16
030416	Timer A2-1 Register	TA21	XX16
030516			XX16
030616	Timer A4-1 Register	TA41	XX16
030716			XX16
030816	Three-Phase PWM Control Register 0	INVC0	0016
030916	Three-Phase PWM Control Register 1	INVC1	0016
030A16	Three-Phase Output Buffer Register 0	IDB0	XX11 11112
030B16	Three-Phase Output Buffer Register 1	IDB1	XX11 11112
030C16	Dead Time Timer	DTT	XX16
030D16	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX16
030E16			
030F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0310$_{16}$	Timer B3 Register	TB3	XX$_{16}$
0311$_{16}$			XX$_{16}$
0312$_{16}$	Timer B4 Register	TB4	XX$_{16}$
0313$_{16}$			XX$_{16}$
0314$_{16}$	Timer B5 Register	TB5	XX$_{16}$
0315$_{16}$			XX$_{16}$
0316$_{16}$			
0317$_{16}$			
0318$_{16}$			
0319$_{16}$			
031A$_{16}$			
031B$_{16}$	Timer B3 Mode Register	TB3MR	00XX 0000$_2$
031C$_{16}$	Timer B4 Mode Register	TB4MR	00XX 0000$_2$
031D$_{16}$	Timer B5 Mode Register	TB5MR	00XX 0000$_2$
031E$_{16}$			
031F$_{16}$	External Interrupt Request Source Select Register	IFSR	00$_{16}$
0320$_{16}$			
0321$_{16}$			
0322$_{16}$			
0323$_{16}$			
0324$_{16}$	UART3 Special Mode Register 4	U3SMR4	00$_{16}$
0325$_{16}$	UART3 Special Mode Register 3	U3SMR3	00$_{16}$
0326$_{16}$	UART3 Special Mode Register 2	U3SMR2	00$_{16}$
0327$_{16}$	UART3 Special Mode Register	U3SMR	00$_{16}$
0328$_{16}$	UART3 Transmit/Receive Mode Register	U3MR	00$_{16}$
0329$_{16}$	UART3 Bit Rate Register	U3BRG	XX$_{16}$
032A$_{16}$	UART3 Transmit Buffer Register	U3TB	XX$_{16}$
032B$_{16}$			XX$_{16}$
032C$_{16}$	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000$_2$
032D$_{16}$	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010$_2$
032E$_{16}$	UART3 Receive Buffer Register	U3RB	XX$_{16}$
032F$_{16}$			XX$_{16}$
0330$_{16}$			
0331$_{16}$			
0332$_{16}$			
0333$_{16}$			
0334$_{16}$	UART2 Special Mode Register 4	U2SMR4	00$_{16}$
0335$_{16}$	UART2 Special Mode Register 3	U2SMR3	00$_{16}$
0336$_{16}$	UART2 Special Mode Register 2	U2SMR2	00$_{16}$
0337$_{16}$	UART2 Special Mode Register	U2SMR	00$_{16}$
0338$_{16}$	UART2 Transmit/Receive Mode Register	U2MR	00$_{16}$
0339$_{16}$	UART2 Bit Rate Register	U2BRG	XX$_{16}$
033A$_{16}$	UART2 Transmit Buffer Register	U2TB	XX$_{16}$
033B$_{16}$			XX$_{16}$
033C$_{16}$	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000$_2$
033D$_{16}$	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010$_2$
033E$_{16}$	UART2 Receive Buffer Register	U2RB	XX$_{16}$
033F$_{16}$			XX$_{16}$

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
034016	Count Start Flag	TABSR	0016
034116	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX2
034216	One-Shot Start Flag	ONSF	0016
034316	Trigger Select Register	TRGSR	0016
034416	Up/Down Flag	UDF	0016
034516			
034616 034716	Timer A0 Register	TA0	XX16 XX16
034816 034916	Timer A1 Register	TA1	XX16 XX16
034A16 034B16	Timer A2 Register	TA2	XX16 XX16
034C16 034D16	Timer A3 Register	TA3	XX16 XX16
034E16 034F16	Timer A4 Register	TA4	XX16 XX16
035016 035116	Timer B0 Register	TB0	XX16 XX16
035216 035316	Timer B1 Register	TB1	XX16 XX16
035416 035516	Timer B2 Register	TB2	XX16 XX16
035616	Timer A0 Mode Register	TA0MR	0016
035716	Timer A1 Mode Register	TA1MR	0016
035816	Timer A2 Mode Register	TA2MR	0016
035916	Timer A3 Mode Register	TA3MR	0016
035A16	Timer A4 Mode Register	TA4MR	0016
035B16	Timer B0 Mode Register	TB0MR	00XX 00002
035C16	Timer B1 Mode Register	TB1MR	00XX 00002
035D16	Timer B2 Mode Register	TB2MR	00XX 00002
035E16	Timer B2 Special Mode Register	TB2SC	XXXX XXX02
035F16	Count Source Prescaler Register(1)	TCSPR	0XXX 00002
036016			
036116			
036216			
036316			
036416	UART0 Special Mode Register 4	U0SMR4	0016
036516	UART0 Special Mode Register 3	U0SMR3	0016
036616	UART0 Special Mode Register 2	U0SMR2	0016
036716	UART0 Special Mode Register	U0SMR	0016
036816	UART0 Transmit/Receive Mode Register	U0MR	0016
036916	UART0 Bit Rate Register	U0BRG	XX16
036A16 036B16	UART0 Transmit Buffer Register	U0TB	XX16 XX16
036C16	UART0 Transmit/Receive Control Register 0	U0C0	0000 10002
036D16	UART0 Transmit/Receive Control Register 1	U0C1	0000 00102
036E16 036F16	UART0 Receive Buffer Register	U0RB	XX16 XX16

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The TCSPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
037016			
037116			
037216			
037316			
037416			
037516			
037616			
037716			
037816	DMA0 Request Source Select Register	DM0SL	0X00 00002
037916	DMA1 Request Source Select Register	DM1SL	0X00 00002
037A16	DMA2 Request Source Select Register	DM2SL	0X00 00002
037B16	DMA3 Request Source Select Register	DM3SL	0X00 00002
037C16 037D16	CRC Data Register	CRCD	XX16 XX16
037E16	CRC Input Register	CRCIN	XX16
037F16			
038016 038116	A/D0 Register 0	AD00	XXXX XXXX2 0000 00002
038216 038316	A/D0 Register 1	AD01	XX16 XX16
038416 038516	A/D0 Register 2	AD02	XX16 XX16
038616 038716	A/D0 Register 3	AD03	XX16 XX16
038816 038916	A/D0 Register 4	AD04	XX16 XX16
038A16 038B16	A/D0 Register 5	AD05	XX16 XX16
038C16 038D16	A/D0 Register 6	AD06	XX16 XX16
038E16 038F16	A/D0 Register 7	AD07	XX16 XX16
039016			
039116			
039216			
039316			
039416	A/D0 Control Register 2	AD0CON2	XX0X XXX02
039516	A/D0 Control Register 3	AD0CON3	XXXX X0002
039616	A/D0 Control Register 0	AD0CON0	0016
039716	A/D0 Control Register 1	AD0CON1	0016
039816	D/A Register 0	DA0	XX16
039916			
039A16	D/A Register 1	DA1	XX16
039B16			
039C16	D/A Control Register	DACON	XXXX XX002
039D16			
039E16			
039F16			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
03A0$_{16}$			
03A1$_{16}$			
03A2$_{16}$			
03A3$_{16}$			
03A4$_{16}$			
03A5$_{16}$			
03A6$_{16}$			
03A7$_{16}$	Function Select Register D1	PSD1	X0XX XX00$_2$
03A8$_{16}$			
03A9$_{16}$			
03AA$_{16}$			
03AB$_{16}$			
03AC$_{16}$			
03AD$_{16}$	Function Select Register C3	PSC3	X0XX XXXX$_2$
03AE$_{16}$			
03AF$_{16}$	Function Select Register C	PSC	00X0 0000$_2$
03B0$_{16}$	Function Select Register A0	PS0	00$_{16}$
03B1$_{16}$	Function Select Register A1	PS1	00$_{16}$
03B2$_{16}$	Function Select Register B0	PSL0	00$_{16}$
03B3$_{16}$	Function Select Register B1	PSL1	00$_{16}$
03B4$_{16}$	Function Select Register A2	PS2	00X0 0000$_2$
03B5$_{16}$	Function Select Register A3	PS3	00$_{16}$
03B6$_{16}$	Function Select Register B2	PSL2	00X0 0000$_2$
03B7$_{16}$	Function Select Register B3	PSL3	00$_{16}$
03B8$_{16}$			
03B9$_{16}$			
03BA$_{16}$			
03BB$_{16}$			
03BC$_{16}$			
03BD$_{16}$			
03BE$_{16}$			
03BF$_{16}$			
03C0$_{16}$	Port P6 Register	P6	XX$_{16}$
03C1$_{16}$	Port P7 Register	P7	XX$_{16}$
03C2$_{16}$	Port P6 Direction Register	PD6	00$_{16}$
03C3$_{16}$	Port P7 Direction Register	PD7	00$_{16}$
03C4$_{16}$	Port P8 Register	P8	XX$_{16}$
03C5$_{16}$	Port P9 Register	P9	XX$_{16}$
03C6$_{16}$	Port P8 Direction Register	PD8	00X0 0000$_2$
03C7$_{16}$	Port P9 Direction Register	PD9	00$_{16}$
03C8$_{16}$	Port P10 Register	P10	XX$_{16}$
03C9$_{16}$			
03CA$_{16}$	Port P10 Direction Register	PD10	00$_{16}$
03CB$_{16}$			
03CC$_{16}$			
03CD$_{16}$			
03CE$_{16}$			
03CF$_{16}$			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
03D0₁₆			
03D1₁₆			
03D2₁₆			
03D3₁₆			
03D4₁₆			
03D5₁₆			
03D6₁₆			
03D7₁₆			
03D8₁₆			
03D9₁₆			
03DA₁₆	Pull-Up Control Register 2	PUR2	00₁₆
03DB₁₆	Pull-Up Control Register 3	PUR3	00₁₆
03DC₁₆			
03DD₁₆			
03DE₁₆			
03DF₁₆			
03E0₁₆	Port P0 Register(1)	P0	XX₁₆
03E1₁₆	Port P1 Register(1)	P1	XX₁₆
03E2₁₆	Port P0 Direction Register(1)	PD0	00₁₆
03E3₁₆	Port P1 Direction Register(1)	PD1	00₁₆
03E4₁₆	Port P2 Register(1)	P2	XX₁₆
03E5₁₆	Port P3 Register(1)	P3	XX₁₆
03E6₁₆	Port P2 Direction Register(1)	PD2	00₁₆
03E7₁₆	Port P3 Direction Register(1)	PD3	00₁₆
03E8₁₆	Port P4 Register(1)	P4	XX₁₆
03E9₁₆	Port P5 Register(1)	P5	XX₁₆
03EA₁₆	Port P4 Direction Register(1)	PD4	00₁₆
03EB₁₆	Port P5 Direction Register(1)	PD5	00₁₆
03EC₁₆			
03ED₁₆			
03EE₁₆			
03EF₁₆			
03F0₁₆	Pull-up Control Register 0	PUR0	00₁₆
03F1₁₆	Pull-up Control Register 1	PUR1	XXXX 0000₂
03F2₁₆			
03F3₁₆			
03F4₁₆			
03F5₁₆			
03F6₁₆			
03F7₁₆			
03F8₁₆			
03F9₁₆			
03FA₁₆			
03FB₁₆			
03FC₁₆			
03FD₁₆			
03FE₁₆			
03FF₁₆	Port Control Register	PCR	XXXX XXX0₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. Pins, functioning as bus control pins, cannot be selected as I/O ports.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V_{CC1}, V_{CC2}	Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_{CC2}	Supply Voltage		-	-0.3 to V_{CC1}	V
AV$_{CC}$	Analog Supply Voltage		V_{CC1}=AV$_{CC}$	-0.3 to 6.0	V
V_I	Input Voltage	$\overline{RESET}$, CNV$_{SS}$, BYTE, P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, V_{REF}, X_{IN}		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$		-0.3 to V_{CC2}+0.3	
		P7$_0$, P7$_1$		-0.3 to 6.0	
V_O	Output Voltage	P6$_0$-P6$_7$, P7$_2$-P7$_7$, P8$_0$-P8$_4$, P8$_6$, P8$_7$, P9$_0$-P9$_7$, P10$_0$-P10$_7$, X_{OUT}		-0.3 to V_{CC1}+0.3	V
		P0$_0$-P0$_7$, P1$_0$-P1$_7$, P2$_0$-P2$_7$, P3$_0$-P3$_7$, P4$_0$-P4$_7$, P5$_0$-P5$_7$		-0.3 to V_{CC2}+0.3	
		P7$_0$, P7$_1$		-0.3 to 6.0	
Pd	Power Dissipation		Topr=25° C	500	mW
Topr	Operating Ambient Temperature			-20 to 85/ -40 to 85(1)	° C
Tstg	Storage Temperature			-65 to 150	° C

NOTE:
1. Contact our sales office if temperature range of -40 to 85° C is required.

Table 5.2 Recommended Operating Conditions

(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V_{CC1}, V_{CC2}	Supply Voltage ($V_{CC1} \geq V_{CC2}$)		3.0	5.0	5.5	V
AVCC	Analog Supply Voltage			V_{CC1}		V
VSS	Supply Voltage			0		V
AVSS	Analog Supply Voltage			0		V
V_{IH}	Input High ("H") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$	0.8V_{CC2}		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0.8V_{CC1}		V_{CC1}	
		$P7_0$, $P7_1$	0.8V_{CC1}		6.0	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0.8V_{CC2}		V_{CC2}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0.5V_{CC2}		V_{CC2}	
V_{IL}	Input Low ("L") Voltage	$P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$	0		0.2V_{CC2}	V
		$P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$(3), $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	0		0.2V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in single-chip mode)	0		0.2V_{CC2}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$ (in memory expansion mode and microprocesor mode)	0		0.16V_{CC2}	
$I_{OH(peak)}$	Peak Output High ("H") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$			-10.0	mA
$I_{OH(avg)}$	Average Output High ("H") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$			-5.0	mA
$I_{OL(peak)}$	Peak Output Low ("L") Current(2)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$			10.0	mA
$I_{OL(avg)}$	Average Output Low ("L") Current(1)	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$			5.0	mA

NOTES:

1. Typical values when average output current is 100 ms.
2. Total $I_{OL(peak)}$ for P0, P1, P2, $P8_6$, $P8_7$, P9, and P10 must be 80 mA or less.
   Total $I_{OL(peak)}$ for P3, P4, P5, P6, P7, and $P8_0$ to $P8_4$ must be 80 mA or less.
   Total $I_{OH(peak)}$ for P0, P1, and P2 must be -40 mA or less.
   Total $I_{OH(peak)}$ for $P8_6$, $P8_7$, P9, and P10 must be -40 mA or less.
   Total $I_{OH(peak)}$ for P3, P4, and P5 must be -40 mA or less.
   Total $I_{OH(peak)}$ for P6, P7, and $P8_0$ to $P8_4$ must be -40 mA or less.
3. V_{IH} and V_{IL} reference for $P8_7$ applies when $P8_7$ is used as a programmable input port.
   It does not apply when $P8_7$ is used as X_{CIN}.

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at Topr=–20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
$f(BCLK)$	CPU Operation Frequency	V_{CC1}=4.2 to 5.5 V	0		32	MHz
		V_{CC1}=3.0 to 5.5 V	0		24	MHz
$f(X_{IN})$	Main Clock Input Frequency	V_{CC1}=4.2 to 5.5 V	0		32	MHz
		V_{CC1}=3.0 to 5.5 V	0		24	MHz
$f(X_{CIN})$	Sub Clock Frequency			32.768	50	kHz
$f(Ring)$	On-chip Oscillator Frequency (Topr=25° C)		0.5	1	2	MHz
$f(PLL)$	PLL Clock Frequency	V_{CC1}=4.2 to 5.5 V	10		32	MHz
		V_{CC1}=3.0 to 5.5 V	10		24	MHz
$t_{SU(PLL)}$	Wait Time to Stabilize PLL Frequency Synthesizer	V_{CC1}=5.0 V			5	ms
		V_{CC1}=3.3 V			10	ms

$V_{CC1}=V_{CC2}=5V$

Table 5.3 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr= –20 to 85°C, f(BCLK)=32MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$	I_{OH}=-5mA	V_{CC2}-2.0		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	I_{OH}=-5mA	V_{CC1}-2.0		V_{CC1}	
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$	I_{OH}=-200µA	V_{CC2}-0.3		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	I_{OH}=-200µA	V_{CC1}-0.3		V_{CC1}	
		X_{OUT}	I_{OH}=-1mA	3.0		V_{CC1}	V
		X_{COUT} High Power	No load applied		2.5		V
		X_{COUT} Low Power	No load applied		1.6		
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	I_{OL}=5mA			2.0	V
		$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	I_{OL}=200µA			0.45	V
		X_{OUT}	I_{OL}=1mA			2.0	V
		X_{COUT} High Power	No load applied		0		V
		X_{COUT} Low Power	No load applied		0		
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, TA0$_{IN}$-TA4$_{IN}$, TB0$_{IN}$-TB5$_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, TA0$_{OUT}$-TA4$_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=5V			5.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-5.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	V_I=0V	20	40	167	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			1.5		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			15		MΩ
V_{RAM}	RAM Standby Voltage	In stop mode		2.0			V
I_{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=32 MHz, Square wave, No division		22	60	mA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			20	µA

$V_{CC1}=V_{CC2}=5V$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition		Standard			Unit
				Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$				10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$	AN_0 to AN_7, ANEX0, ANEX1			±3	LSB
							LSB
			External op-amp connection mode			±7	LSB
							LSB
DNL	Differential Nonlinearity Error					±1	LSB
-	Offset Error					±3	LSB
-	Gain Error					±3	LSB
R_{LADDER}	Resistor Ladder	$V_{REF}=V_{CC1}$		8		40	kΩ
t_{CONV}	10-bit Conversion Time(1, 2)			2.06			µs
t_{CONV}	8-bit Conversion Time(1, 2)			1.75			µs
t_{SAMP}	Sampling Time(1)			0.188			µs
V_{REF}	Reference Voltage			2		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

NOTES:
1. Divide f(X_{IN}), if exceeding 16 MHz, to keep ϕAD frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=4.2$ to 5.5V, $V_{SS}=AV_{SS}=0V$ at Topr=–20 to 85°C, f(BCLK) = 32MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTE:
1. Measurement when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.6 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.7 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTE:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to 5.5V, $V_{SS}=0V$ at Topr=–20 to 85°C unless otherwise specified)

Table 5.8 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.9 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.10 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.11 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.12 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=5V$

Timing Requirements

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.13 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.16 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.17 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.18 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.19 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n=(bx2)-1)

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= b)

$V_{CC1}=V_{CC2}=5V$

Switching Characteristics

(V_{CC} = 4.2 to 5.5V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.20 Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$td_{(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$th_{(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$th_{(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$th_{(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$th_{(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$th_{(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
$th_{(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$th_{(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$td_{(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$th_{(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$td_{(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$th_{(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$td_{(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$th_{(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-5		ns
$td_{(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$th_{(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$tdz_{(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$th_{(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$th_{(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td_{(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, m= (bx2)-1)

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$td_{(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$th_{(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$ (if external bus cycle is aϕ + bϕ, n= a)

$V_{CC1}=V_{CC2}=5V$

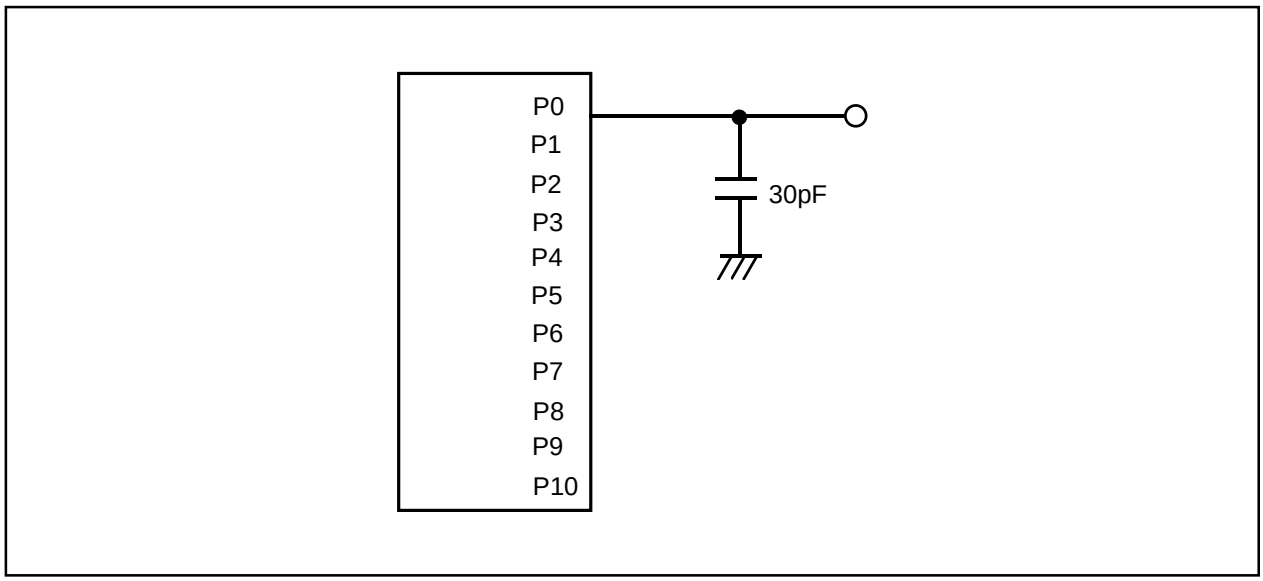


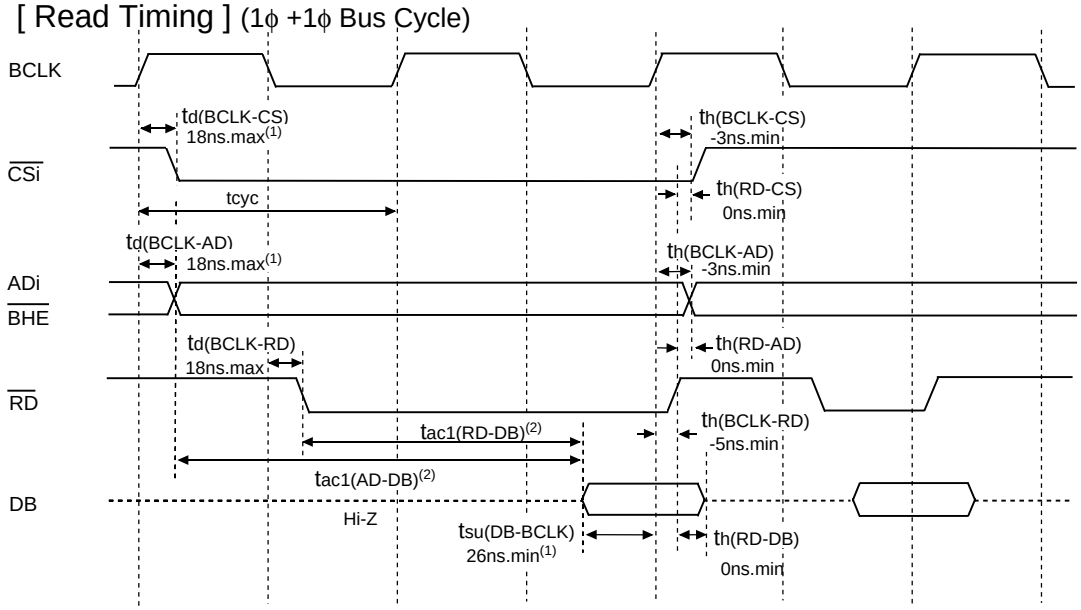
Figure 5.1 P0 to P10 Measurement Circuit

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1φ +1φ Bus Cycle)



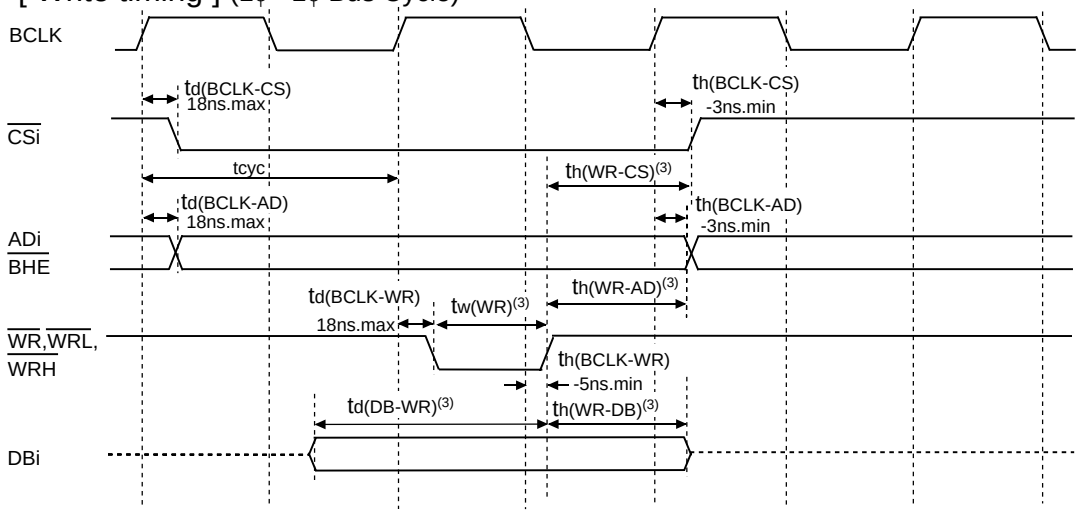
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency:

$t_{ac1(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2)+1)

$t_{ac1(AD-DB)}$=(tcyc x n-35)ns.max (if external bus cycle is aφ + bφ, n=a+b)

[Write timing] (1φ +1φ Bus Cycle)



NOTE:

3. Varies with operation frequency:
$t_{d(DB-WR)}$=(tcyc x m-20)ns.min
(if external bus cycle is aφ+bφ, m=b)
$t_{h(WR-DB)}$=(tcyc/2-10)ns.min
$t_{h(WR-AD)}$=(tcyc/2-10)ns.min
$t_{h(WR-CS)}$=(tcyc/2-10)ns.min
$t_{w(WR)}$=(tcyc/2 x n-15)ns.min
(if external bus cycle is aφ+bφ , n=(bx2)-1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

$$tcyc = \frac{10^9}{f(BCLK)}$$

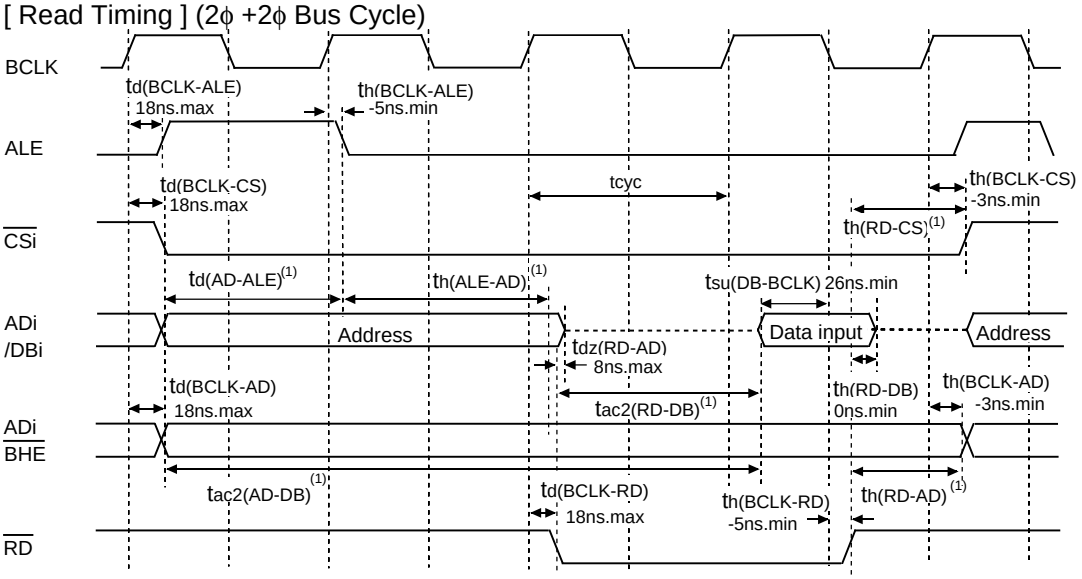
Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1)

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycle)



NOTE:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

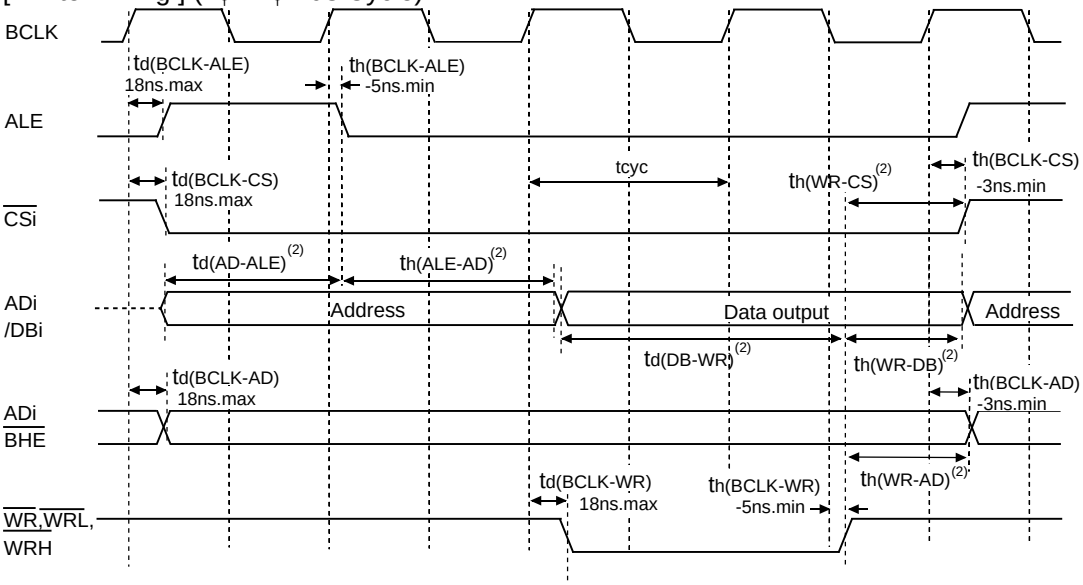
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}+1)

[Write Timing] (2ϕ +2ϕ Bus Cycle)



NOTE:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-10)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=4.2 to 5.5V
- Input high and low voltage: V_{IH}=2.5V, V_{IL}=0.8V
- Output high and low voltage: V_{OH}=2.0V, V_{OL}=0.8V

$$tcyc = \frac{10^9}{f_{(BCLK)}}$$

Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)

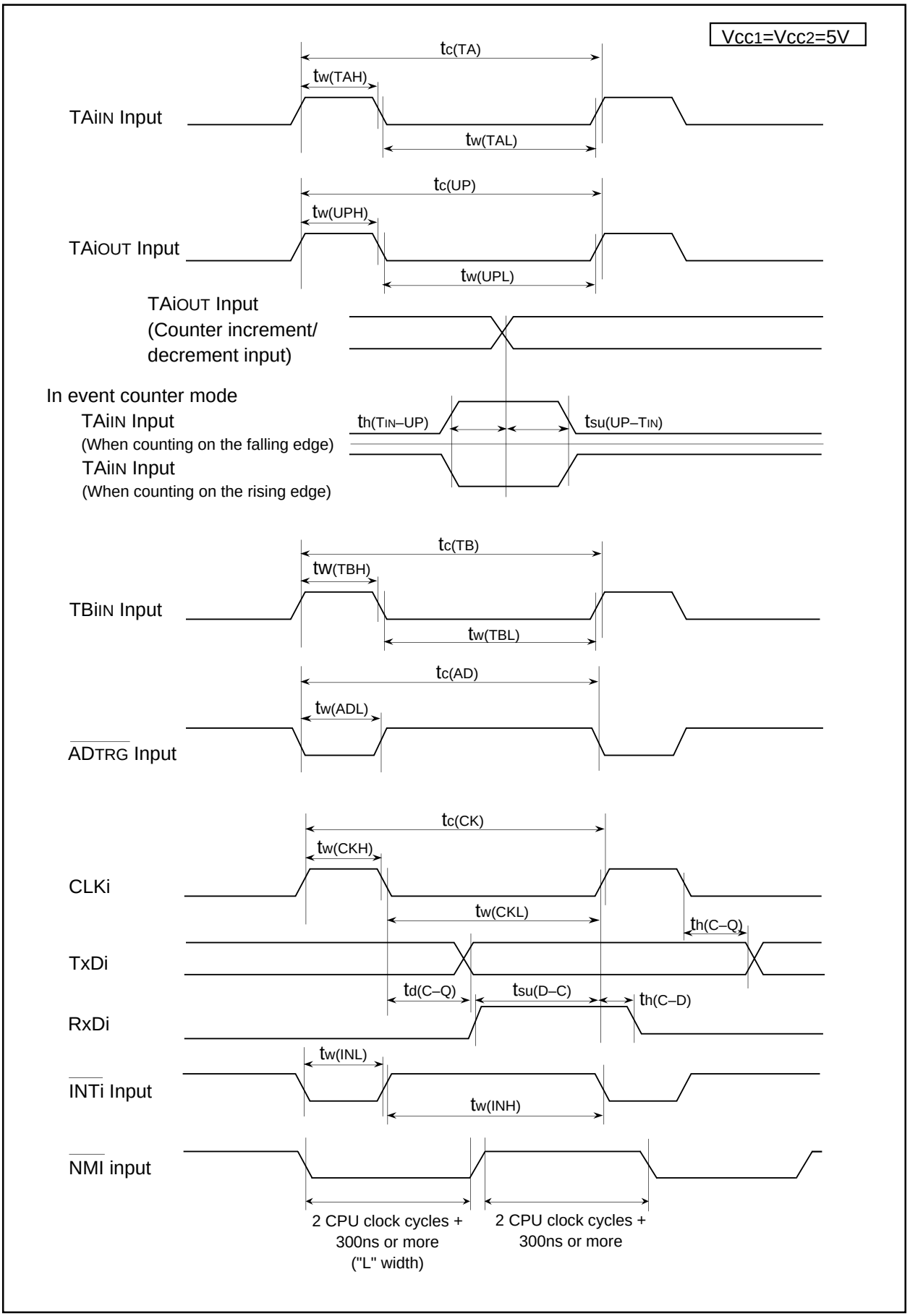
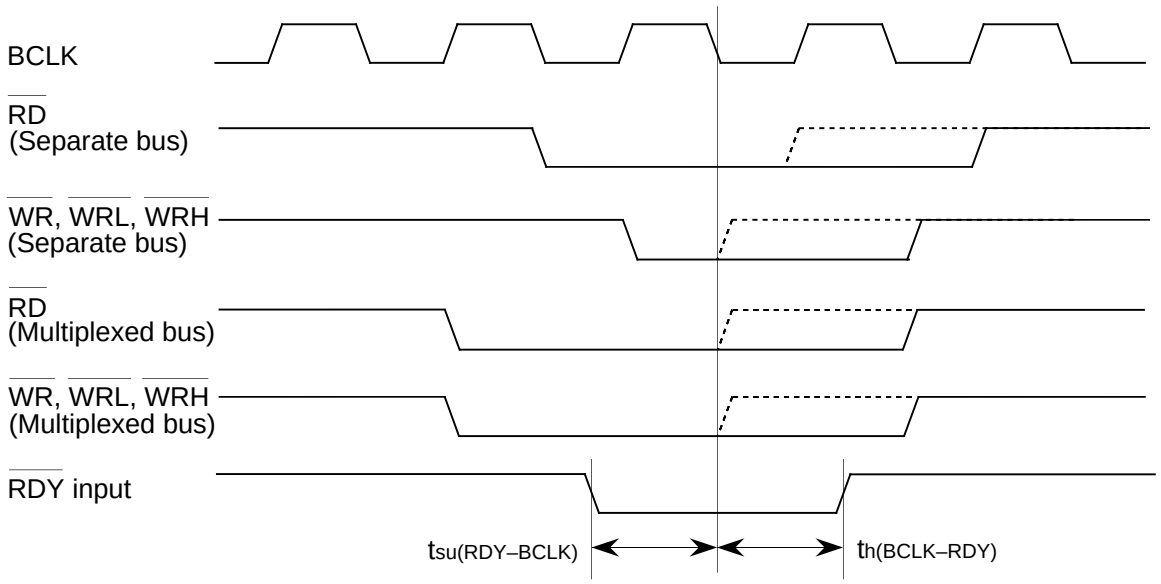
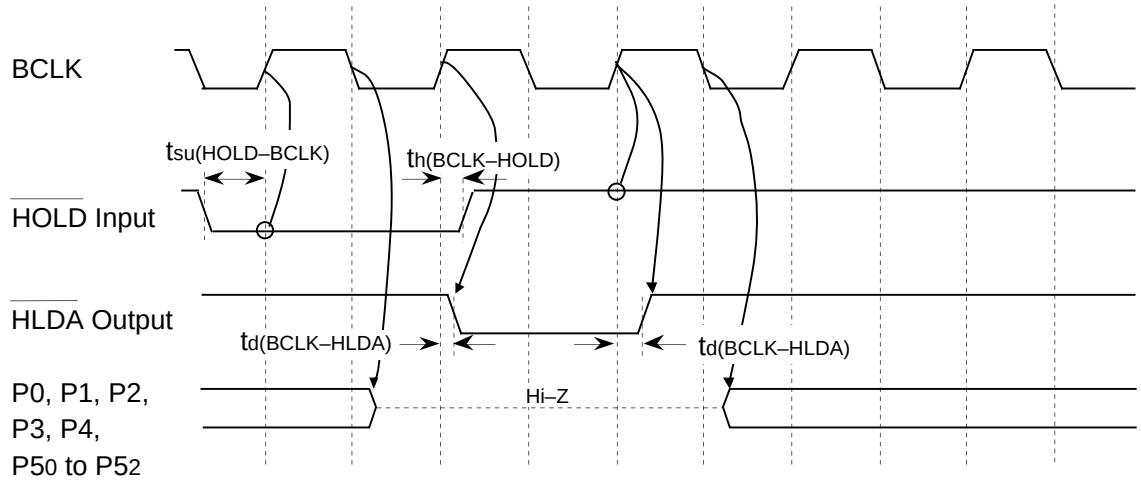


Figure 5.4 Vcc1=Vcc2=5V Timing Diagram (3)

Vcc1=Vcc2=5V

Memory Expansion Mode and Microprocessor Mode





Measurement Conditions
- Vcc1=Vcc2=4.2 to 5.5V
- Input high and low voltage: VIH=4.0V, VIL=1.0V
- Output high and low voltage: VOH=2.5V, VOL=2.5V

Figure 5.5 Vcc1=Vcc2=5V Timing Diagram (4)

$V_{CC1}=V_{CC2}=3.3V$

Table 5.21 Electrical Characteristics ($V_{CC1}=V_{CC2}$=3.0 to 3.6V, V_{SS}=0V at Topr = –20 to 85°C, f(BCLK)=24MHz unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V_{OH}	Output High ("H") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$	I_{OH}=-1mA	V_{CC2}-0.6		V_{CC2}	V
		$P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$		V_{CC1}-0.6		V_{CC1}	V
		X_{OUT}	I_{OH}=-0.1mA	2.7		V_{CC1}	V
		X_{COUT} High Power	No load applied		2.5		V
		X_{COUT} Low Power	No load applied		1.6		V
V_{OL}	Output Low ("L") Voltage	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	I_{OL}=1mA			0.5	V
		X_{OUT}	I_{OL}=0.1mA			0.5	V
		X_{COUT} High Power	No load applied		0		V
		X_{COUT} Low Power	No load applied		0		V
V_{T+}-V_{T-}	Hysteresis	$\overline{HOLD}$, $\overline{RDY}$, $TA0_{IN}$-$TA4_{IN}$, $TB0_{IN}$-$TB5_{IN}$, $\overline{INT0}$-$\overline{INT5}$, $\overline{ADTRG}$, $\overline{CTS0}$-$\overline{CTS4}$, CLK0-CLK4, $TA0_{OUT}$-$TA4_{OUT}$, $\overline{NMI}$, $\overline{KI0}$-$\overline{KI3}$, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		$\overline{RESET}$		0.2		1.8	V
I_{IH}	Input High ("H") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=3V			4.0	µA
I_{IL}	Input Low ("L") Current	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_0$-$P7_7$, $P8_0$-$P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$, X_{IN}, $\overline{RESET}$, CNV_{SS}, BYTE	V_I=0V			-4.0	µA
R_{PULLUP}	Pull-up Resistance	$P0_0$-$P0_7$, $P1_0$-$P1_7$, $P2_0$-$P2_7$, $P3_0$-$P3_7$, $P4_0$-$P4_7$, $P5_0$-$P5_7$, $P6_0$-$P6_7$, $P7_2$-$P7_7$, $P8_0$-$P8_4$, $P8_6$, $P8_7$, $P9_0$-$P9_7$, $P10_0$-$P10_7$	V_I=0V	40	70	500	kΩ
Rf_{XIN}	Feedback Resistance	X_{IN}			3.0		MΩ
Rf_{XCIN}	Feedback Resistance	X_{CIN}			30.0		MΩ
V_{RAM}	RAM Standby Voltage	in stop mode		2.0			V
I_{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V_{SS}.	f(BCLK)=24 MHz, Square wave, No division		17	35	mA
			f(BCLK)=32 kHz, In wait mode, Topr=25° C		10		µA
			While clock stops, Topr=25° C		0.8	5	µA
			While clock stops, Topr=85° C			50	µA

$V_{CC1}=V_{CC2}=3.3V$

Table 5.22 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}$= 3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}$=3.3V			±2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				±1	LSB
-	Offset Error	No S&H (8-bit)				±2	LSB
-	Gain Error	No S&H (8-bit)				±2	LSB
R_{LADDER}	Resistor Ladder		$V_{REF}=V_{CC1}$	8.0		40	kΩ
t_{CONV}	8-bit Conversion Time(1, 2)			6.1			µs
V_{REF}	Reference Voltage			3.3		V_{CC1}	V
V_{IA}	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:
1. Divide f(X_{IN}), if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

Table 5.23 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}$=3.0 to 3.6V, $V_{SS}=AV_{SS}$=0V at Topr = –20 to 85°C, f(BCLK) = 24MHz unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t_{SU}	Setup Time				3	µs
R_O	Output Resistance		4	10	20	kΩ
I_{VREF}	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTE:
1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00_{16}". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.24 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
tc	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
tr	External Clock Rise Time		5	ns
tf	External Clock Fall Time		5	ns

Table 5.25 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTE:
1. Values can be obtained from the following equations, according to BCLK frequecncy and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)+1)

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, n=a+b)

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, m=(bx2)-1)

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35$$ [ns] (if external bus cycle is aϕ + bϕ, p={(a+b-1)x2}+1)

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS}= 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.26 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	100		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	40		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	40		ns

Table 5.27 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	400		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	200		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	200		ns

Table 5.28 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TA)}$	TAi_{IN} Input Cycle Time	200		ns
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.29 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(TAH)}$	TAi_{IN} Input High ("H") Width	100		ns
$t_{w(TAL)}$	TAi_{IN} Input Low ("L") Width	100		ns

Table 5.30 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(UP)}$	TAi_{OUT} Input Cycle Time	2000		ns
$t_{w(UPH)}$	TAi_{OUT} Input High ("H") Width	1000		ns
$t_{w(UPL)}$	TAi_{OUT} Input Low ("L") Width	1000		ns
$t_{su(UP-TIN)}$	TAi_{OUT} Input Setup Time	400		ns
$t_{h(TIN-UP)}$	TAi_{OUT} Input Hold Time	400		ns

$V_{CC1}=V_{CC2}=3.3V$

Timing Requirements

($V_{CC1}=V_{CC2}$= 3.0 to 3.6V, V_{SS} = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.31 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBi_{IN} Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width (counted on both edges)	80		ns

Table 5.32 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Wdth	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.33 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBi_{IN} Input Cycle Time	400		ns
$t_{w(TBH)}$	TBi_{IN} Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBi_{IN} Input Low ("L") Width	200		ns

Table 5.34 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	$\overline{ADTRG}$ Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	$\overline{ADTRG}$ Input Low ("L") Width	125		ns

Table 5.35 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.36 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

($V_{CC1}=V_{CC2}$=3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.37 Memory Expansion Mode and Microprocessor Mode (when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad \text{(if external bus cycle is } a\phi + b\phi, m=b)$$

$V_{CC1}=V_{CC2}=3.3V$

Switching Characteristics

(V_{CC1} = V_{CC2} = 3.0 to 3.6V, VSS = 0V at Topr = –20 to 85°C unless otherwise specified)

Table 5.38 Memory Expansion Mode and Microprocessor Mode (when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdz(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained by the following equations, according to BLCK frequency.

$$th(RD-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR-DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$td(DB-WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns]$$ (if external bus cycle is aφ + bφ, m=(b+2)-1)

3. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

$$td(AD-ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns]$$ (if external bus cycle is aφ + bφ, n=a)

4. Values can be obtained by the following equations, according to BLCK frequency and external bus cycles.

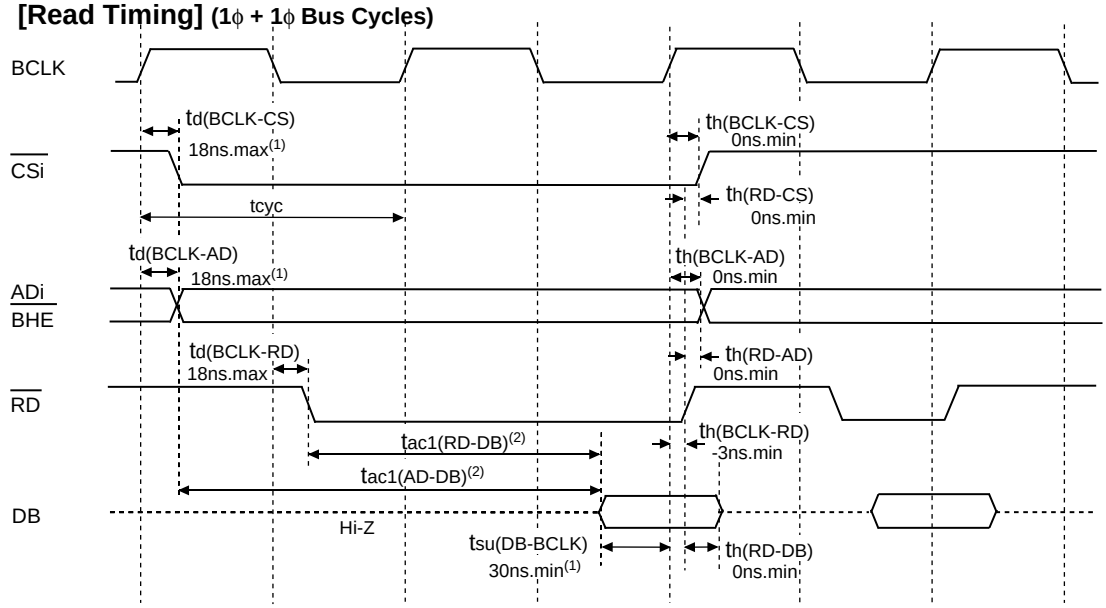
$$th(ALE-AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns]$$ (if external bus cycle is aφ + bφ, n=a)

Vcc1=Vcc2=3.3V

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space)

[Read Timing] (1φ + 1φ Bus Cycles)



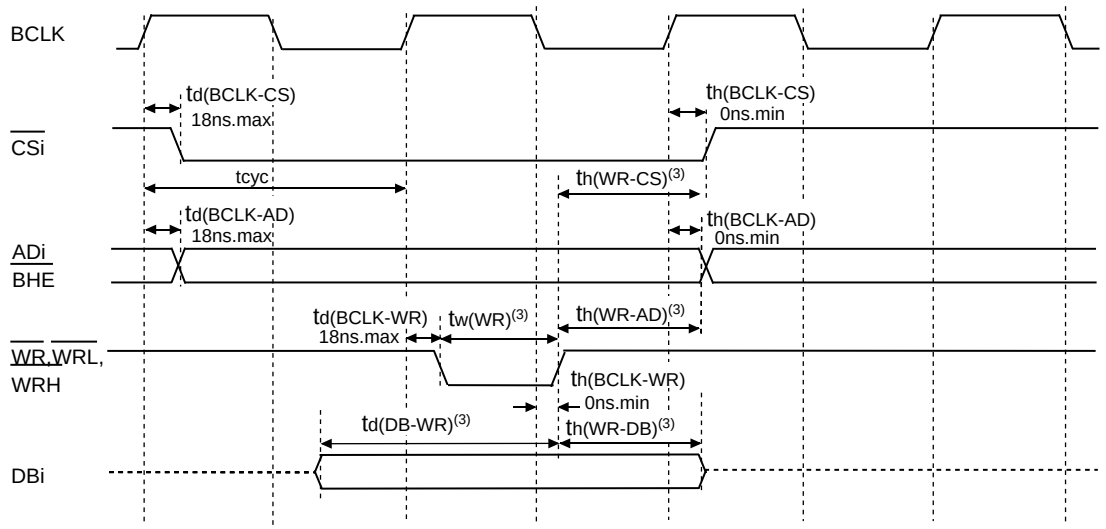
NOTES:

1. Values guaranteed only when the microcomputer is used independently.
   A maximum of 35ns is guaranteed for $t_{d(BCLK-AD)}+t_{su(DB-BCLK)}$.
2. Varies with operation frequency.

   $t_{ac1(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aφ + bφ, m=(b x 2) + 1)

   $t_{ac1(AD-DB)}$=(tcyc x n-35)ns.max (if external bus cycle is aφ + bφ, n = a + b)

[Write Timing] (1φ + 1φ Bus Cycles)



NOTE:

3. Varies with operation frequency.

   $t_{d(DB-WR)}$=(tcyc x m-20)ns.min

   (if external bus cycle is aφ + bφ, m=b)

   $t_{h(WR-DB)}$=(tcyc/2-20)ns.min

   $t_{h(WR-AD)}$=(tcyc/2-10)ns.min

   $t_{h(WR-CS)}$=(tcyc/2-10)ns.min

   $t_{w(WR)}$=(tcyc/2 x n-15)ns.min

   (if external bus cycle is aφ + bφ, n=(bx2)-1)

Measurement Conditions

- $V_{CC1}=V_{CC2}$=3.0 to 3.6V
- Input high and low voltage: V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage: V_{OH}=1.5V, V_{OL}=1.5V

$$tcyc = \frac{10^9}{f(BCLK)}$$

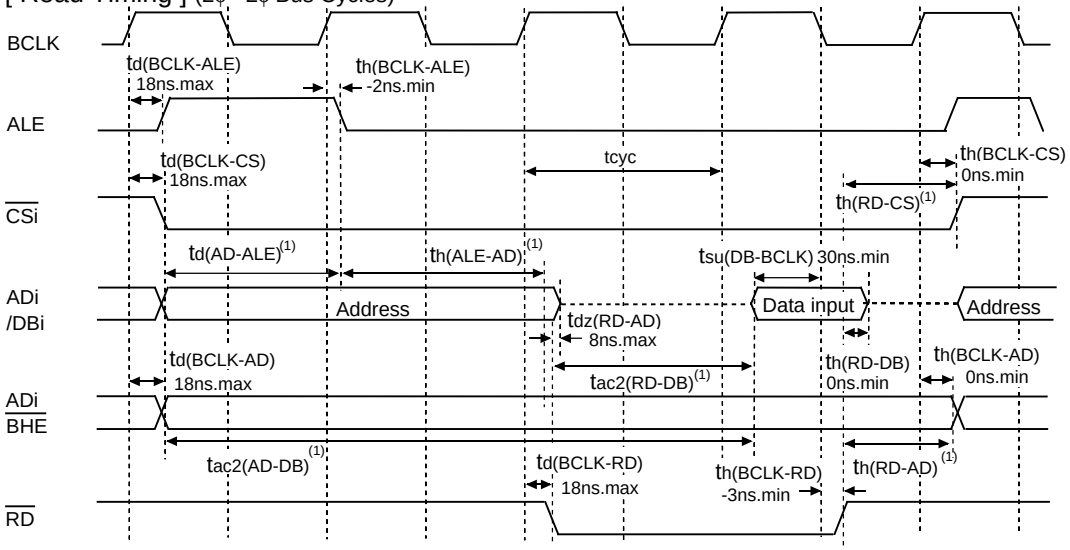
Figure 5.6 $V_{CC1}=V_{CC2}$=3.3V Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

Vcc1=Vcc2=3.3V

(when accessing external memory space and using the multiplexed bus)

[Read Timing] (2ϕ +2ϕ Bus Cycles)



NOTE:

1. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n-20)ns.min (if external bus cycle is aϕ + bϕ, n=a)

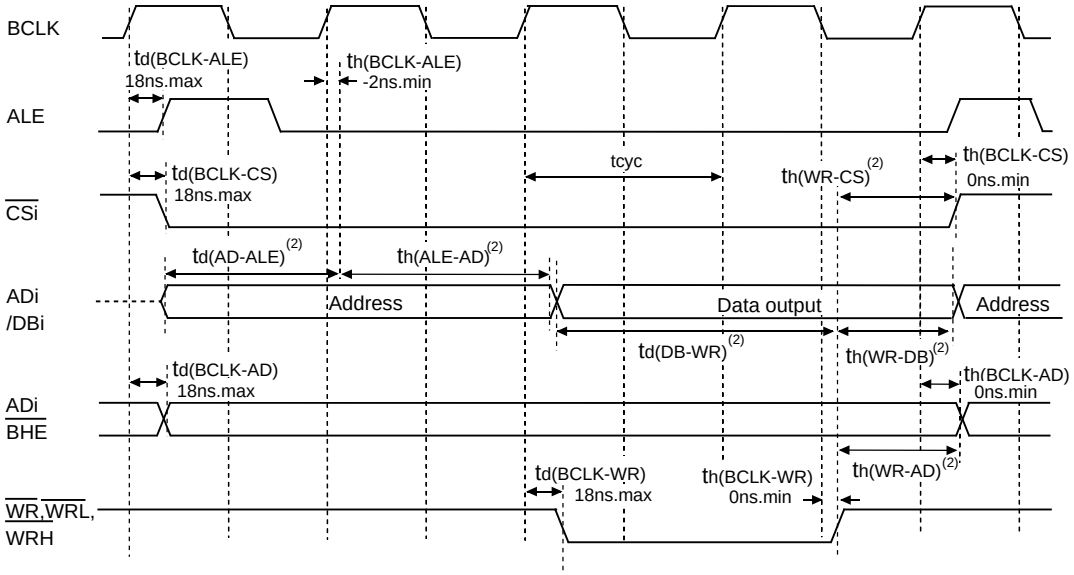
$t_{h(ALE-AD)}$=(tcyc/2 x n-10)ns.min (if external bus cycle is aϕ + bϕ, n=a)

$t_{h(RD-AD)}$=(tcyc/2-10)ns.min, $t_{h(RD-CS)}$=(tcyc/2-10)ns.min

$t_{ac2(RD-DB)}$=(tcyc/2 x m-35)ns.max (if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

$t_{ac2(AD-DB)}$=(tcyc/2 x p-35)ns.max (if external bus cycle is aϕ + bϕ, p={(a+b-1) x 2}+1)

[Write Timing] (2ϕ +2ϕ Bus Cycles)



NOTE:

2. Varies with operation frequency:

$t_{d(AD-ALE)}$=(tcyc/2 x n - 20)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(ALE-AD)}$=(tcyc/2 x n -10)ns.min

(if external bus cycle is aϕ + bϕ, n=a)

$t_{h(WR-AD)}$=(tcyc/2-10)ns.min,

$t_{h(WR-CS)}$=(tcyc/2-10)ns.min, $t_{h(WR-DB)}$=(tcyc/2-20)ns.min

$t_{d(DB-WR)}$=(tcyc/2 x m-25)ns.min

(if external bus cycle is aϕ + bϕ, m=(b x 2)-1)

Measurement Conditions:

- V_{CC1}=V_{CC2}=3.0 to 3.6V
- Input high and low voltage:
  V_{IH}=1.5V, V_{IL}=0.5V
- Output high and low voltage:
  V_{OH}=1.5V, V_{OL}=1.5V

$$tcyc = \frac{10^9}{f_{(BCLK)}}$$

Figure 5.7 Vcc1=Vcc2=3.3V Timing Diagram (2)

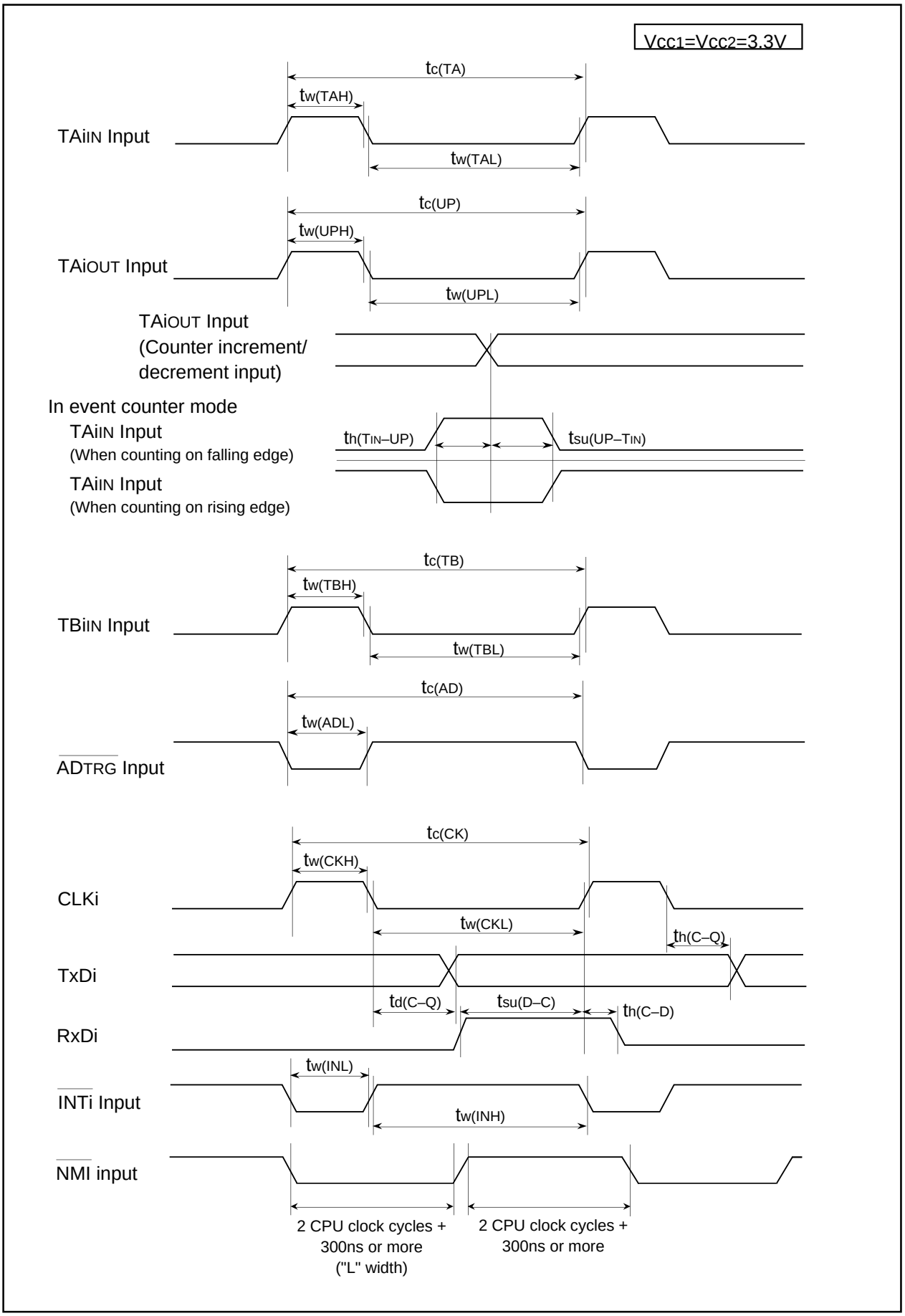
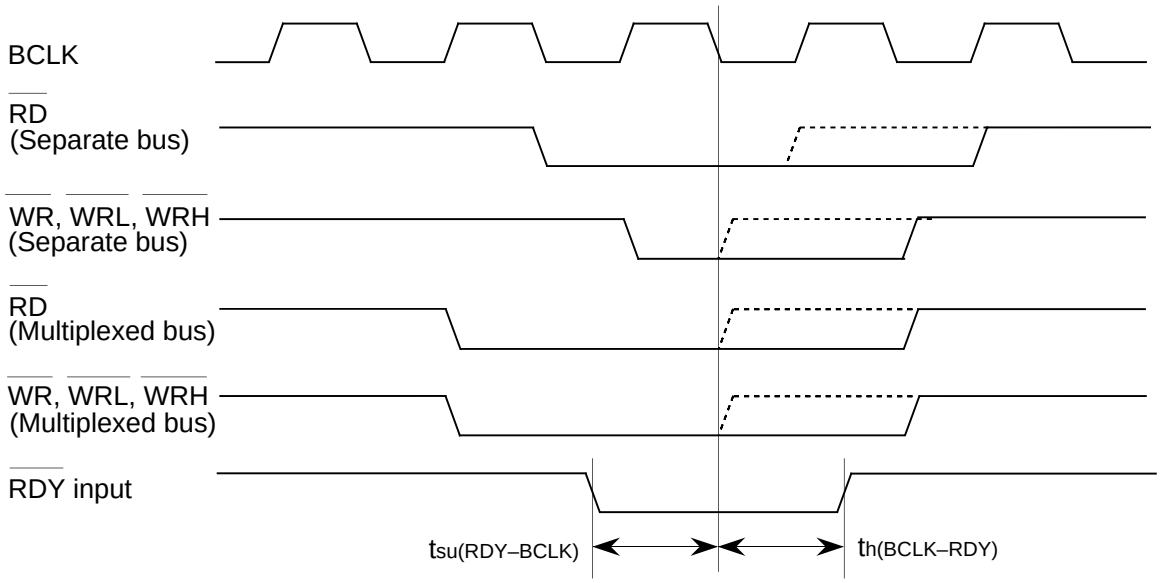
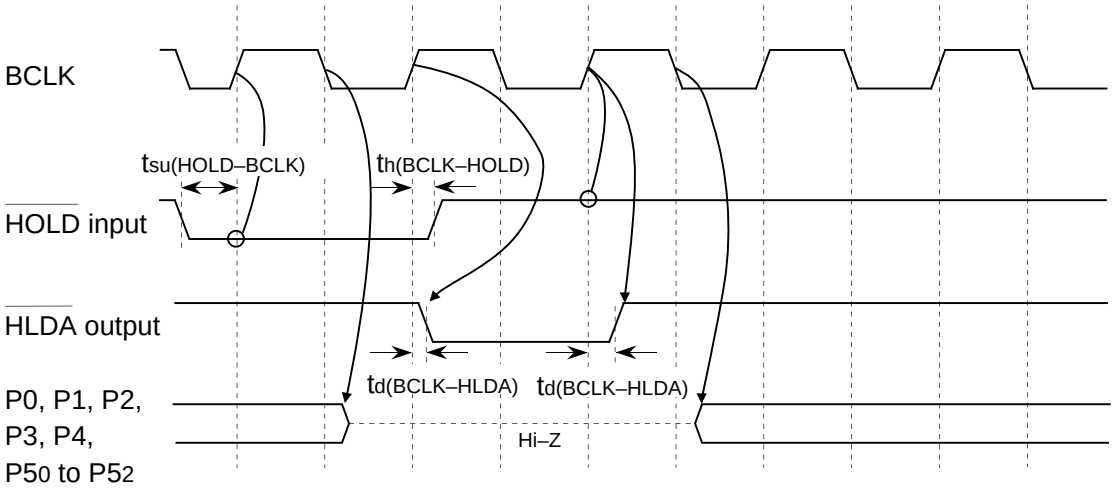


Figure 5.8 Vcc1=Vcc2=3.3V Timing Diagram (3)

$V_{CC1}=V_{CC2}=3.3V$

Memory Expansion Mode and Microprocessor Mode



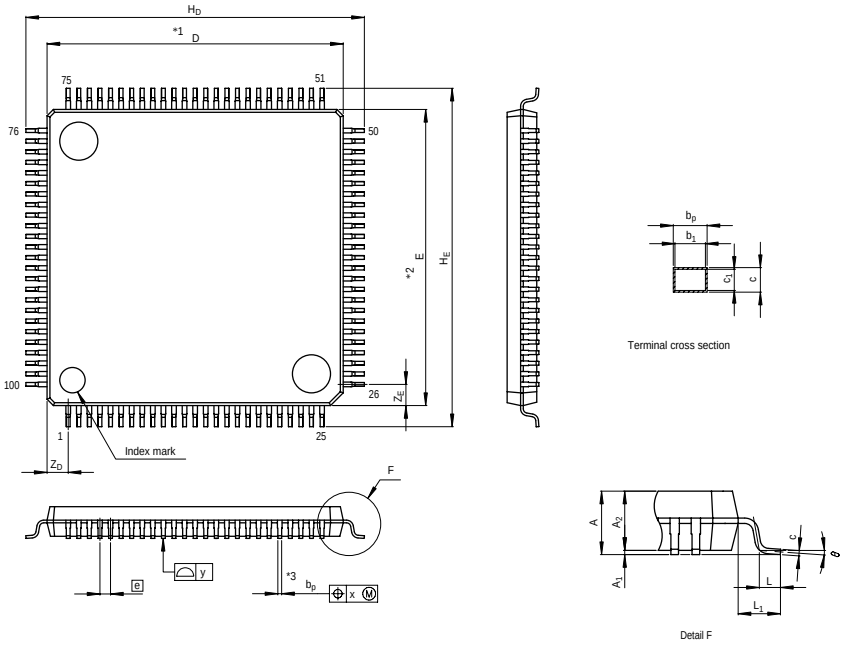


Measurement Conditions:
- $V_{CC1}=V_{CC2}=3.0$ to 3.6V
- Input high and low voltage: $V_{IH}=2.4V$, $V_{IL}=0.6V$
- Output high and low voltage: $V_{OH}=1.5V$, $V_{OL}=1.5V$

Figure 5.9 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

Package Dimensions

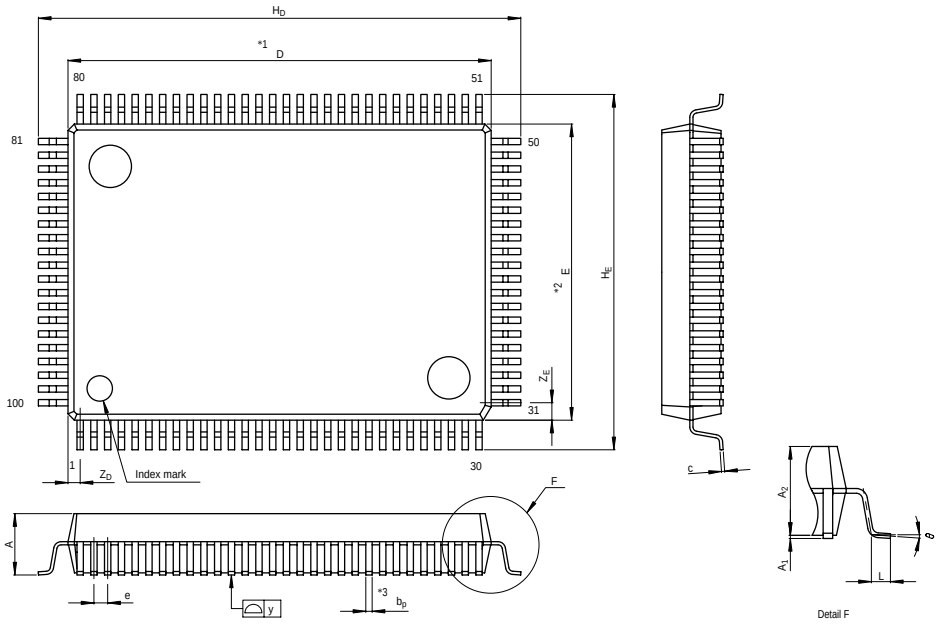
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

REVISION HISTORY	M32C/80 Group Datasheet

Rev.	Date	Description	
		Page	Summary
0.10	**Sep., 02**	–	New Document
0.11	**Sep., 02**	3	Table 1.1.1 “CAN” deleted
0.12	**Nov., 02**	3	Table 1.1.1 “4.2 to 5.5V” --> “3.0 to 5.5V” "3.0 to 3.6V (f(XIN)=20MHz without software wait)" deleted "26mA (f(XIN)=20MHz without software wait,Vcc=3.3V)" deleted
0.30	**Aug., 02**	–	1. Overview changed 1.2 Performance Outline changed 1.3 Block Diagram added 1.5 Pin Assignments changed Table 1.3 Pin Characteristics for 100-Pin Package changed 1.6 Pin Description added 2. Central Processing Unit (CPU) added 3. Memory added 4. Special Function Registers (SFR) added
0.40	**Jun., 04**	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.00	**Nov., 04**		**Overview**
		2, 3	• **Table 1.1 and 1.2 M32C/80 Group Performance** "When using 16-bit bus" added to I/O ports "Option" deleted from Serial I/O, I^2C bus, and IEBus "Voltage Detection Circuit" added Value added to "Power Consumption" "Flash Memory" added
		4	• **1.3 Block Diagram** Description deleted
		5	• **Figure 1.2 ROM/RAM Capacity** deleted
			• **Table 1.3 M32C/85 Group** Note1 deleted
		11	• **Table 1.5 Pin Description** Note 1 added to I/O ports
			Memory
		23	• Chapter Description modified • **Figure 3.1 Memory Map** modified
			SFR
		16-	• "X: Nothing is assigned" modified to "X: Indeterminate" • "?: Indeterminate” modified to "X: Indeterminate" • "Users cannot use any symbols with *" deleted • Register names, symbols, value after RESET of addresses 0017_{16}, $001B_{16}$, $001F_{16}$, $002B_{16}$, $002F_{16}$, $004C_{16}$, and $004D_{16}$ deleted • Value after RESET in the PM0 register revised
		16	• Note 3 deleted
		29	• Note 1 added to addresses $03E0_{16}$ to $03EB_{16}$

REVISION HISTORY	M32C/80 Group Datasheet

Rev.	Date	Description	
		Page	Summary
			Electrical Characteristics
		30-	• This capter added
1.10	**Nov., 05**	All pages	Package code chnaged: 100P6Q-A to PLQP0100KB-A and 100P6S-A to PRQP0100JB-A
			Overview
		1	• Note that the M32C/80 Group is ROMless device added
		2	• **Table 1.1 M32C/80 Group Performance** Item "HDLC Data Processing" changed to "Intelligent I/O Communication Function"; item "Flash Memory" deleted
		3	• **Figure 1.1 M32C/80 Group Block Diagram** Notes 1 and 2 added
		9	• **Table 1.4 Pin Description** Supply voltage for analog power supply input modified "-" to "V_{CC1}"; description for CNV_{SS} changed; supply voltage for $\overline{INT}$ interrupt input modified; note for I/O ports added
			Memory
		15	• **Figure 3.1 Memory Map** Disgram changed; note added
			Special Function Registers (SFRs)
		16	• Note 2 deleted
		17	• Values after RESET in the RMAD6 and RMAD7 registers modified
		19	• Value after RESET in the RLVL register modified
		20	• Value after RESET in the G0RB register modified
		21	• Values after RESET in the G0EMR, G0ERC, and G0IRF registers modified
		26	• Value after RESET in the TCSPR register modified; note 1 added
		27, 28	• Register names, symbols, and value after RESET of addresses 0392_{16} and $03AC_{16}$ deleted
		28	• Value after RESET in the PSC register modified
			Electrical Characteristics
		30-	• Ports P11 to P15 deleted
		32	• **Table 5.2 Recpmmended Operating Conditions** $f_{(BCLK)}$ standard added
		33	• **Table 5.3 Electrical Characteristics** Max. standard for I_{CC} modified
		34	• **Table 5.4 A/D Conversion Characteristics** $AN0_0$ to $AN0_7$ deleted from "INL" row
		35	• **Table 5.7 Memory Expansion Mode and Microprocessor Mode** Expressions on note 1 corrected
		41	• **Figure 5.2 V_{CC1}=V_{CC2}=5V Timing Diagram (1)** Expression for tcyc added; note 3 corrected
		42	• **Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)** Expression for tcyc added; notes 1 and 2 corrected
		46	• **Table 5.22 A/D Conversion Characteristics** Min. standard for V_{REF} modified
		47	• **Table 5.25 Memory Expansion Mode and Microprocessor Mode** Expressions on note 1 corrected
		52	• **Figure 5.6 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)** Expression for tcyc added; note 3 corrected

Rev.	Date	Description	
		Page	Summary
		53	• **Figure 5.7 V_{CC1}=V_{CC2}=3.3V Timing Diagram (2)** Expression for tcyc added; notes 1 and 2 corrected

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