

High-ESD Profibus RS-485 Transceiver

General Description

The MAX14770E is a half-duplex, $\pm 35\text{kV}$ high ESD-protected transceiver for PROFIBUS-DP and RS-485 applications. In addition, it can be used for RS-422/V.11 communications. The MAX14770E is designed to meet IEC 61158-2, TIA/EIA-422-B, TIA/EIA-485-A, V.11, and X.27 standards.

The MAX14770E operates from a +5V supply and has true fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted.

The MAX14770E features a 1/4 standard-unit load receiver input impedance, allowing up to 128 1/4 unit load transceivers on the bus. Drivers are short-circuit current limited and are protected against excessive power dissipation by thermal-shutdown circuitry.

The MAX14770E is available in an 8-pin SO and an 8-pin μMAX specified over the extended (-40°C to $+105^\circ\text{C}$) temperature range. It is also available in a tiny TDFN (3mm x 3mm) package and specified over the automotive (-40°C to $+125^\circ\text{C}$) temperature range.

Applications

PROFIBUS-DP Networks
Industrial Fieldbuses
Motion Controllers
RS-485 Networks
Machine Encoders

Typical PROFIBUS-DP Operating Circuit appears at end of data sheet.

Features

- ◆ Meets EIA 61158-2 Type 3 PROFIBUS-DP
- ◆ +4.5V to +5.5V Supply Voltage
- ◆ 20Mbps Data Rate
- ◆ Short-Circuit Protected
- ◆ True Fail-Safe Receiver
- ◆ Thermal-Shutdown Protected
- ◆ Hot Swappable
- ◆ High ESD Protection
 - ◆ $\pm 35\text{kV}$ Human Body Model (HBM)
 - ◆ $\pm 20\text{kV}$ IEC 61000-4-2 Air Gap
 - ◆ $\pm 10\text{kV}$ IEC 61000-4-2 Contact
- ◆ -40°C to $+125^\circ\text{C}$ Automotive Temperature Range in Tiny 8-Pin (3mm x 3mm) TDFN

Ordering Information

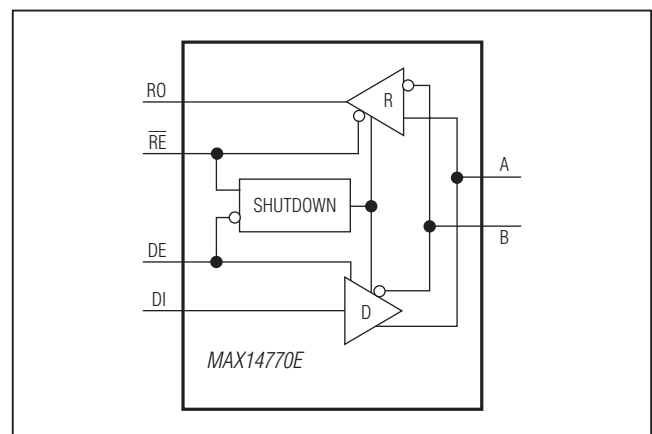
PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX14770EGUA+T	-40°C to $+105^\circ\text{C}$	8 μMAX	—
MAX14770EGSA+T	-40°C to $+105^\circ\text{C}$	8 SO	—
MAX14770EATA+T	-40°C to $+125^\circ\text{C}$	8 TDFN-EP*	BMG

+ Denotes a lead (Pb)-free/RoHS-compliant package.

T = Tape and reel.

*EP = Exposed pad.

Functional Diagram



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For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

MAX14770E

High-ESD Profibus RS-485 Transceiver

ABSOLUTE MAXIMUM RATINGS

(Voltages referenced to GND.)

V _{CC}	-0.3V to +6.0V
RE, RO.....	-0.3V to (V _{CC} + 0.3V)
DE, DI.....	-0.3V to +6.0V
A, B.....	-8.0V to +13.0V
Short-Circuit Duration (RO, A, B) to GND.....	Continuous
Continuous Power Dissipation (T _A = +70°C)	
SO (derate 7.6mW/°C above +70°C).....	606mW
TDFN (derate 24.4mW/°C above +70°C).....	1951mW
μMAX (derate 4.8mW/°C above +70°C).....	387.8mW

Operating Temperature Range

μMAX.....	-40°C to +105°C
SO.....	-40°C to +105°C
TDFN.....	-40°C to +125°C
Storage Temperature Range.....	-65°C to +150°C
Junction Temperature Range.....	-40°C to +150°C
Lead Temperature (soldering, 10s).....	+300°C
Soldering Temperature (reflow).....	+260°C

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SO

Junction-to-Ambient Thermal Resistance (θ _{JA}).....	132°C/W
Junction-to-Case Thermal Resistance (θ _{JC}).....	38°C/W

μMAX

Junction-to-Ambient Thermal Resistance (θ _{JA}).....	206.3°C/W
Junction-to-Case Thermal Resistance (θ _{JC}).....	42°C/W

TDFN

Junction-to-Ambient Thermal Resistance (θ _{JA}).....	41°C/W
Junction-to-Case Thermal Resistance (θ _{JC}).....	8°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Power-Supply Range	V _{CC}		4.5		5.5	V
Supply Current	I _{CC}	DE = 1, RE = 0 or DE = 0, RE = 0 or DE = 1, RE = 1; no load		2.5	4	mA
Shutdown Supply Current	I _{SH}	DE = 0, RE = 1			15	μA
DRIVER						
Differential Driver Output	I _{VODI}	R _L = 54Ω, DI = V _{CC} or GND; Figure 1	2.1			V
Differential Driver Peak-to-Peak Output	V _{ODPP}	Figure 2 (Note 3)	4.0		6.8	V
Change in Magnitude of Differential Output Voltage	ΔV _{OD}	R _L = 54Ω; Figure 1 (Note 4)	-0.2	0	+0.2	V
Driver Common-Mode Output Voltage	V _{OC}	R _L = 54Ω; Figure 1		1.8	3	V
Change in Common-Mode Voltage	ΔV _{OC}	R _L = 54Ω; Figure 1 (Note 4)	-0.2		+0.2	V
Driver Short-Circuit Output Current (Note 5)	I _{OSD}	0V ≤ V _{OUT} ≤ +12V; output low			+250	mA
		-7V ≤ V _{OUT} ≤ V _{CC} ; output high	-250			

MAX14770E

High-ESD Profibus RS-485 Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(VCC = +5V ±10%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V, TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Driver Short-Circuit Foldback Output Current (Note 5)	IOSDF	$(V_{CC} - 1V) \leq V_{OUT} \leq +12V$; output low	-15			mA
		$-7V \leq V_{OUT} \leq +1V$; output high			+15	
LOGIC INPUTS						
Driver Input High Voltage	VIH	DE, DI, \overline{RE}	2.0			V
Driver Input Low Voltage	VIL	DE, DI, \overline{RE}			0.8	V
Driver Input Hysteresis	VHYS	DE, DI, \overline{RE}		50		mV
Driver Input Current	IIN	DE, DI, \overline{RE}	-1		+1	μA
Input Impedance in Hot Swap	RDE	Figure 11 until the first low-to-high transition of DE occurs	1	5.6	10	kΩ
	R \overline{RE}	Figure 11 until the first high-to-low transition of \overline{RE} occurs				
RECEIVER						
Input Current (A, B)	IA, IB	DE = GND, VCC = VGND or +5.5V	VIN = 12V		+250	μA
			VIN = -7V	-200		
Differential Input Capacitance	CAB	Between A and B, DE = \overline{RE} = GND at 6MHz		8		pF
Receiver Differential Threshold Voltage	VTH	$-7V \leq V_{CM} \leq 12V$	-200	-125	-50	mV
Receiver Input Hysteresis	ΔVTH	VCM = 0V		15		mV
LOGIC OUTPUT						
Output High Voltage	VOH	IOUT = -6mA, VA - VB = VTH	4			V
Output Low Voltage	VOL	IOUT = 6mA, VA - VB = -VTH			0.4	V
Three-State Receiver Output Current	IOZR	$0V \leq V_{OUT} \leq V_{CC}$	-1		+1	μA
Receiver Input Resistance	RIN	$-7V \leq V_{CM} \leq 12V$	48			kΩ
Receiver Output Short-Circuit Current	IOSR	$0V \leq V_{RO} \leq V_{CC}$	-110		+110	mA
PROTECTION SPECIFICATIONS						
Thermal-Shutdown Threshold	VTS			+160		°C
Thermal-Shutdown Hysteresis	VTSH			15		°C
ESD Protection, A and B Pins		HBM		±35		kV
		IEC 61000-4-2 Air-Gap Discharge to GND		±20		
		IEC 61000-4-2 Contact Discharge to GND		±10		

MAX14770E

High-ESD Profibus RS-485 Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±10%, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ESD Protection, All Other Pins		HBM		±2		kV
DRIVER SWITCHING CHARACTERISTICS						
Driver Propagation Delay	t _{DPLH}	R _L = 54Ω, C _L = 50pF; Figures 3 and 4		15	28	ns
	t _{DPHL}					
Differential Driver Output Skew t _{DPLH} - t _{DPHL}	t _{DSKEW}	R _L = 54Ω, C _L = 50pF; Figures 3 and 4		1.2		ns
Driver Output Transition Skew t _{t(MLH)} , t _{t(MHL)}	t _{TSKEW}	R _L = 54Ω, C _L = 50pF; Figures 3 and 5		2		ns
Driver Differential Output Rise or Fall Time	t _{LH} , t _{HL}	R _L = 54Ω, C _L = 50pF; Figures 3 and 4		7	15	ns
Maximum Data Rate			20			Mbps
Driver Enable to Output High	t _{DZH}	R _L = 500Ω, C _L = 50pF; Figure 6		25	48	ns
Driver Enable to Output Low	t _{DZL}	R _L = 500Ω, C _L = 50pF; Figure 7		25	48	ns
Driver Disable Time from Low	t _{DLZ}	R _L = 500Ω, C _L = 50pF; Figure 7		20	40	ns
Driver Disable Time from High	t _{DHZ}	R _L = 500Ω, C _L = 50pF; Figure 6		20	40	ns
Driver Enable Skew Time	t _{ZL} - t _{ZH}	R _L = 500Ω, C _L = 50pF; Figures 6 and 7			8	ns
Driver Disable Skew Time	t _{LZ} - t _{HZ}	R _L = 500Ω, C _L = 50pF; Figures 6 and 7			8	ns
Driver Enable High—Propagation Delay Difference	t _{DZH} - t _{DPHL}			8	20	ns
Driver Enable Low—Propagation Delay Difference	t _{DZL} - t _{DPHL}			10	20	ns
Driver Enable from Shutdown to Output High	t _{DZL(SHDN)}	R _L = 500Ω, C _L = 50pF; Figure 7 (Note 6)		46	100	μs
Driver Enable from Shutdown to Output Low	t _{DZH(SHDN)}	R _L = 500Ω, C _L = 50pF; Figure 6 (Note 6)		46	100	μs
Time to Shutdown	t _{SHDN}	(Note 6)	50		800	ns

MAX14770E

High-ESD Profibus RS-485 Transceiver

ELECTRICAL CHARACTERISTICS (continued)

(VCC = +5V ±10%, TA = TMIN to TMAX, unless otherwise noted. Typical values are at VCC = +5V, TA = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
RECEIVER SWITCHING CHARACTERISTICS						
Receiver Propagation Delay	tRPLH	CL = 15pF; Figures 8 and 9 (Note 7)			28	ns
	tRPHL					
Receiver Output Skew	tRSKEW	CL = 15pF; Figures 8 and 9 (Notes 7, 8)			2	ns
Maximum Data Rate			20			Mbps
Receiver Enable to Output High	tRZH	S2 closed; RL = 1kΩ, CL = 15pF; Figure 10			30	ns
Receiver Enable to Output Low	tRZL	S1 closed; RL = 1kΩ, CL = 15pF; Figure 10			30	ns
Receiver Disable Time from Low	tRLZ	S1 closed; RL = 1kΩ, CL = 15pF; Figure 10			30	ns
Receiver Disable Time from High	tRHZ	S2 closed; RL = 1kΩ, CL = 15pF; Figure 10			30	ns
Receiver Enable from Shutdown to Output High	tRZL(SHDN)	S1 closed; RL = 1kΩ, CL = 15pF; Figure 10 (Notes 6, 7)			100	μs
Receiver Enable from Shutdown to Output Low	tRZH(SHDN)	S2 closed; RL = 1kΩ, CL = 15pF; Figure 10 (Notes 6, 7)			100	μs
Time to Shutdown	tSHDN	(Note 6)	50		800	ns

Note 2: Devices are production tested at TA = +25°C. Specifications over temperature limits are guaranteed by design.

Note 3: VODPP is the difference in VOD, with the DI at high and DI at low.

Note 4: ΔVOD and ΔVOC are the changes in |VOD| and |VOC|, respectively, with the DI at high and DI at low.

Note 5: The short-circuit output current applies to peak current just prior to foldback current limiting; the short-circuit foldback output current applies during current limiting to allow a recovery from bus contention.

Note 6: Shutdown is enabled by bringing RE high and DE low. If the enable inputs are in this state for less than 50ns, the device is guaranteed not to enter shutdown. If the enable inputs are in this state for at least 800ns, the device is guaranteed to have entered shutdown.

Note 7: Capacitive load includes test probe and fixture capacitance.

Note 8: Guaranteed by characterization; not production tested.

MAX14770E

High-ESD Profibus RS-485 Transceiver

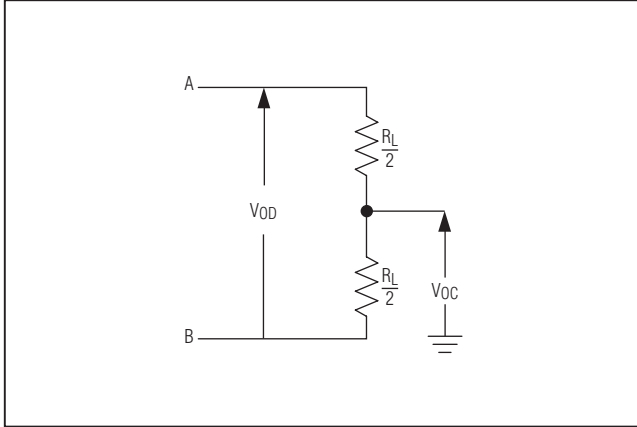


Figure 1. Driver DC Test Load

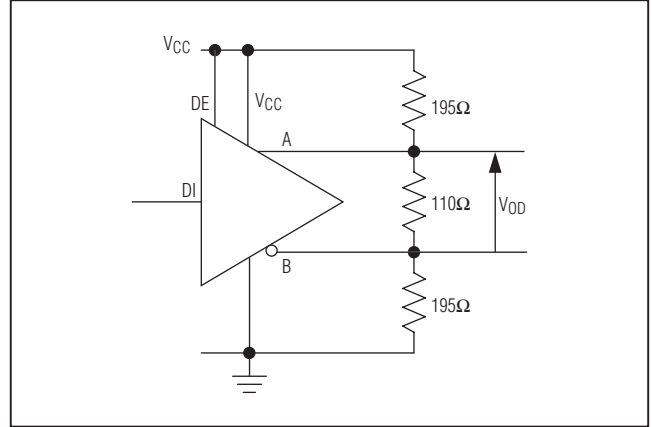


Figure 2. V_{ODPP} Swing Under Profibus Equivalent Load Test

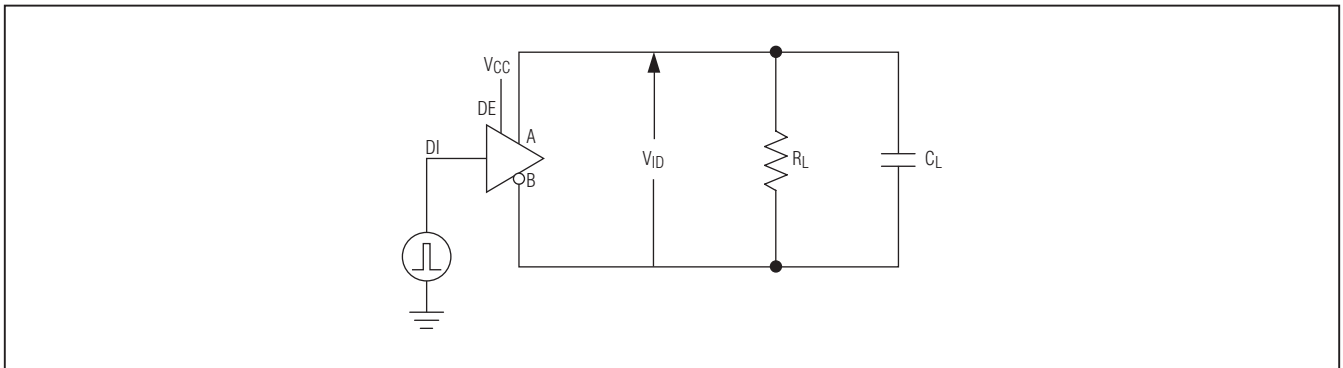


Figure 3. Driver Timing Test Circuit

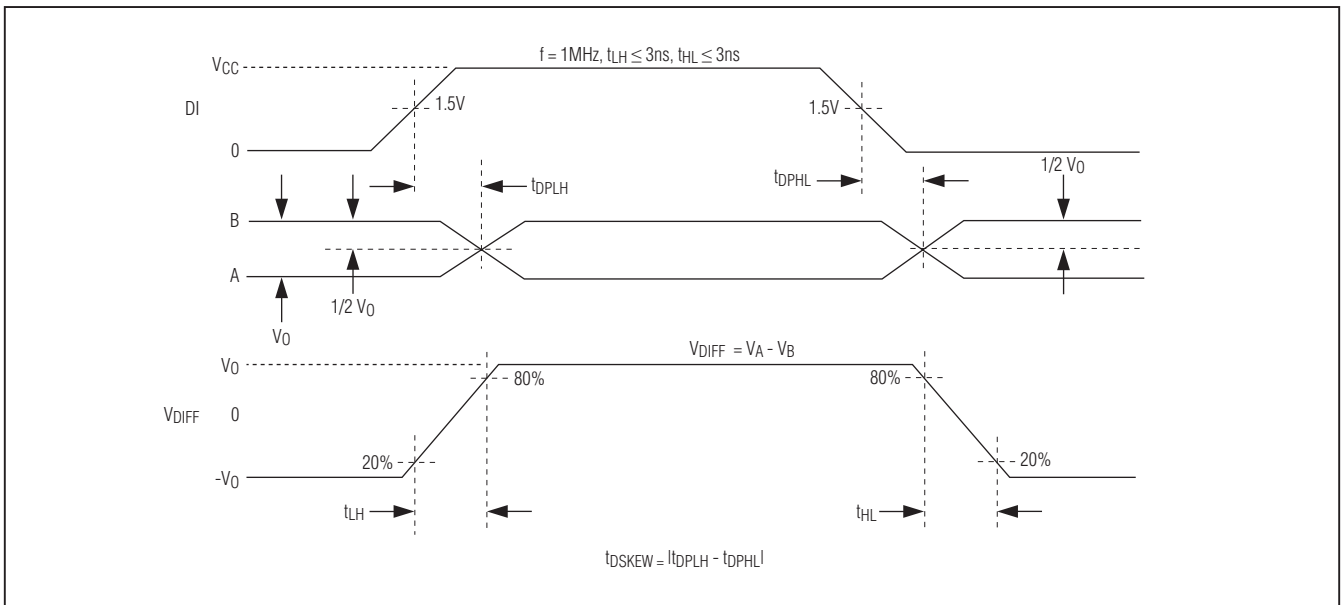


Figure 4. Driver Propagation Delays

MAX14770E

High-ESD Profibus RS-485 Transceiver

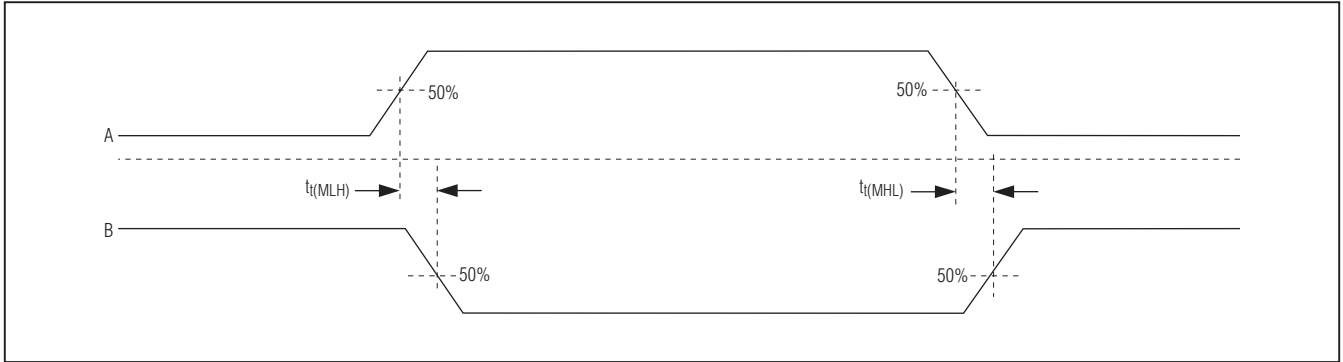


Figure 5. Driver Transition Skew

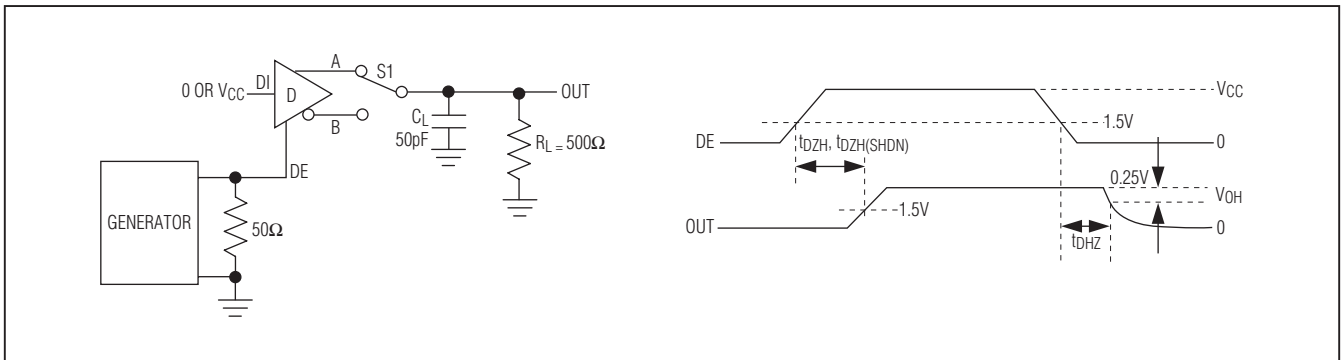


Figure 6. Driver Enable and Disable Times

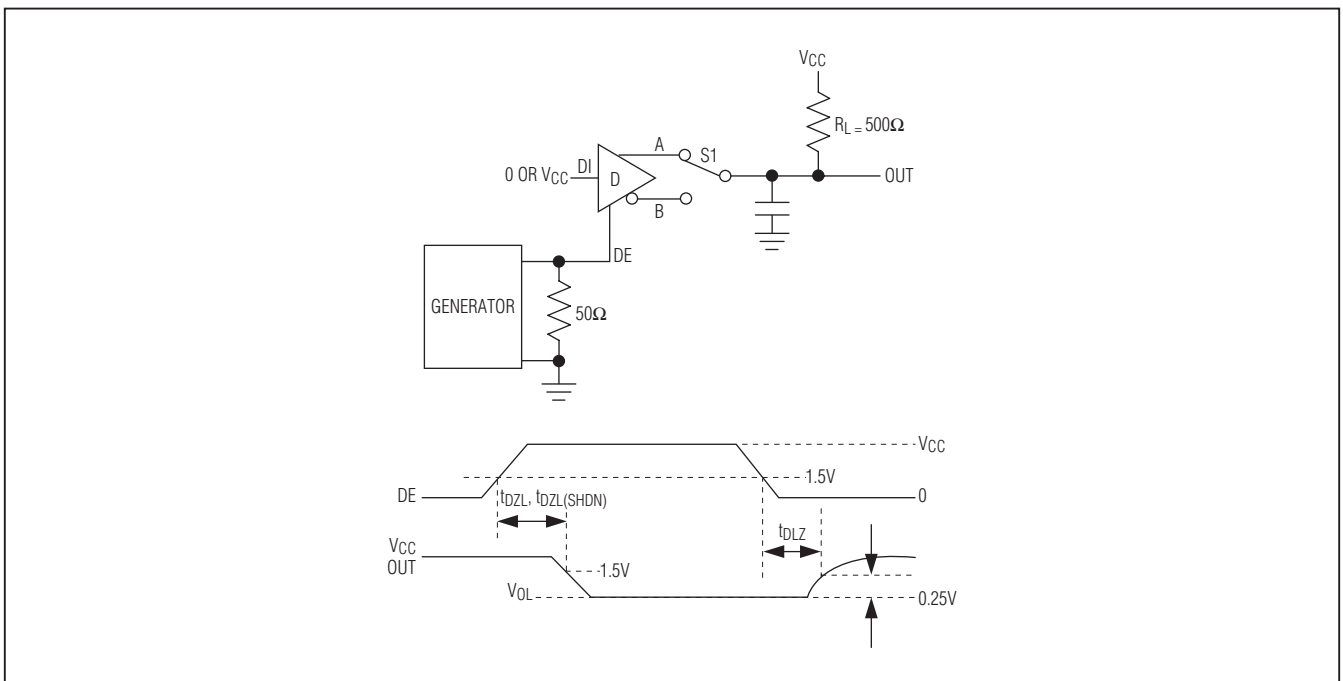


Figure 7. Driver Enable and Disable Times

MAX14770E

High-ESD Profibus RS-485 Transceiver

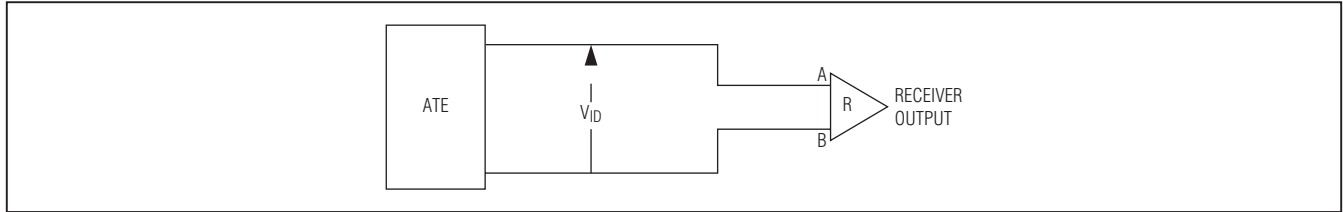


Figure 8. Receiver Propagation Delay Test Circuit

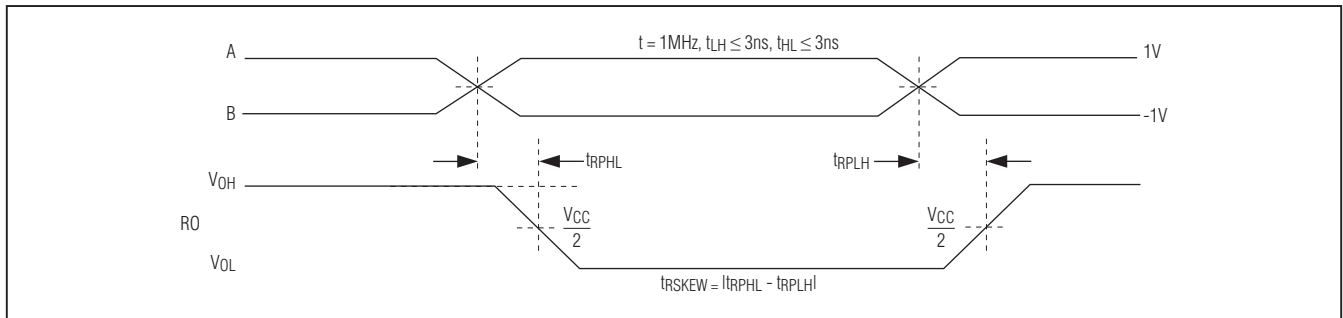


Figure 9. Receiver Propagation Delays

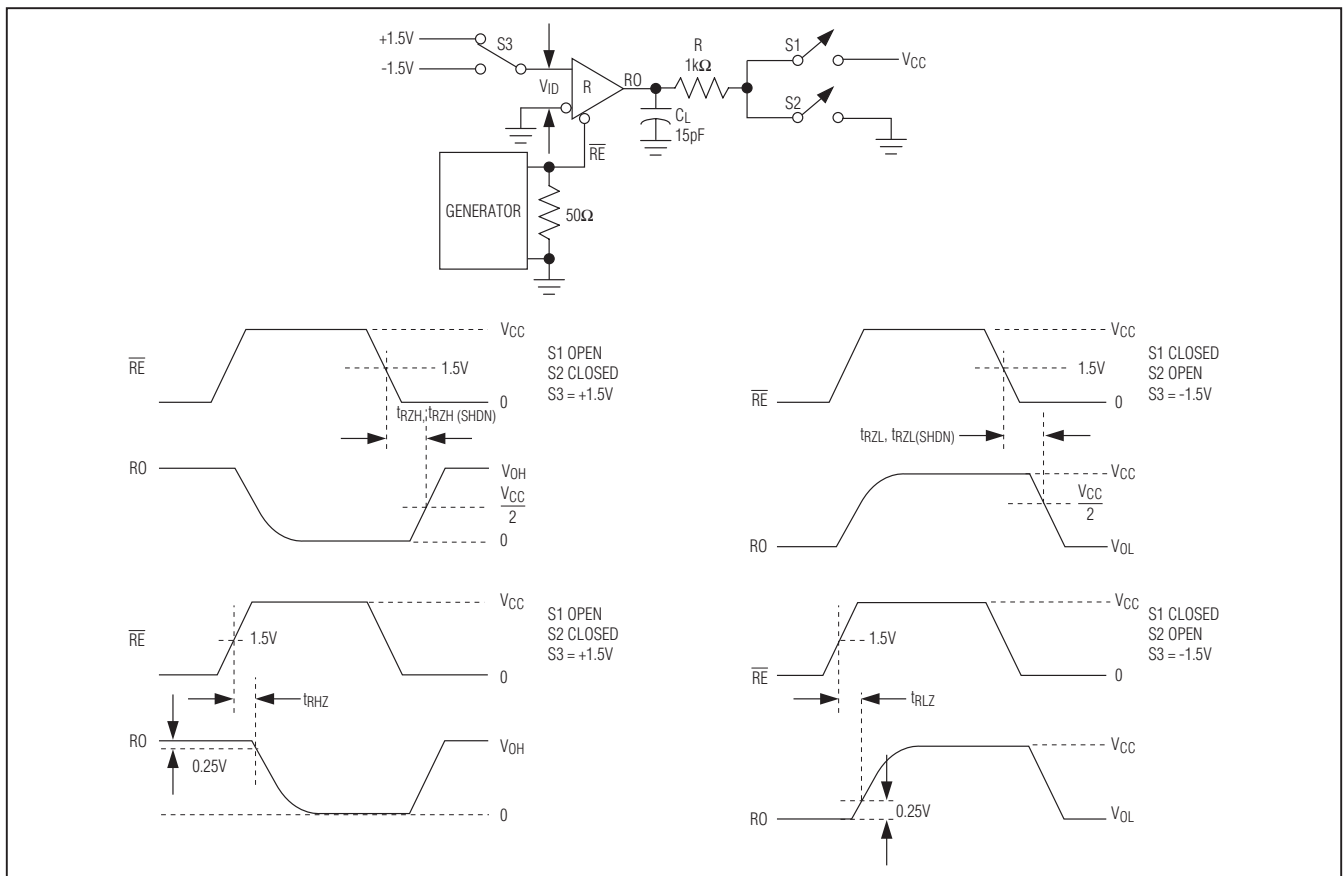


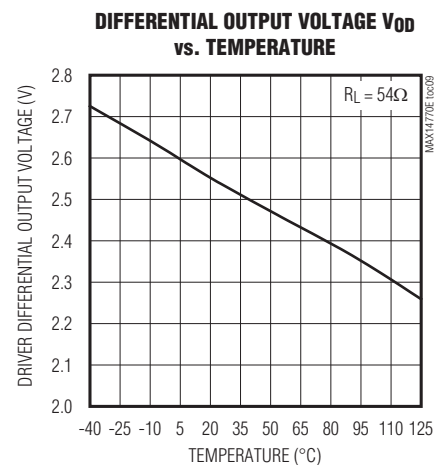
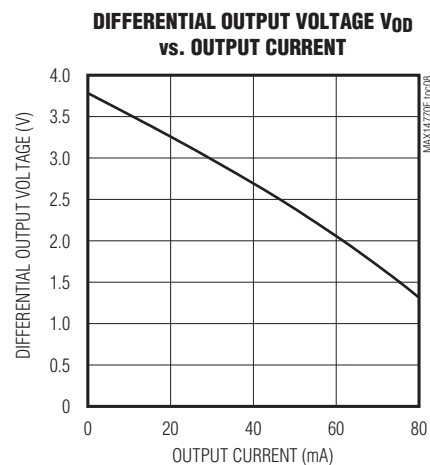
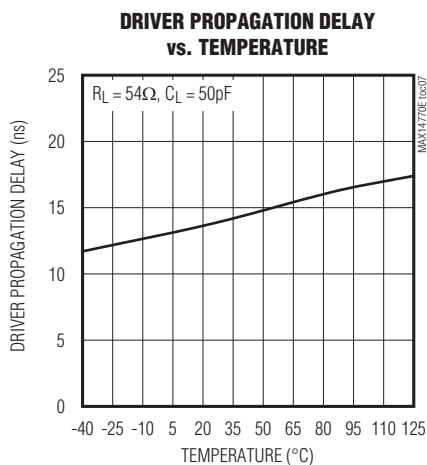
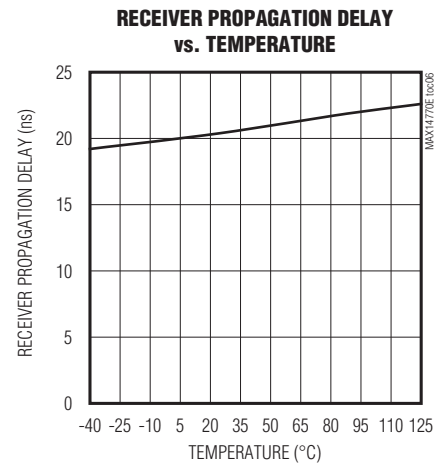
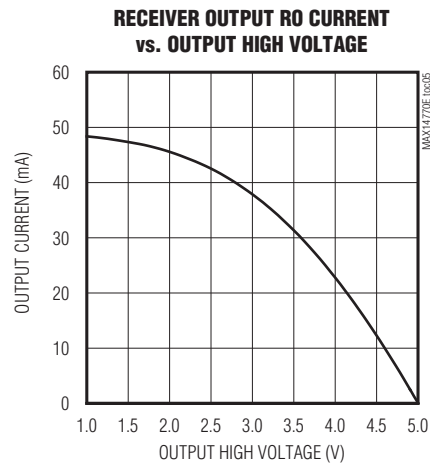
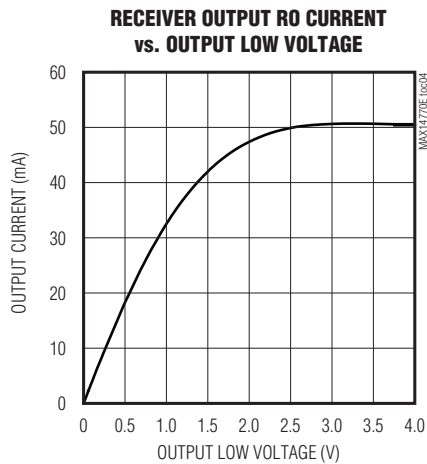
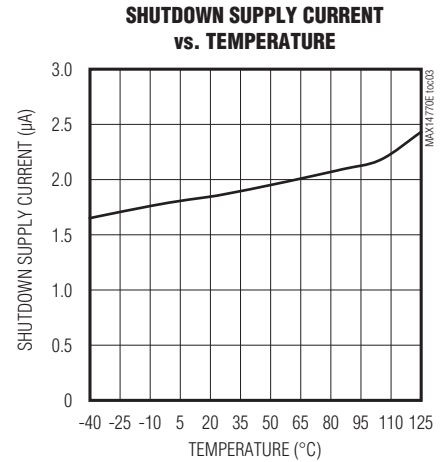
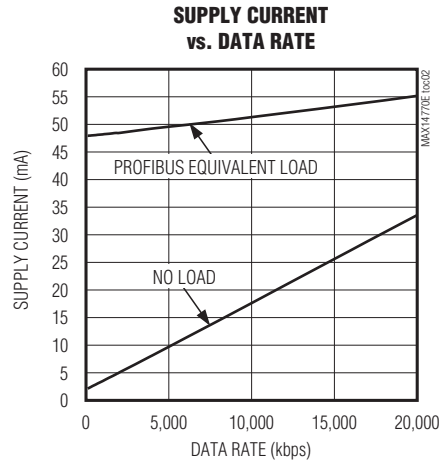
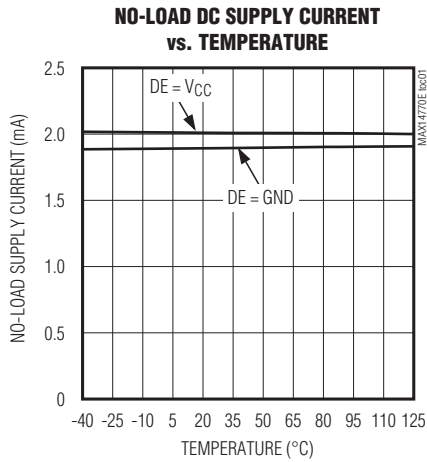
Figure 10. Receiver Enable and Disable Times

MAX14770E

High-ESD Profibus RS-485 Transceiver

Typical Operating Characteristics

($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)

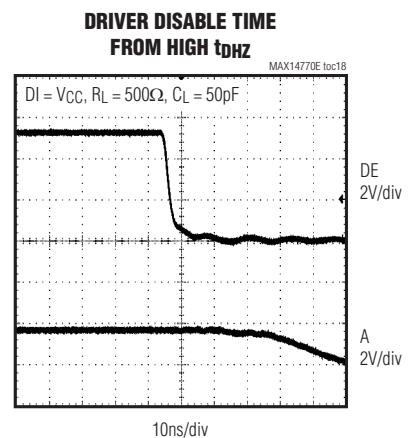
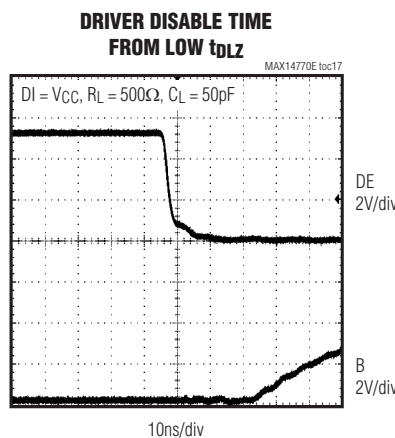
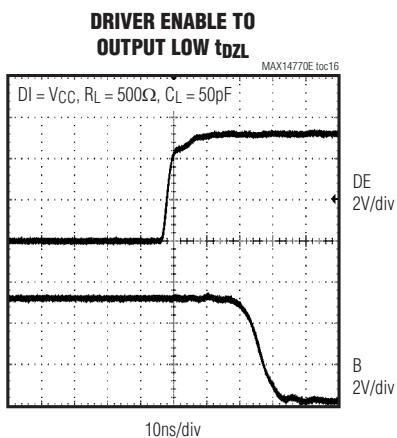
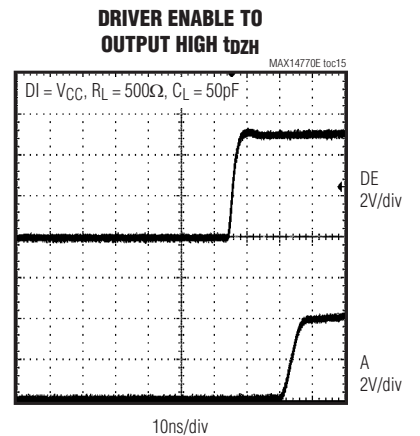
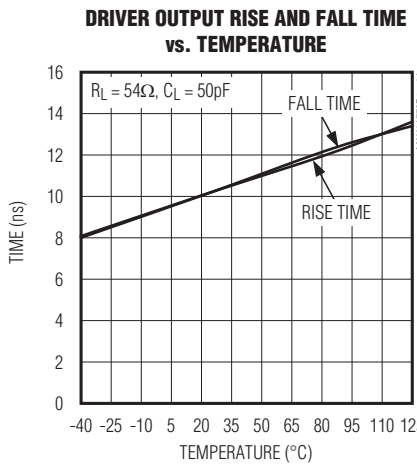
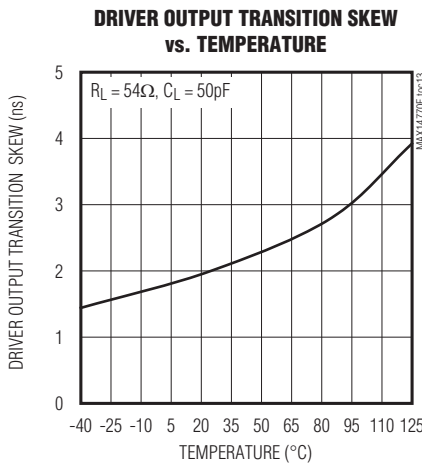
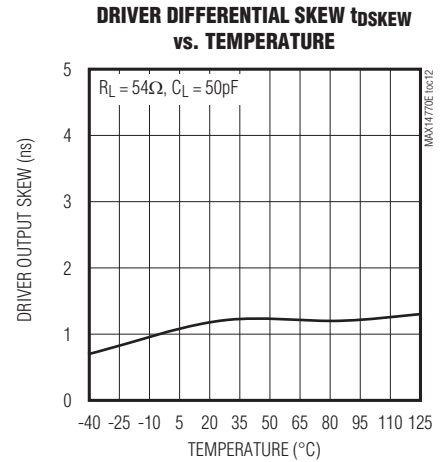
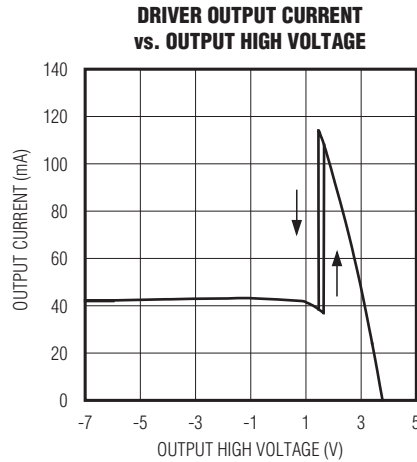
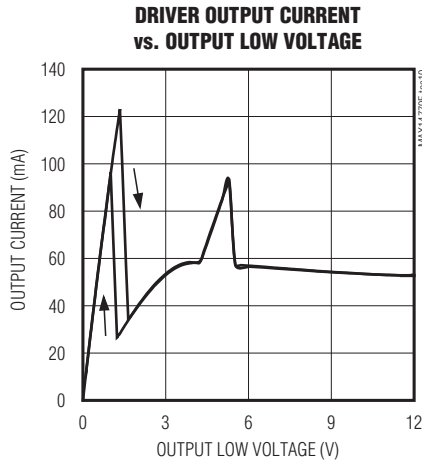


MAX14770E

High-ESD Profibus RS-485 Transceiver

Typical Operating Characteristics (continued)

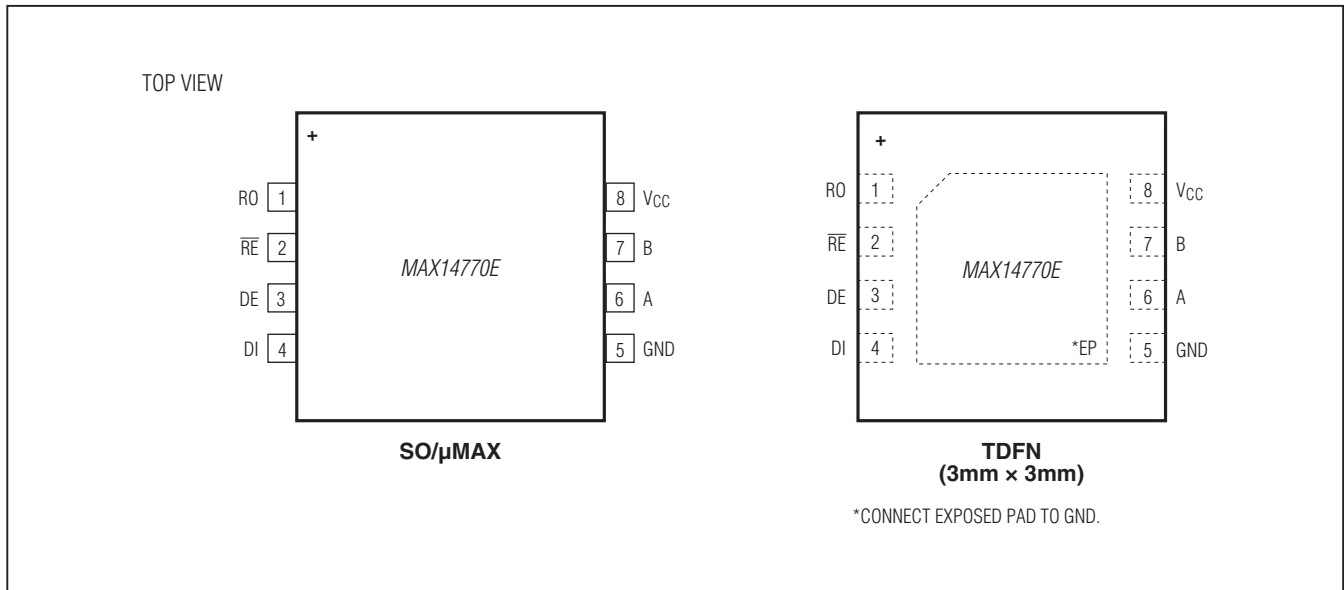
($V_{CC} = +5V$, $T_A = +25^\circ C$, unless otherwise noted.)



MAX14770E

High-ESD Profibus RS-485 Transceiver

Pin Configurations



Pin Description

PIN	NAME	FUNCTION
1	RO	Receiver Output. When \overline{RE} is low and $(A - B) \geq -50\text{mV}$, RO is high; if $(A - B) \leq -200\text{mV}$, RO is low.
2	\overline{RE}	Receiver Enable. Drive \overline{RE} low to enable RO; RO is high impedance when \overline{RE} is high. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
3	DE	Driver Enable. Drive DE high to enable driver output. The driver outputs are high impedance when DE is low. Drive \overline{RE} high and DE low to enter low-power shutdown mode.
4	DI	Driver Input. With DE high, a low on DI forces the noninverting output, A, low and the inverting output, B, high. Similarly, a high on DI forces the noninverting output, A, high and the inverting output, B, low.
5	GND	Ground
6	A	Noninverting Receiver Input and Noninverting Driver Output
7	B	Inverting Receiver Input and Inverting Driver Output
8	VCC	Positive Supply. Bypass VCC to GND with a 0.1μF ceramic capacitor as close as possible to the device.
—	EP	Exposed Pad (TDFN Only). Connect EP to GND.

MAX14770E

High-ESD Profibus RS-485 Transceiver

Detailed Description

The MAX14770E is a half-duplex, $\pm 35\text{kV}$ high ESD-protected transceiver for PROFIBUS-DP, RS-485, and RS-422 communications. The device features true fail-safe circuitry that guarantees a logic-high receiver output when the receiver inputs are open or shorted, or when they are connected to a terminated transmission line with all drivers disabled (see the *True Fail-Safe* section). The MAX14770E supports data rates up to 20Mbps.

The MAX14770E operates from a single +4.5V to +5.5V supply. Drivers are output short-circuit current limited. Thermal-shutdown circuitry protects drivers against excessive power dissipation. When activated, the thermal-shutdown circuitry places the driver outputs into a high-impedance state. The MAX14770E has a hot-swap input structure that prevents disturbances on the differential signal lines when the MAX14770E is powered up (see the *Hot-Swap Capability* section).

True Fail-Safe

The MAX14770E guarantees a logic-high receiver output when the receiver inputs are shorted or open, or when they are connected to a terminated transmission line with all drivers disabled. This is done by having the receiver

threshold between -50mV and -200mV . If the differential receiver input voltage (A - B) is greater than or equal to -50mV , RO is logic-high. If (A - B) is less than or equal to -200mV , RO is logic-low. In the case of a terminated bus with all transmitters disabled, the receiver's differential input voltage is pulled to 0V by the termination. With the receiver thresholds of the MAX14770E, this results in a logic-high with a 50mV minimum noise margin. The -50mV to -200mV threshold complies with the $\pm 200\text{mV}$ EIA/TIA-485 standard.

Hot-Swap Capability

Hot-Swap Inputs

When circuit boards are inserted into a hot or powered backplane, disturbances to the enable inputs and differential receiver inputs can lead to data errors. Upon initial circuit board insertion, the processor undergoes its power-up sequence. During this period, the processor output drivers are high impedance and are unable to drive the DE and $\overline{\text{RE}}$ inputs of the MAX14770E to a defined logic level. Leakage currents up to $10\mu\text{A}$ from the high-impedance output of a controller could cause DE and $\overline{\text{RE}}$ to drift to an incorrect logic state. Additionally, parasitic circuit board capacitance could cause coupling of V_{CC} or GND to DE and $\overline{\text{RE}}$. These factors could improperly enable the driver or receiver. However, the MAX14770E has hot-swap inputs that avoid these potential problems.

When V_{CC} rises, an internal pulldown circuit holds DE low and $\overline{\text{RE}}$ high. After the initial power-up sequence, the pulldown circuit becomes transparent, resetting the hot-swap-tolerable inputs.

Hot-Swap Input Circuitry

The MAX14770E DE and $\overline{\text{RE}}$ enable inputs feature hot-swap capability. At the input, there are two NMOS devices, M1 and M2 (Figure 11). When V_{CC} ramps from 0, an internal $15\mu\text{s}$ timer turns on M2 and sets the SR latch that also turns on M1. Transistors M2, a 1mA current sink, and M1, a $100\mu\text{A}$ current sink, pull DE to GND through a $5.6\text{k}\Omega$ resistor. M2 is designed to pull DE to the disabled state against an external parasitic capacitance up to 100pF that can drive DE high. After $15\mu\text{s}$, the timer deactivates M2 while M1 remains on, holding DE low against three-state leakages that can drive DE high. M1 remains on until an external source overcomes the required input current. At this time, the SR latch resets and M1 turns off. When M1 turns off, DE reverts to a standard, high-impedance CMOS input. Whenever V_{CC} drops below 1V, the hot-swap input is reset.

For $\overline{\text{RE}}$, there is a complementary circuit employing two PMOS devices pulling $\overline{\text{RE}}$ to V_{CC} .

Table 1. Functional Table (Transmitting)

TRANSMITTING				
INPUTS			OUTPUTS	
$\overline{\text{RE}}$	DE	DI	B	A
X	1	1	0	1
X	1	0	1	0
0	0	X	High-Z	High-Z
1	0	X	High-Z and shutdown	

X = Don't care.

Table 2. Functional Table (Receiving)

RECEIVING			
INPUTS			OUTPUT
$\overline{\text{RE}}$	DE	A-B	RO
0	X	$\geq -0.05\text{V}$	1
0	X	$\leq -0.2\text{V}$	0
0	X	Open/shorted	1
1	1	X	High-Z
1	0	X	High-Z and shutdown

X = Don't care.

MAX14770E

High-ESD Profibus RS-485 Transceiver

Thermal-Shutdown Protection

The MAX14770E features thermal-shutdown circuitry. The internal switch turns off when the junction temperature exceeds +160°C (typ) and immediately goes into a fault mode. The device exits thermal shutdown after the junction temperature cools by 15°C (typ).

Applications Information

128 Transceivers on the Bus

The standard RS-485 receiver input impedance is one unit load, and a standard driver can drive up to 32 unit loads. The MAX14770E transceiver has a 1/4 unit load receiver, which allows up to 128 transceivers connected in parallel on one communication line. Connect any combination of these devices, and/or other RS-485 devices, for a maximum of 32 unit loads to the line.

Low-Power Shutdown Mode

Low-power shutdown mode is initiated by bringing both \overline{RE} high and DE low. In shutdown, the devices draw only 15 μ A (max) of supply current. \overline{RE} and DE can be driven simultaneously; the devices are guaranteed not to enter shutdown if \overline{RE} is high and DE is low for less than 50ns. If the inputs are in this state for at least 800ns, the devices are guaranteed to enter shutdown.

Driver Output Protection

Two mechanisms prevent excessive output current and power dissipation caused by faults or by bus contention. The first, a foldback current limit on the output stage, provides immediate protection against short circuits over the whole common-mode voltage range (see the *Typical Operating Characteristics*). The second, a thermal-shutdown circuit, forces the driver outputs into a high-impedance state if the die temperature exceeds +160°C (typ).

Typical Application

The MAX14770E transceivers are designed for bidirectional data communications on multipoint bus transmission lines. Figure 12 shows a typical network applications circuit. To minimize reflections, the line should be terminated at both ends in its characteristic impedance, and stub lengths off the main line should be kept as short as possible.

Profibus Termination

The MAX14770E is designed for driving PROFIBUS-DP termination networks. With a worst-case loading of two termination networks with 220 Ω termination impedance and 390 Ω pullups/pulldowns, the drivers can drive $V(A - B) > 2.1V$ output.

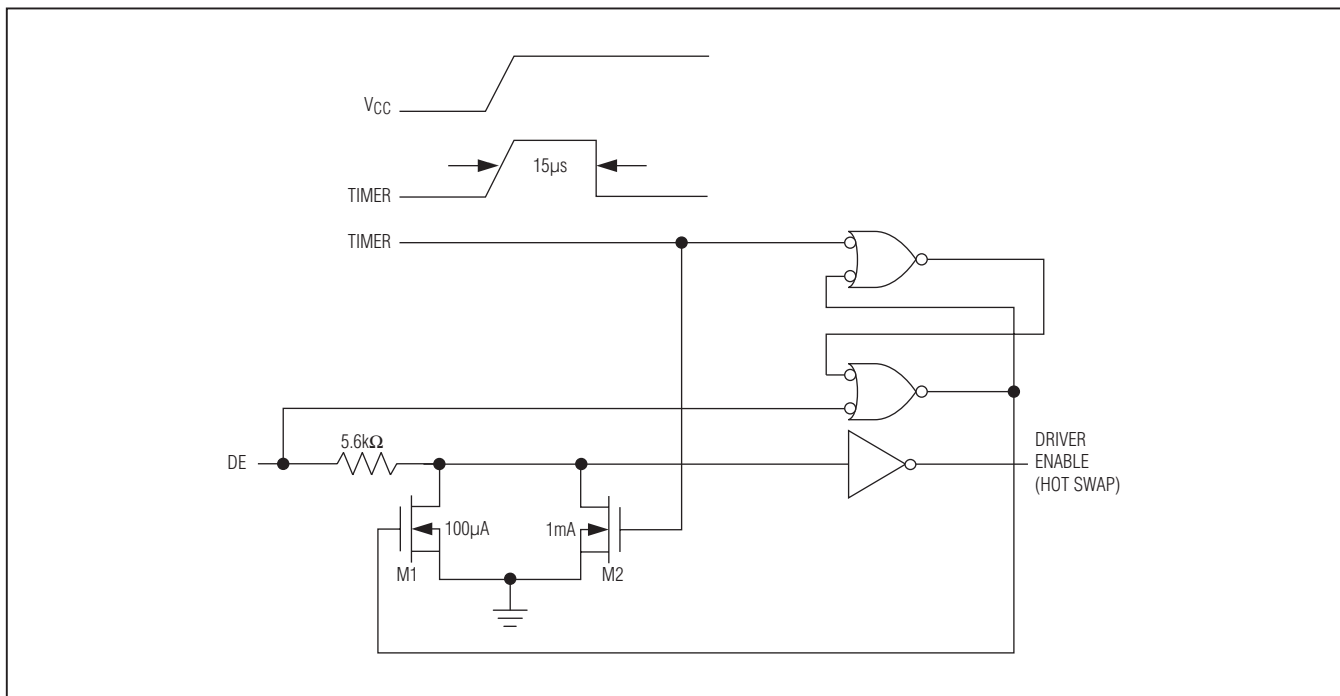


Figure 11. Simplified Structure of the Driver Enable Pin (DE)

MAX14770E

High-ESD Profibus RS-485 Transceiver

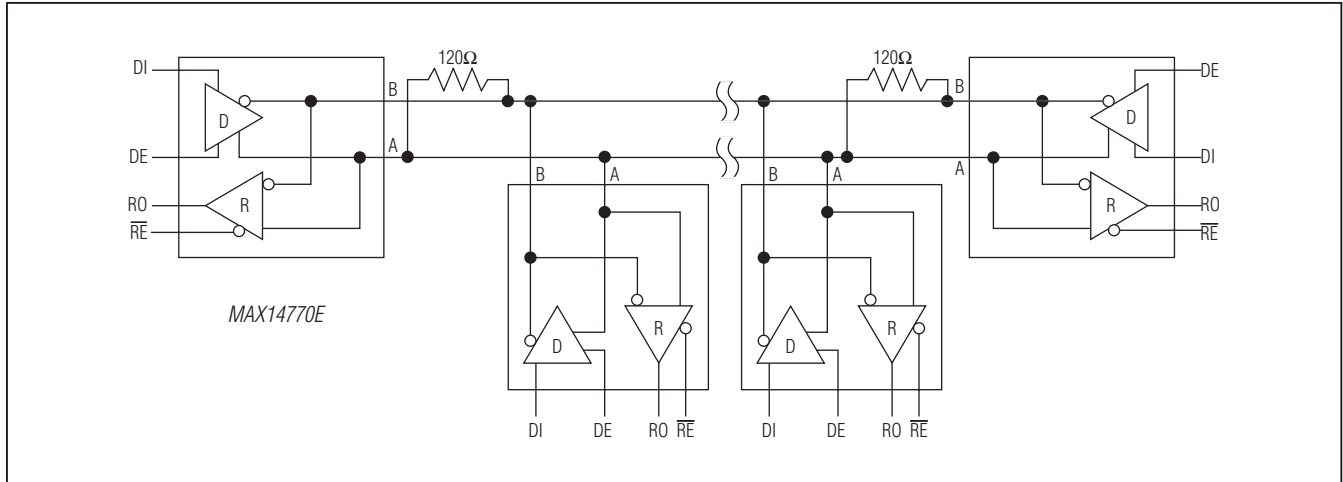


Figure 12. Typical Half-Duplex RS-485 Network

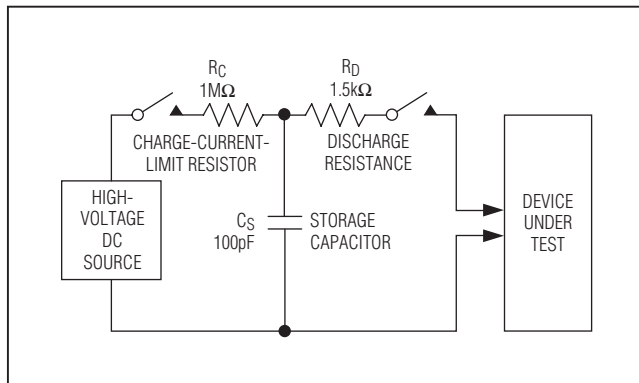


Figure 13. Human Body ESD Test Model

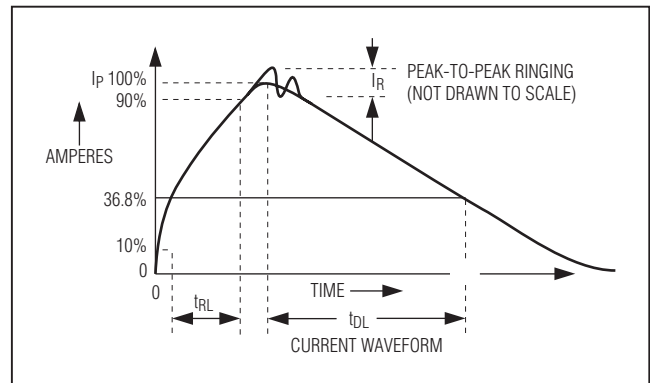


Figure 14. Human Body Current Waveform

Extended ESD Protection

ESD protection structures are incorporated on all pins to protect against electrostatic discharges up to $\pm 2\text{kV}$ (HBM) encountered during handling and assembly. A and B are further protected against high ESD up to $\pm 35\text{kV}$ (HBM) without damage. The A and B pins are also protected against $\pm 20\text{kV}$ Air-Gap and $\pm 10\text{kV}$ Contact IEC61000-4-2 ESD events. The ESD structures withstand high ESD both in normal operation and when the device is powered down. After an ESD event, the MAX14770E continues to function without latchup.

ESD Test Conditions

ESD performance depends on a variety of conditions. Contact Maxim for a reliability report that documents test setup, test methodology, and test results.

Human Body Model

Figure 13 shows the HBM. Figure 14 shows the current waveform it generates when discharged into a low-impedance state. This model consists of a 100pF capacitor charged to the ESD voltage of interest that is then discharged into the device through a $1.5\text{k}\Omega$ resistor.

IEC 61000-4-2

The IEC 61000-4-2 standard covers ESD testing and performance of finished equipment. It does not specifically refer to integrated circuits. The MAX14770E is specified for $\pm 20\text{kV}$ Air-Gap Discharge and $\pm 10\text{kV}$ Contact Discharge IEC 61000-4-2 on the A and B pins.

The main difference between tests done using the HBM and IEC 61000-4-2 is higher peak current in IEC 61000-4-2. Because series resistance is lower in the IEC 61000-4-2

MAX14770E

High-ESD Profibus RS-485 Transceiver

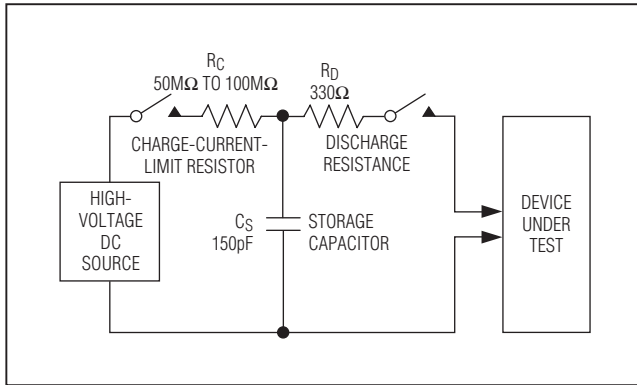


Figure 15. IEC61000-4-2 ESD Test Model

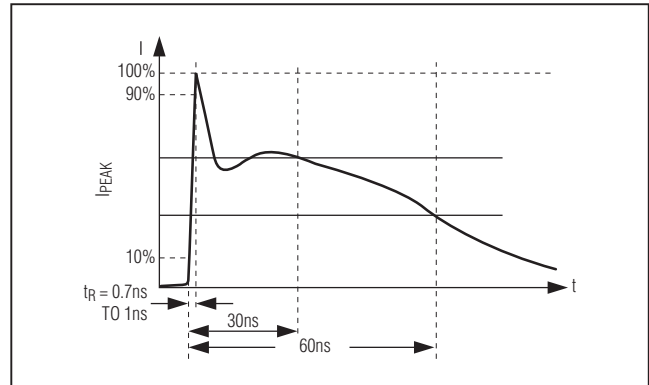
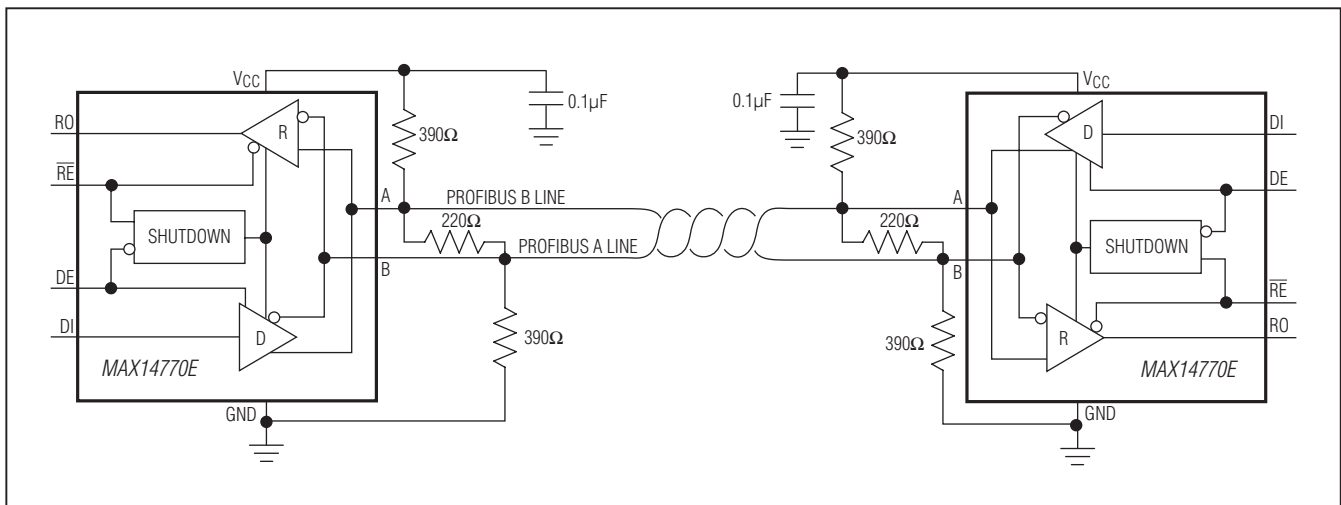


Figure 16. IEC61000-4-2 ESD Generator Current Waveform

Typical PROFIBUS-DP Operating Circuit



ESD test model (Figure 15), the ESD-withstand voltage measured to this standard is generally lower than that measured using the HBM. Figure 16 shows the current waveform for the $\pm 10\text{kV}$ IEC 61000-4-2 Level 4 ESD Contact Discharge test. The Air-Gap Discharge test involves approaching the device with a charged probe. The Contact Discharge method connects the probe to the device before the probe is energized.

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to www.maximintegrated.com/packages. Note that a "+," "#," or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 SO	S8+4	21-0041	90-0096
8 TDFN-EP	T833+2	21-0137	90-0059
8 μ MAX	U8+1	21-0036	90-0092

MAX14770E

High-ESD Profibus RS-485 Transceiver

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/09	Initial release	—
1	4/10	Switched the position of the pins DE and DI (TDFN) in the <i>Pin Configurations</i>	11
2	1/11	Updated logic output specifications, TOC 15, and the <i>Typical PROFIBUS-DP Operating Circuit</i> , added the “Driver Enable High/Low—Propagation Delay Difference” parameters and updated various typical values in the <i>Electrical Characteristics</i> table	3, 4, 10, 15
3	10/12	Added μ MAX and new SOIC packaging to data sheet	1, 2, 11, 15



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[SN65HVD77DGKR](#) [SN65HVD77DGK](#) [SN65HVD76DGSR](#) [SN65HVD71DR](#) [SN65HVD70DR](#) [SN65HVD1477DGKR](#) [SN65HVD1477DGK](#)
[SN65HVD1476DGSR](#) [SN65HVD1473DR](#) [SN65HVD1470DGSR](#) [MAX13450EAUD](#) [MAX13451EAUD](#) [LTC1685CS8#PBF](#)
[LTC1518IS#PBF](#) [LTC1535ISW#PBF](#) [MAX13432EESD+T](#) [MAX13451EAUD+T](#) [MAX14770EESA+T](#) [ADM3065EARMZ](#)
[LTC487CSW#PBF](#) [LTC486ISW](#) [MAX13431EEUB+T](#) [LTC1520CS#PBF](#) [LTC487CN#PBF](#) [LTC1483CS8#PBF](#) [LTC1687IS#PBF](#)
[LTC489IN#PBF](#) [LTC1687CS#PBF](#) [LTC1688IS#PBF](#)