MCP39F501

Single-Phase, Power-Monitoring IC with Calculation and Event Detection

Features:

- Power Monitoring Accuracy capable of 0.1% error across 4000:1 dynamic range
- Fast Calibration Routines
- Programmable Event Notifications such as over-current and voltage sag, surge protection
- 512 bytes User-accessible EEPROM through page read/write commands
- Non-volatile On-chip Memory, no external memory required
- Built-in calculations on fast 16-bit processing core
  - Active, Reactive and Apparent Power
  - True RMS Current, RMS Voltage
  - Line Frequency, Power Factor
- Two-Wire Serial Protocol using a 2-wire Universal Asynchronous Receiver/Transmitter (UART) interface supporting multiple devices on a single bus
- Low-Drift Internal Voltage Reference, 10 ppm/°C typical
- 28-lead 5x5 QFN package
- Extended Temperature Range -40°C to +125°C

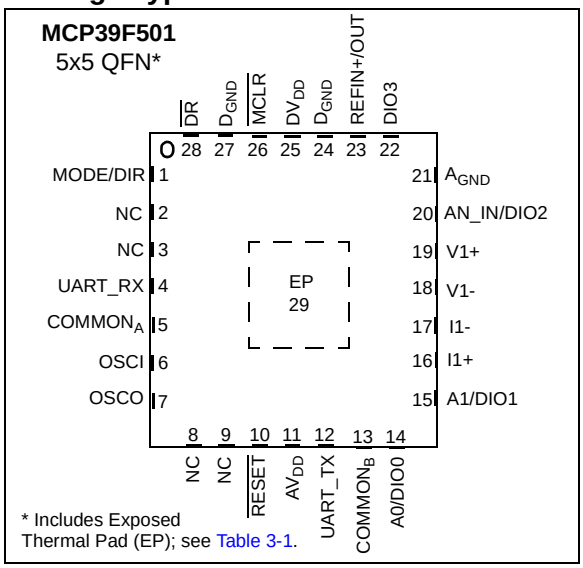
Applications:

- Real-time Measurement of Input Power for AC/DC supplies
- Intelligent Power Distribution Units

Description:

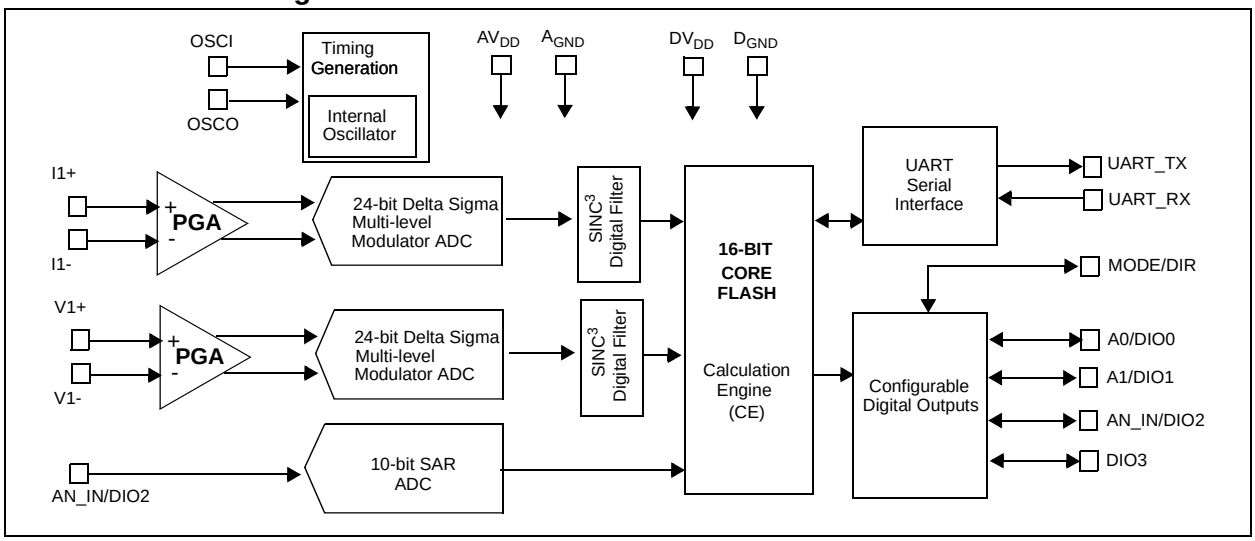
The MCP39F501 is a highly integrated, single-phase power-monitoring IC designed for real-time measurement of input power for AC/DC power supplies, power distribution units and industrial applications. It includes dual-channel delta sigma ADCs, a 16-bit calculation engine, EEPROM and a flexible 2-wire interface. An integrated low-drift voltage reference with 10 ppm/°C in addition to 94.5 dB of SINAD performance on each measurement channel allows for better than 0.1% accurate designs across a 4000:1 dynamic range.

Package Type

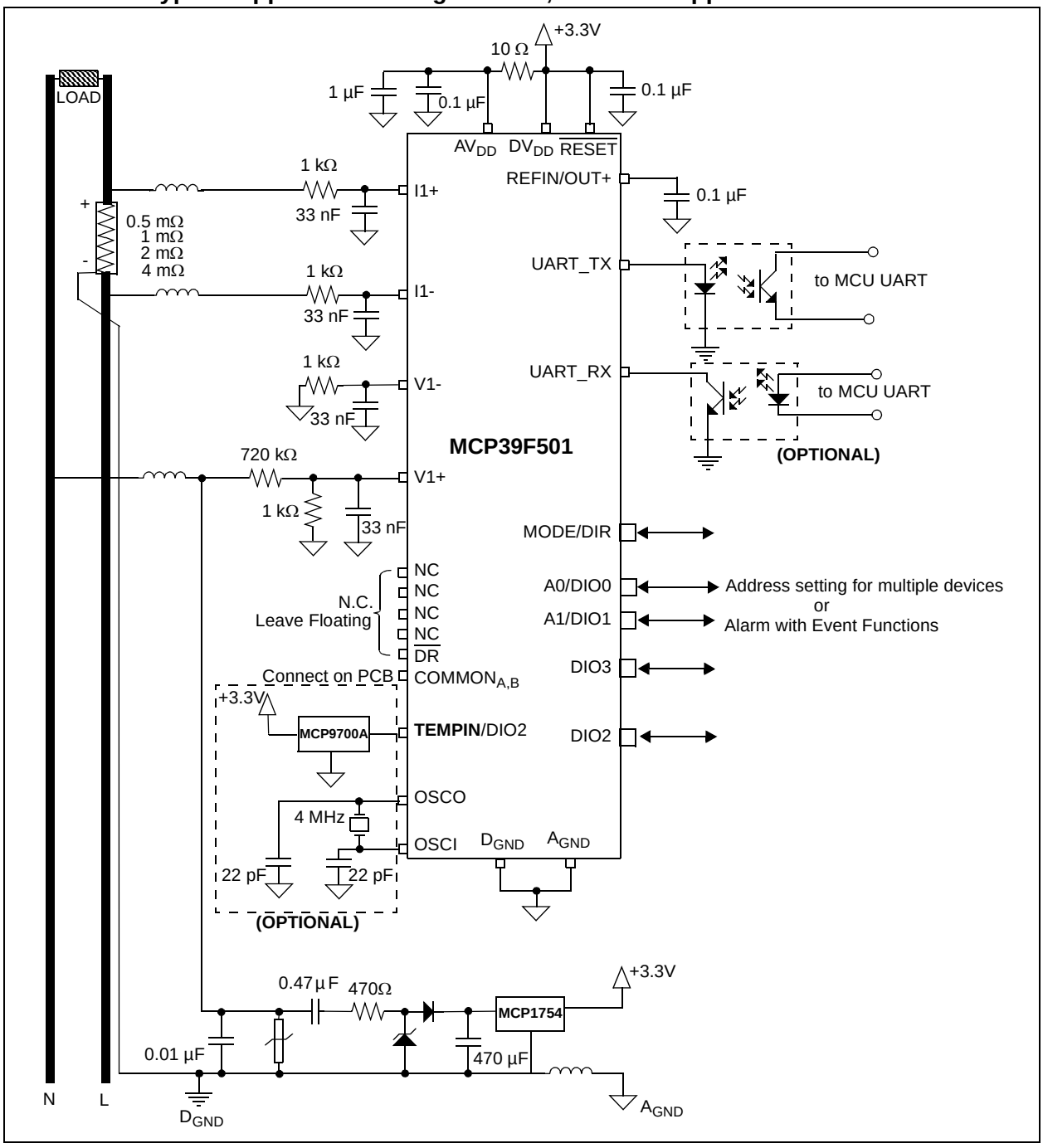


* Includes Exposed Thermal Pad (EP); see Table 3-1.

Functional Block Diagram



MCP39F501 Typical Application – Single Phase, Two-Wire Application Schematic



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

DV_{DD} .....-0.3 to 4.5V
AV_{DD} .....-0.3 to 4.0V
Digital inputs and outputs w.r.t. A_{GND}..... -0.3V to 4.0V
Analog Inputs (I+,I-,V+,V-) w.r.t. A_{GND} ....-2V to +2V
V_{REF} input w.r.t. A_{GND} .....-0.6V to AV_{DD} +0.6V
Maximum Current out of D_{GND} pin.....300 mA
Maximum Current into DV_{DD} pin.....250 mA
Maximum Output Current Sunk by Digital IO.....25 mA
Maximum Current Sourced by Digital IO.....25 mA
Storage temperature .....-65°C to +150°C
Ambient temperature with power applied.....-40°C to +125°C
Soldering temperature of leads (10 seconds) ..... +300°C
ESD on the analog inputs (HBM,MM) .....4.0 kV, 200V
ESD on all other pins (HBM,MM) .....4.0 kV, 200V

† Notice: Stresses above those listed under "Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 Specifications

TABLE 1-1: ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Power Measurement						
Active Power **(Note 2)**	P	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Reactive Power **(Note 2)**	Q	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Apparent Power **(Note 2)**	S	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Current RMS **(Note 2)**	I_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Current Channel **(Note 1)**
Voltage RMS **(Note 2)**	V_{RMS}	—	±0.1	—	%	4000:1 Dynamic Range on Voltage Channel **(Note 1)**
Power Factor **(Note 2)**	Φ	—	±0.1	—	%	
Line Frequency **(Note 2)**	V_{RMS}	—	±0.1	—	%	
Calibration, Calculation and Event Detection Times						
Auto-Calibration Time	t_{CAL}	—	2^N x ($1/f_{LINE}$)	—	ms	**Note 7**
Minimum Calculation and Event Detection Time	t_{CALC_EVENT}	2^N x ($1/f_{LINE}$)	—	—	ms	
Minimum Time for Voltage Sag Detection	t_{AC_DROP}	—	see **Section 7.7**	—	ms	**Note 4**

Note 1: Specification by design and characterization; not production tested.
2: Calculated from reading the register values.
3: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.
4: Applies to Voltage Sag and Voltage Surge Events Only.
5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.
6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.
7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
24-Bit Delta Sigma ADC Performance						
Analog Input Absolute Voltage	V_{IN}	-1	—	+1	V	
Analog Input Leakage Current	A_{IN}	—	1	—	nA	
Differential Input Voltage Range	(I1+ – I1-), (V1+ – V1-)	-600/GAIN	—	+600/GAIN	mV	V_{REF} = 1.2V, proportional to V_{REF}
Offset Error	V_{OS}	-1	—	+1	mV	
Offset Error Drift		—	0.5	—	µV/°C	
Gain Error	GE	-4	—	+4	%	**Note 6**
Gain Error Drift		—	1	—	ppm/°C	
Differential Input Impedance	Z_{IN}	232	—	—	kΩ	G = 1
		142	—	—	kΩ	G = 2
		72	—	—	kΩ	G = 4
		38	—	—	kΩ	G = 8
		36	—	—	kΩ	G = 16
		33	—	—	kΩ	G = 32
Signal-to-Noise and Distortion Ratio	SINAD	92	94.5	—	dB	**Note 3**
Total Harmonic Distortion	THD	—	-106.5	-103	dBc	**Note 3**
Signal-to-Noise Ratio	SNR	92	95	—	dB	**Note 3**
Spurious Free Dynamic Range	SFDR	—	111	—	dB	**Note 3**
Crosstalk	CTALK	—	-122	—	dB	
AC Power Supply Rejection Ratio	AC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.3V + 0.6V_{PP}, 100 Hz, 120 Hz, 1 kHz
DC Power Supply Rejection Ratio	DC PSRR	—	-73	—	dB	AV_{DD} and DV_{DD} = 3.0 to 3.6V
DC Common Mode Rejection Ratio	DC CMRR	—	-105	—	dB	V_{CM} varies from -1V to +1V
10-Bit SAR ADC Performance for Temperature Measurement						
Resolution	N_R	—	10	—	bits	
Absolute Input Voltage	V_{IN}	D_{GND} - 0.3	—	D_{GND} + 0.3	V	
Recommended Impedance of Analog Voltage Source	R_{IN}	—	—	2.5	kΩ	
Integral Non-Linearity	I_{NL}	—	±1	±2	LSb	

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: V_{IN} = 1V_{PP} = 353 mV_{RMS} @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.

Characteristic	Sym.	Min.	Typ.	Max.	Units	Test Conditions
Differential Non-Linearity	D_{NL}	—	±1	±1.5	LSb	
Gain Error	G_{ERR}	—	±1	±3	LSb	
Offset Error	E_{OFF}	—	±1	±2	LSb	
Temperature Measurement Rate		—	$f_{LINE}/2^N$	—	sps	**Note 7**
Clock and Timings						
UART Baud Rate	UDB	—	4.8	—	kbps	See **Section 3.2** for protocol details
Master Clock and Crystal Frequency	f_{MCLK}	-2%	4	+2%	MHz	
Capacitive Loading on OSCO pin	COSC2	—	—	15	pF	When an external clock is used to drive the device
Internal Oscillator Tolerance	f_{INT_OSC}	—	2	—	%	-40 to +85°C only (**Note 5**)
Internal Voltage Reference						
Internal Voltage Reference Tolerance	V_{REF}	-2%	1.2	+2%	V	
Temperature Coefficient	TCV_{REF}	—	10	—	ppm/°C	T_A = -40°C to +85°C, VREFEXT = 0
Output Impedance	$ZOUTV_{REF}$	—	2	—	kΩ	
Current, V_{REF}	$AI_{DD}V_{REF}$	—	40	—	µA	
Voltage Reference Input						
Input Capacitance		—	—	10	pF	
Absolute Voltage on V_{REF+} Pin	V_{REF+}	A_{GND} + 1.1V	—	A_{GND} + 1.1V	V	
Power Specifications						
Operating Voltage	AV_{DD}, DV_{DD}	2.7	—	3.6	V	
DV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	D_{GND}	—	0.7	V	
DV_{DD} Rise Rate to Ensure Internal Power-On Reset Signal	SDV_{DD}	0.05	—	—	V/ms	0 – 3.3V in 0.1s, 0 – 2.5V in 60 ms
AV_{DD} Start Voltage to Ensure Internal Power-On Reset Signal	V_{POR}	A_{GND}	—	2.1	V	
AV_{DD} Rise Rate to Ensure Internal Power On Reset Signal	SAV_{DD}	0.042	—	—	V/ms	0 – 2.4V in 50 ms

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: V_{IN} = $1V_{PP}$ = 353 mV_{RMS} @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

TABLE 1-1: ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz, PGA GAIN = 1.						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
Operating Current	I_{DD}	—	13	—	mA	
Data EEPROM Memory						
Cell Endurance	EPS	100,000	—	—	E/W	
Self-Timed Write Cycle Time	T_{IWD}	—	4	—	ms	
Number of Total Write/Erase Cycles Before Refresh	R_{REF}	—	10,000,000	—	E/W	
Characteristic Retention	T_{RETDD}	40	—	—	Years	Provided no other specifications are violated
Supply Current during Programming	I_{DDPD}	—	7	—	mA	

Note 1: Specification by design and characterization; not production tested.

2: Calculated from reading the register values.

3: $V_{IN} = 1V_{PP} = 353\ mV_{RMS}$ @ 50/60 Hz.

4: Applies to Voltage Sag and Voltage Surge Events Only.

5: Variation applies to internal clock and UART only. All calculated output quantities are temperature compensated to the performance listed in the respective specification.

6: Applies to all gains. Offset and gain errors depend on the PGA gain setting. See **Section 2.0 "Typical Performance Curves"** for typical performance.

7: N = Value in the AccumulationInternalParameter register (0x005A). The default value of this register is 2 or T_{CAL} = 80 ms for 50 Hz line.

TABLE 1-2: SERIAL DC CHARACTERISTICS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6 V, T_A = -40°C to +125°C, MCLK = 4 MHz						
Characteristic	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Test Conditions**
High-Level Input Voltage	V_{IH}	0.8 DV_{DD}	—	DV_{DD}	V	
Low-Level Input Voltage	V_{IL}	V_{SS}	—	0.2 V_{SSD}	V	
High-Level Output Voltage	V_{OH}	3	—	—	V	I_{OH} = -3.0 mA, V_{DD} = 3.6V
Low-Level Output Voltage	V_{OL}	—	—	0.4	V	I_{OL} = 4.0 mA, V_{DD} = 3.6V
Input Leakage Current	I_{LI}	—	—	1	µA	
		—	0.050	0.100	µA	DIO pins only

TABLE 1-3: TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise indicated, all parameters apply at AV_{DD}, DV_{DD} = 2.7 to 3.6V.						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, 28LD 5x5 QFN	θ_{JA}	—	35.3	—	°C/W	

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

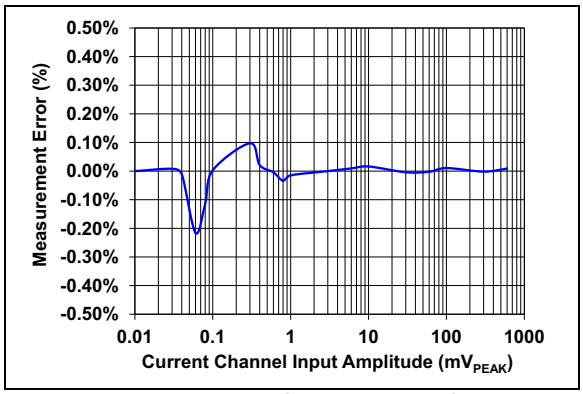


FIGURE 2-1: *Active Power, Gain = 1.*

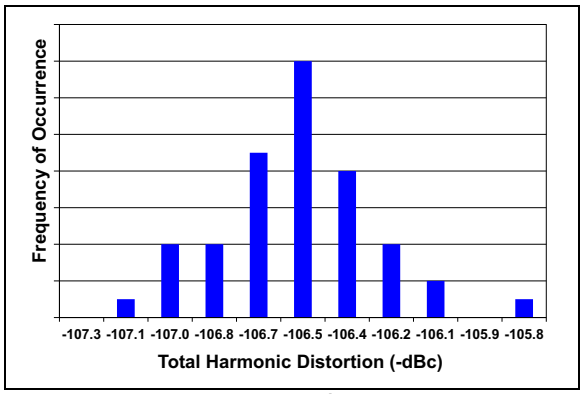


FIGURE 2-4: *THD Histogram.*

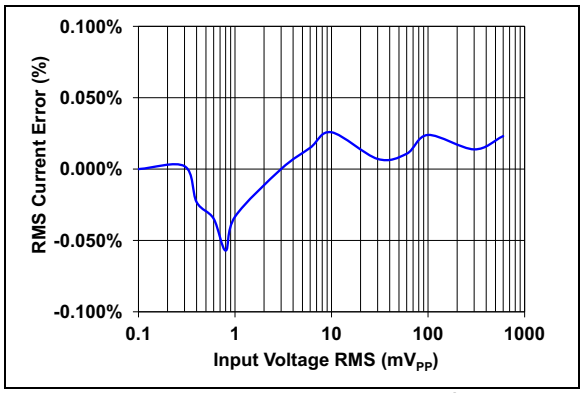


FIGURE 2-2: *RMS Current, Gain = 1.*

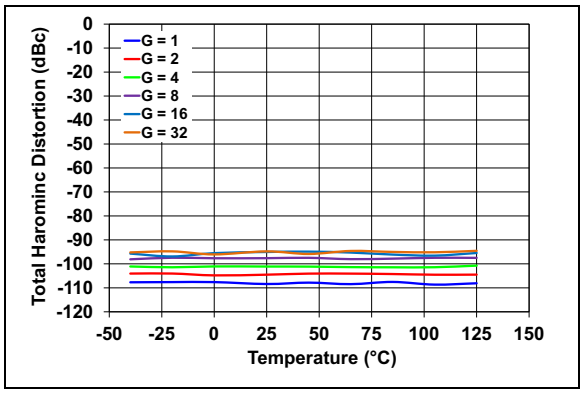


FIGURE 2-5: *THD vs. Temperature.*

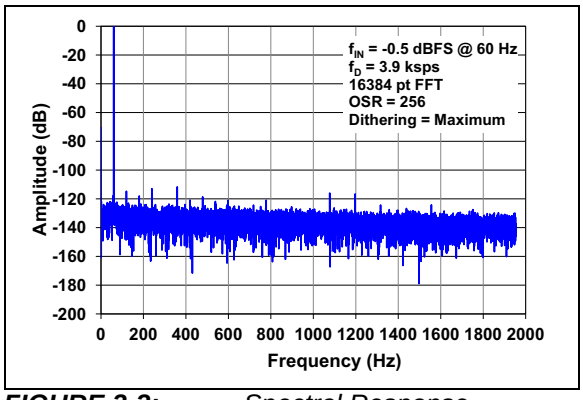


FIGURE 2-3: *Spectral Response.*

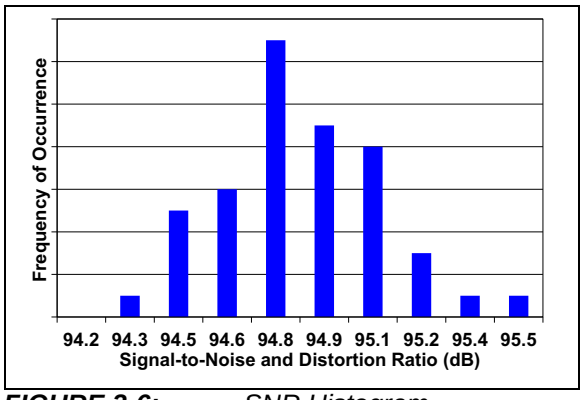


FIGURE 2-6: *SNR Histogram.*

Note: Unless otherwise indicated, AV_{DD} = 3.3V, DV_{DD} = 3.3V, T_A = +25°C, GAIN = 1, V_{IN} = -0.5 dBFS at 60 Hz.

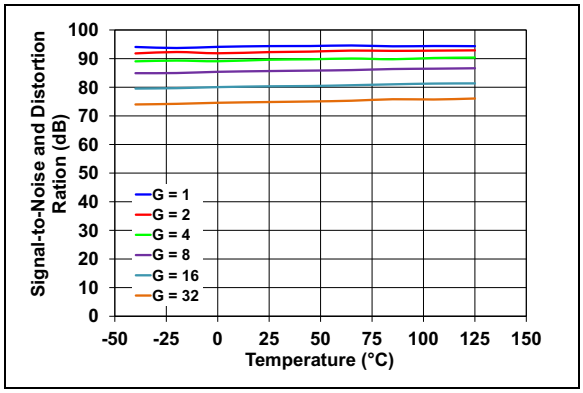


FIGURE 2-7: *SINAD vs. Temperature.*

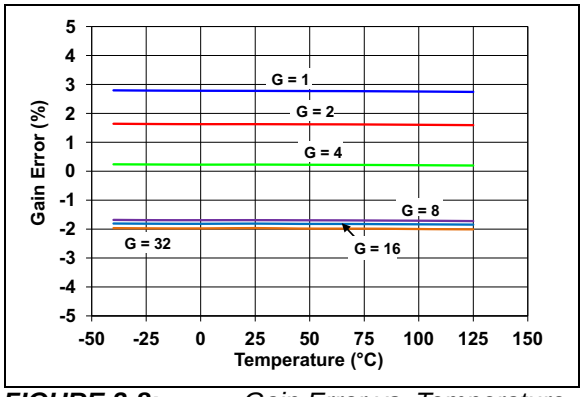


FIGURE 2-8: *Gain Error vs. Temperature.*

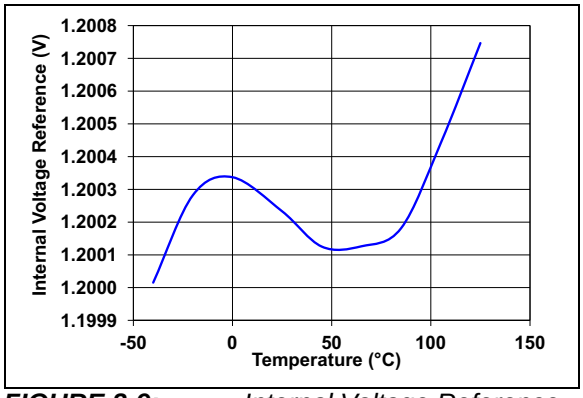


FIGURE 2-9: *Internal Voltage Reference vs. Temperature.*

3.0 PIN DESCRIPTION

The description of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP39F501 5x5 QFN	Symbol	Function
1	MODE/DIR	Single or Multiple Device mode with direction control for RS-485 drivers
2	NC	No Connect (must be left floating)
3	NC	No Connect (must be left floating)
4	UART_RX	UART Communication RX Pin
5	$COMMON_A$	Common pin A, to be connected to $COMMON_B$
6	OSCI	Oscillator Crystal Connection Pin or External Clock Input Pin
7	OSCO	Oscillator Crystal Connection Pin
8	NC	No Connect (must be left floating)
9	NC	No Connect (must be left floating)
10	$\overline{RESET}$	Reset Pin for Delta Sigma ADCs
11	AV_{DD}	Analog Power Supply Pin
12	UART_TX	UART Communication TX Pin
13	$COMMON_B$	Common pin B, to be connected to $COMMON_A$
14	A0/DIO0	Address Select Pin 0 / Configurable digital I/O 0
15	A1/DIO1	Address Select Pin 1 / Configurable digital I/O 1
16	I1+	Non-Inverting Current Channel Input for 24-bit ΔΣ ADC
17	I1-	Inverting Current Channel Input for 24-bit ΔΣ ADC
18	V1-	Inverting Voltage Channel Input for 24-bit ΔΣ ADC
19	V1+	Non-Inverting Voltage Channel Input for 24-bit ΔΣ ADC
20	AN_IN/DIO2	Analog Input for SAR ADC / Configurable Digital Input/Output 2 Pin
21	A_{GND}	Analog Ground Pin, Return Path for internal analog circuitry
22	DIO3	Configurable Digital Input/Output 3
23	REFIN+/OUT	Non-Inverting Voltage Reference Input and Internal Reference Output Pin
24	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
25	DV_{DD}	Power Supply Pin
26	$\overline{MCLR}$	Master Clear for Device
27	D_{GND}	Digital Ground Pin, Return Path for internal digital circuitry
28	$\overline{DR}$	Data Ready (must be left floating)
29	EP	Exposed Thermal Pad (to be connected to D_{GND})

3.1 Single/Multiple Device Mode and Direction Pin (MODE/DIR)

When using multiple devices on a single bus, this pin should be tied to the DIR pin of the transceiver for direction control. This will cause the A0/DIO0 and A1/DIO1 pins to act as address pins A0,A1. If additional devices are required, the Device Address register can be programmed to allow for more than four devices. For this operation, a 4.7 kΩ pull-down resistor should be connected to this pin.

If only a single device is being used, the MODE pin should be driven high at power-on reset (POR), making the A0/DIO0 and A1/DIO1 pins additional configurable digital I/O (DIO).

3.2 UART Communication Pins (UART_TX, UART_RX)

The MCP39F501 device contains an asynchronous full-duplex UART. The UART communication is 8 bits with Start and Stop bit. See **Section 4.2 "UART Settings"** for more information.

3.3 Common Pins (COMMON A and B)

The $COMMON_A$ and $COMMON_B$ pins are internal connections for the MCP39F501. These two pins should be connected together in the application.

3.4 Data Ready Pin ($\overline{DR}$)

The data ready pin indicates if a new delta-sigma A/D conversion result is ready to be processed. This pin is for indication only and should be left floating. After each conversion is finished, a low pulse will take place on the Data Ready pin to indicate the conversion result is ready and an interrupt is generated in the calculation engine (CE). This pulse is synchronous with line frequency and has a predefined and constant width.

Note:	This pin is internally connected to the IRQ of the calculation engine and should be left floating.

3.5 Oscillator Pins (OSCO/OSCI)

OSCO and OSCI provide the master clock for the device. Appropriate load capacitance should be connected to these pins for proper operation. An optional 4 MHz crystal can be connected to these pins. If a crystal of external clock source is not detected, the device will clock from the internal 4 MHz oscillator.

3.6 Reset Pin ($\overline{RESET}$)

This pin is active-low and places the delta-sigma ADCs, PGA, internal V_{REF} and other blocks associated with the analog front-end in a reset state when pulled low. This input is Schmitt-triggered.

3.7 Analog Power Supply Pin (AV_{DD})

AV_{DD} is the power supply pin for the analog circuitry within the MCP39F501.

This pin requires appropriate bypass capacitors and should be maintained to 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.8 Digital Power Supply Pin (DV_{DD})

DV_{DD} is the power supply pin for the digital circuitry within the MCP39F501. This pin requires appropriate bypass capacitors and should be maintained between 2.7V and 3.6V for specified operation. It is recommended to use 0.1 µF ceramic capacitors.

3.9 Configurable Digital Input/Output Pins (DIOn)

These digital I/O pins can be configured to act as input or as output events, such as alarm events or interrupt flags, based on the device configuration. For more information, see **Section 8.0 "Configurable Digital I/O Pins (DIO Configuration – 0x0046)"**.

3.10 24-Bit Delta Sigma ADC Differential Current Channel Input Pins (I1+/I1-)

I1- and I1+ are the two fully-differential current channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each In+/- input pin is ±1V with no distortion and ±6V with no breaking after continuous voltage.

3.11 24-Bit Delta Sigma ADC Differential Voltage Channel Inputs (V1+/V1-)

V1- and V1+ are the two fully-differential voltage channel inputs for the Delta-Sigma ADCs.

The linear and specified region of the channels are dependent on the PGA gain. This region corresponds to a differential voltage range of ±600 mV_{PEAK}/GAIN with V_{REF} = 1.2V.

The maximum absolute voltage, with respect to A_{GND}, for each V_N+/- input pin is ±1V with no distortion and ±6V, with no breaking after continuous voltage.

3.12 Analog Input for Temperature Measurement/Configurable Digital Output 2 Pin (AN_IN/DIO2)

This is the input to the analog-to-digital converter to be used for temperature measurement. If temperature sensing is required in the application, it is advised to connect the low-power active thermistor IC™ MCP9700A to this pin.

3.13 Analog Ground Pin (A_{GND})

A_{GND} is the ground connection to internal analog circuitry (ADCs, PGA, voltage reference, POR). If an analog ground pin is available on the PCB, it is recommended that this pin be tied to that plane.

3.14 Non-inverting Reference Input/Internal Reference Output Pin (REFIN+/OUT)

This pin is the non-inverting side of the differential voltage reference input for the delta sigma ADCs or the internal voltage reference output.

For optimal performance, bypass capacitances should be connected between this pin and A_{GND} at all times, even when the internal voltage reference is used. However, these capacitors are not mandatory to ensure proper operation.

3.15 Digital Ground Connection Pins (D_{GND})

D_{GND} is the ground connection to internal digital circuitry (SINC filters, oscillator, serial interface). If a digital ground plane is available, it is recommended to tie this pin to the digital plane of the PCB. This plane should also reference all other digital circuitry in the system.

3.16 Exposed Thermal Pad (EP)

This pin is the exposed thermal pad. It must be connected to D_{GND}.

NOTES:

4.0 COMMUNICATION PROTOCOL

The communication protocol for the MCP39F501 device is based on the Simple Sensor Interface (SSI) protocol. This protocol is used for point-to-point communication from a single-host MCU to a single-slave MCP39F501. The protocol supports the ability for multiple devices to be on a single bus, but it is only designed to communicate to one device at a time.

All communication to the device occurs in frames. Each frame consists of a header byte, the number of bytes in the frame, command packet (or command packets) and a checksum.

Note:	If a custom communication protocol is desired, please contact a Microchip sales office.

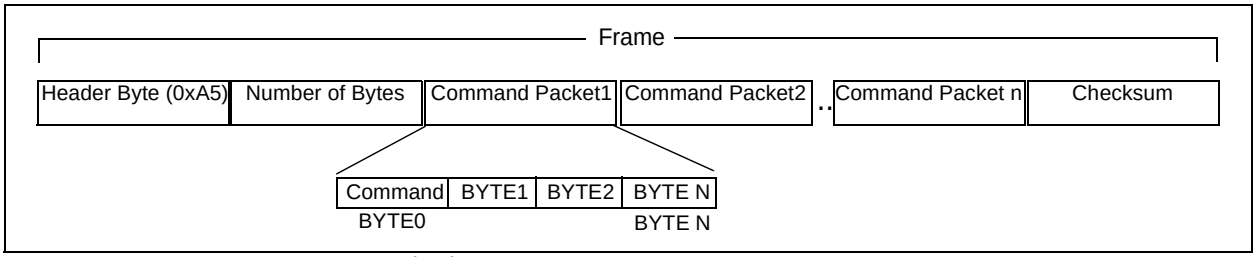


FIGURE 4-1: *MCP39F501 Communication Frame.*

This approach allows for single, secure transmission from the host processor to the MCP39F501 with either a single command, or multiple commands. No command in a frame is processed until the frame is complete and the checksum and number of bytes are validated.

The number of bytes in an individual *command packet* depends on the specific command. For example, to set the instruction pointer, three bytes are needed in the packet: the command byte and two bytes for the address you want to set to the pointer. The first byte in a command packet is always the command byte.

This protocol can also be used to set up transmission from the MCP39F501 on specific registers. A predetermined single-wire transmission frame is defined for one wire interfaces. The Auto-transmit mode can be initiated by setting the SINGLE_WIRE bit in the System Configuration register, allowing for single-wire communication within the application. See **Section 4.9 "Single-Wire Transmission Mode"** for more information on this communication.

4.1 Checksum

The checksum is generated using simple byte addition and taking modulus to find the remainder after dividing the sum of the entire frame by 256. This operation is done to obtain an 8-bit checksum. All the bytes of the frame are included in the checksum, including the header byte and number of bytes. If a frame includes multiple command packets, none of the commands will be issued if the frame checksum fails. In this instance, the MCP39F501 will respond with a CSFAIL response of 0x51.

On commands that are requesting data back from the MCP39F501, the frame and checksum are created in the same way, with the header byte becoming an acknowledge (0x06). Communication examples are given in **Section 4.6 "Example Communication Frames and MCP39F501 Responses"**.

4.2 UART Settings

The default baud rate is 4.8 kbps. The UART operates in 8-bit mode, plus one start bit and one stop bit, for a total of 10 bits per byte, as shown in Figure 4-1.

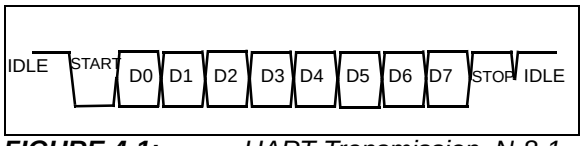


FIGURE 4-1: *UART Transmission, N-8-1.*

The baud rate is fixed at 4.8 kbps.

4.3 Multiple Devices

In order to support multiple devices on a single bus, a device must be selected before any communication occurs between the host MCU and the individual MCP39F501 devices using the `Select Device` command. Once selected, the device will assert the DIR pin until it is deselected.

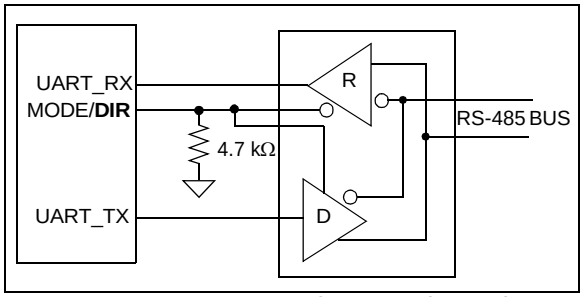


FIGURE 4-2: *DIR Pin Operation Using Example RS-485 Bus Transceiver.*

Based on this operation, the sequence of events when communicating to an MCP39F501 on a bus with multiple devices must be as follows:

1. Select the device.
2. Communicate to selected device through a communication frame.
3. Repeat **Step 2**, if necessary.
4. De-select the device.

4.4 Device Address

A device is selected by issuing the `Select Device` command, followed by the appropriate Device Address. The device address is set through the A0, A1 pins and also through the writing of the Device Address register (Location 0x0026), as shown in Figure 4-3.

A7	A6	A5	A4	A3	A2	A1	A0
Set through Register Write						A1, A0 pins	

FIGURE 4-3: *Device Address Register.*

The default address and default register value is **0x4C.** If the device is in Multiple Device mode (MODE/DIR = `0` at POR), pins A1 and A0 will override bits 0 and 1 and initial possible addresses include 0x4C, 0x4D, 0x4E and 0x4F depending on the state of these pins.

4.5 Command List

The following table is a list of all accepted command bytes for the MCP39F501.

TABLE 4-1: MCP39F501 INSTRUCTION SET

Command	Command ID	Instruction Parameter	Number of Bytes in Command Packet	Successful Response UART_TX
`Register Read, 16 bits`	0x52	---------	1	ACK, Data, CRC
`Register Read, 32 bits`	0x44	---------	1	ACK, Data, CRC
`Register Write, 16 bits`	0x57	Data	3	ACK
`Register Write, 32 bits`	0x45	Data	5	ACK
`Register Read, N bits`	0x4E	Number of Bytes	2	ACK, Data, CRC
`Register Write, N bits`	0x4D	Number of Bytes	1+N	ACK
`Select Device`	0x4C	Device Address	2	ACK
`De-Select Device`	0x4B	Device Address	2	ACK
`Set Address Pointer`	0x41	ADDRESS	3	ACK
`Save Registers To Flash`	0x53	Device Address	2	ACK
`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, CRC
`Page Write EEPROM`	0x50	PAGE	18	ACK
`Bulk Erase EEPROM`	0x4F	Device Address	2	ACK
`Auto-Calibration Gain`	0x5A	Device Address	**Note 1**	
`Auto-Calibration Reactive Gain`	0x7A	Device Address	**Note 1**	
`Auto-Calibration Frequency`	0x76	Device Address	**Note 1**	

Note 1: See **Section 9.0, MCP39F501 Calibration** for more information on calibration.

4.6 Example Communication Frames and MCP39F501 Responses

TABLE 4-2: FRAME EXAMPLE, SELECT DEVICE COMMAND

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x05	Number of Bytes		
0x4C	Command (Select Device)		
0x4D	Device Address		
0x42	Checksum		

TABLE 4-3: FRAME EXAMPLE, READ-16 COMMAND

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x07	Number of Bytes	0x05	Number of Bytes
0x41	Command (Set Address Pointer)	0x00	Data Byte
0x00	Address0	0x4D	Data Byte
0x54	Address1	0x58	Checksum
0x52	Command (Read 16)		
0x93	Checksum		

TABLE 4-4: FRAME EXAMPLE, BULK ERASE EEPROM

Transmit Frame		Response from MCP39F501	
0xA5	Header Byte	0x06	Acknowledge
0x05	Number of Bytes		
0x4F	Command (Bulk Erase EE)		
0x4D	Device Address		
0x46	Checksum		

4.7 Command Descriptions

4.7.1 REGISTER READ, 16-BIT (0X52)

The `Register Read, 16-bit` command, returns the two bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. With this command the data is returned MSB first.

4.7.2 REGISTER READ, 32-BIT (0X44)

The `Register Read, 32-bit` command, returns the four bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. With this command data is returned MSB first.

4.7.3 REGISTER WRITE, 16-BIT (0X57)

The `Register Write, 16-bit` command is followed by bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command.

4.7.4 REGISTER WRITE, 32-BIT (0X45)

The `Register Write, 32-bit` command is followed by four bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command.

4.7.5 REGISTER READ, N BIT (0X4M)

The `Register Read, N-bit` command returns the N bytes that follow whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other read commands. An acknowledge, data and checksum is the response for this command. The maximum number of bytes that can be read with this command is 48. If there are other read commands within a frame, the maximum number of bytes that can be read is 48 minus the number of bytes being read in the frame. With this command, the data is returned LSB first.

4.7.6 REGISTER WRITE, N BIT (0X4D)

The `Register Write, N-bit` command is followed by N bytes that will be written to whatever the current address pointer is set to. It should typically follow a `Set Address Pointer` command. It can be used in conjunction with other write commands. An acknowledge is the response for this command. The maximum number of bytes that can be written with this command is 64. If there are other write commands within a frame, the maximum number of bytes that can be written is 64 minus the number of bytes being written in the frame

4.7.7 SELECT DEVICE (0X4C)

The `Select Device` command is used to drive the direction of the bus in Multiple Device mode by asserting the MODE/**DIR** pin. When the device is in Single Device mode, this command has no effect on the state of the pin. This command is expecting the device address as the command parameter, or the following byte. The device address is a single byte length. If the device address sent with this command matches the value in the MCP39F501's Device Address register, the pin will be asserted and an acknowledge returned.

4.7.8 DE-SELECT DEVICE (0X4B)

The `Select Device` command is used to drive the direction of the bus by deasserting the MODE/**DIR** pin. When the device is in Single Device mode, this command has no effect on the state of the pin. This command is expecting the Device Address as the command parameter, which is the following byte. The Device Address is a single byte length. If the device address sent with this command matches the value in the MCP39F501's Device Address register, the pin will be deasserted and an acknowledge returned.

4.7.9 SET ADDRESS POINTER (0X41)

This command is used to set the address pointer for all read and write commands. This command is expecting the address pointer as the command parameter in the following two bytes. The address pointer is two bytes in length. If the address pointer is within the acceptable addresses of the device, an acknowledge will be returned.

4.7.10 SAVE REGISTERS TO FLASH (0X53)

The `Save Registers To Flash` command makes a copy of all the calibration and configuration registers to flash. This includes all R/W registers in the register set. This command is expecting the device address as the instruction parameter, or the following byte. The device address is a single byte length. If the device address matches, the response to this command is an acknowledge.

4.7.11 PAGE READ EEPROM (0X42)

The `Read Page EEPROM` command returns 16 bytes of data that are stored in an individual page on the MCP39F501. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the EEPROM page as the command parameter or the following byte. The response to this command is an acknowledge, 16-bytes of data and CRC checksum.

4.7.12 PAGE WRITE EEPROM (0X50)

The `Write Page EEPROM` command is expecting 17 additional bytes in the command parameters, which are EEPROM page plus 16 bytes of data. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"** The response to this command is an acknowledge.

4.7.13 BULK ERASE EEPROM (0X4F)

The `Bulk Erase EEPROM` command will erase the entire EEPROM array and return it to a state of 0xFFFF for each memory location of EEPROM. A more complete description of the memory organization of the EEPROM can be found in **Section 10.0 "EEPROM"**. This command is expecting the device address as the command parameter for additional security when bulk erasing the EEPROM of a device.

4.7.14 AUTO-CALIBRATION GAIN (0X5A)

The `Auto-Calibration Gain` command initiates the single point calibration that is all that is typically required for the system. This command calibrates the RMS current, RMS voltage and active power based on the target values written in the corresponding registers. See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

4.7.15 CALIBRATE FREQUENCY (0X76)

For applications not using an external crystal and running the MCP39F501 off the internal oscillator, a gain calibration to the line frequency indication is required. The Gain Line Frequency (0x00AE) register is set such that the frequency indication matches what is set in the Line Frequency Reference (0x0094) register. See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

4.8 Notation for Register Types

The following notation has been adopted for describing the various registers used in the MCP39F501:

TABLE 4-5: SHORT-HAND NOTATION FOR REGISTER TYPES

Notation	Description
u32	Unsigned, 32-bit register
s32	Signed, 32-bit register
u16	Unsigned, 16-bit register
s16	Signed, 16-bit register
b32	32-bit register containing discrete Boolean bit settings

4.9 Single-Wire Transmission Mode

In Single-wire Transmission mode, at the end of each computation cycle, the device automatically transmits a frame of power data. This allows for single-wire communication after the device has been configured.

The single-wire transmission frame consists of 16 bytes: three Header Bytes, one Checksum and 12 bytes of power data (including RMS current, RMS voltage, Active Power and Line Frequency).

TABLE 4-6: SINGLE-WIRE TRANSMISSION FRAME

#	Byte
1	HEADERBYTE (0xAB)
2	HEADERBYTE2 (0xCD)
3	HEADERBYTE3 (0xEF)
4	CURRENT RMS – Byte 0
5	CURRENT RMS – Byte 1
6	CURRENT RMS – Byte 2
7	CURRENT RMS – Byte 3
8	VOLTAGE RMS – Byte 0
9	VOLTAGE RMS – Byte 1
10	ACTIVE POWER – Byte 0
11	ACTIVE POWER – Byte 1
12	ACTIVE POWER – Byte 2
13	ACTIVE POWER – Byte 3
14	LINE FREQUENCY – Byte 0
15	LINE FREQUENCY – Byte 1
16	CHECKSUM

Note 1: For custom single-wire transmission packets, contact a Microchip sales office.

NOTES:

5.0 CALCULATION ENGINE (CE) DESCRIPTION

5.1 Computation Cycle Overview

The MCP39F501 uses a coherent sampling algorithm to lock the sampling rate to the line frequency, and reports all power output quantities at a 2^N number of line cycles. This is defined as a computation cycle and is dependent on the line frequency, so any change in the line frequency will change the update rate of the output power quantities.

5.2 Raw Voltage and Currents Signal Conditioning

The first set of signal conditioning that occurs inside the MCP39F501 is shown in Figure 5-1. All conditions set in this diagram effect all of the output registers (RMS current, RMS voltage, active power, reactive power, apparent power, etc.). The gain of the PGA, the shutdown and reset status of the 24-bit ADCs are all controlled through the System Configuration (0X0042) register.

For DC applications, offset can be removed by using the DC Offset Current (0x003C) register. To compensate for any external phase error between the current and voltage channels, the Phase Compensation register (0x003E) can be used.

See **Section 9.0 "MCP39F501 Calibration"** for more information on device calibration.

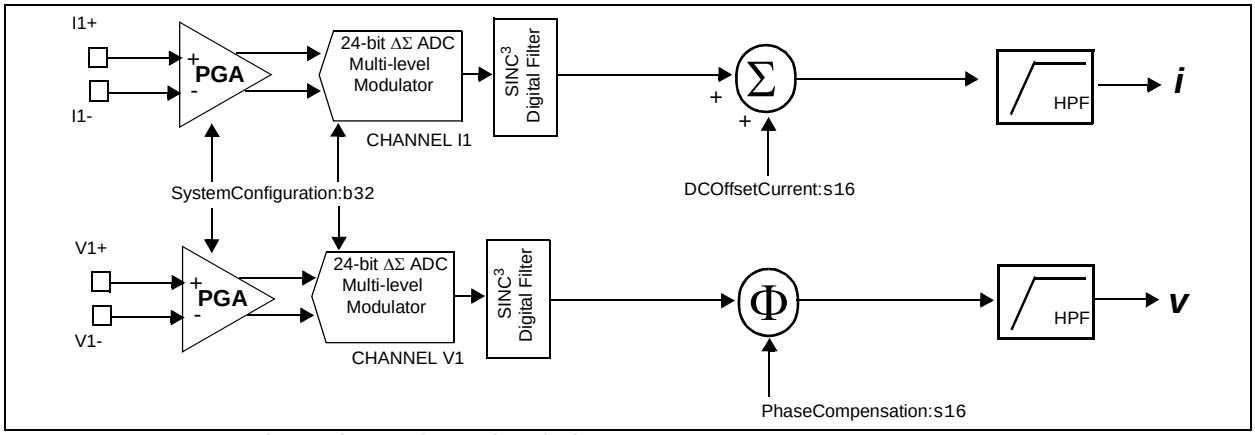


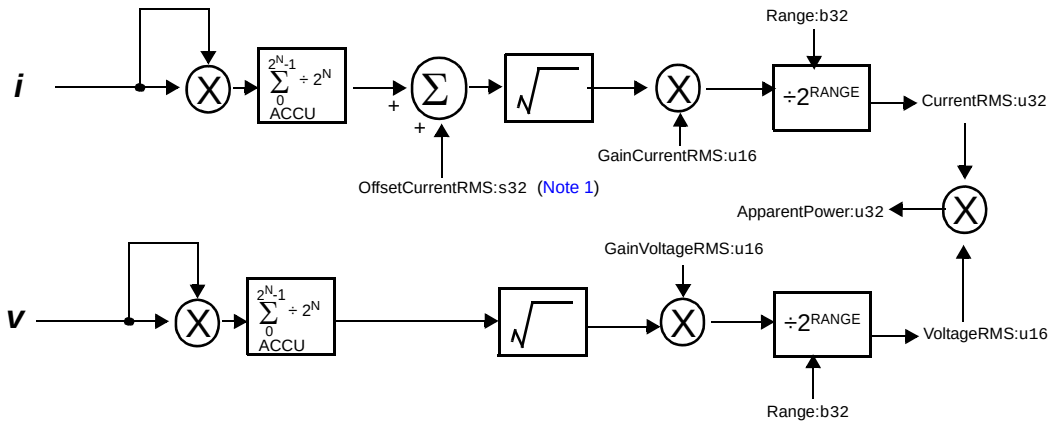
FIGURE 5-1: *Channel I1 and V1 Signal Flow.*

5.3 RMS Current and RMS Voltage (0x0004, 0x0008)

The MCP39F501 device provides true RMS measurements. The MCP39F501 device has two simultaneous sampling 24-bit A/D converters for the current and voltage measurements. The root mean square calculations are performed on 2^N current and voltage samples, where N is defined by the register Accumulation Interval Parameter.

EQUATION 5-1: RMS CURRENT AND VOLTAGE

$$I_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (i_n)^2}{2^N}} \qquad V_{RMS} = \sqrt{\frac{\sum_{n=0}^{2^N-1} (v_n)^2}{2^N}}$$



Note 1: The value of the Offset Current RMS register is squared internal to the calculation engine, so only the lower 16 bits should be used. The sign of the offset correction is the most significant bit (MSb) of the 32 bit register.

FIGURE 5-2: *RMS Current and Voltage Calculation Signal Flow.*

5.4 Apparent Power (0x0012)

This 32-bit register is the output register for the final apparent power indication. It is the product of RMS current and RMS voltage as shown in Equation 5-2.

EQUATION 5-2: APPARENT POWER

$$S = I_{RMS} \times V_{RMS}$$

For scaling of the apparent power indication, the calculation engine uses the register Apparent Power Divisor (0x0040). This is described in the following register operations, per Equation 5-3.

EQUATION 5-3: APPARENT POWER

$$S = \frac{CurrentRMS \times VoltageRMS}{10^{ApparentPowerDivisor}}$$

5.5 Active Power (0x000A)

The MCP39F501 has two simultaneous sampling A/D converters. For the active power calculation, the instantaneous current and instantaneous voltages are multiplied together to create instantaneous power. This instantaneous power is then converted to active power by averaging or taking the DC component.

Equation 5-4 controls the number of samples used in this accumulation prior to updating the Active Power output register.

EQUATION 5-4: ACTIVE POWER

$$P = \frac{1}{2^N} \sum_{k=0}^{k=2^N-1} V_k \times I_k$$

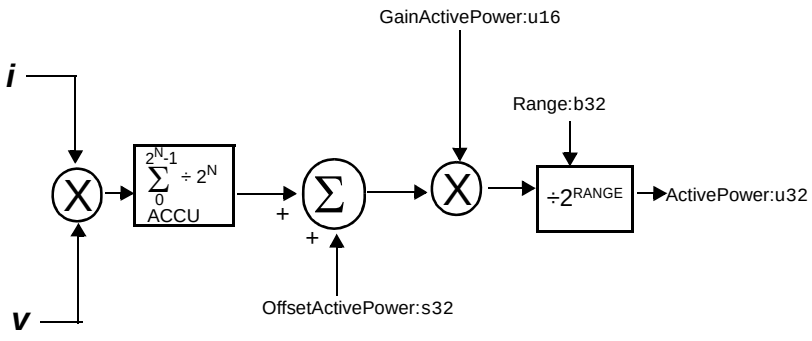


FIGURE 5-3: *Active Power Calculation Signal Flow.*

5.6 Power Factor (0x0016)

Power factor is calculated by the ratio of P to S or active power divided by apparent power.

EQUATION 5-5: POWER FACTOR

$$PF = \frac{P}{S}$$

The Power Factor Reading is stored in a signed 16-bit register (Power Factor, 0x0016). This register is a signed, 2's complement register with the MSB representing the polarity of the power factor. Positive means inductive load, negative means capacitive load. Each LSB is then equivalent to a weight of 2^{-15}. A maximum register value of 0x7FFF corresponds to a power factor of 1. The minimum register value of 0x8000 corresponds to a power factor of -1.

5.7 Reactive Power (0x000E)

In the MCP39F501, Reactive Power is calculated using a 90 degree phase shift in the voltage channel. The same accumulation principles apply as with active power where ACCU acts as the accumulator. Any light load or residual power can be removed by using the Offset Reactive Power (0x0038) register. Gain is corrected by the Gain Reactive Power (0x002E) register. The final output is an unsigned 32-bit value located in the Reactive Power register (0x000E).

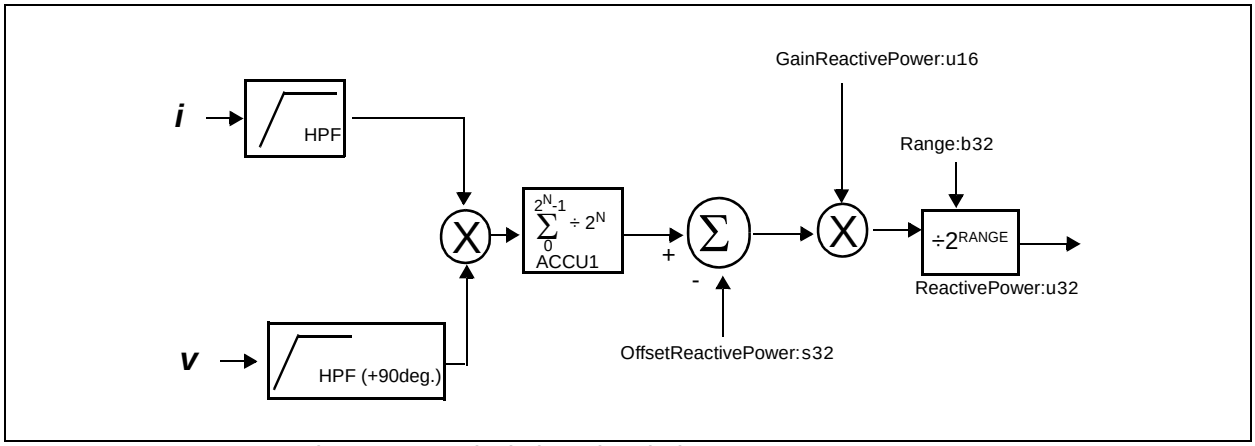


FIGURE 5-4: *Reactive Power Calculation Signal Flow.*

5.8 Accumulation Interval Parameter (0x005A)

The accumulation interval is defined as an 2^N number of line cycles, where N is the value in the Accumulation-IntervalParameter register (0x005A).

5.9 Thermistor Voltage (0x001A)

When a voltage output temperature sensor such as the MCP9700 is connected to the AN_IN/DIO2 pin and the DIO2[n] bits of the DOUT Configuration register are set to 110 for temperature input, the device performs an analog-to-digital conversion on the AN_IN/DIO2 pin.

The least 10 significant bits of the 16-bit Thermistor Voltage register contain the output of the ADC. The conversion rate of the temperature measurement occurs once every computation cycle.

Note that if the AN_IN/DIO2 pin is configured through the DIO Configuration register (0x0046) as an output, then the Thermistor Voltage register value will equal zero.

The Thermistor Voltage is used for temperature compensation of the calculation engine. See **Section 9.8 "Temperature Compensation (Addresses 0x00B0/B2/B4/B6)"** for more information.

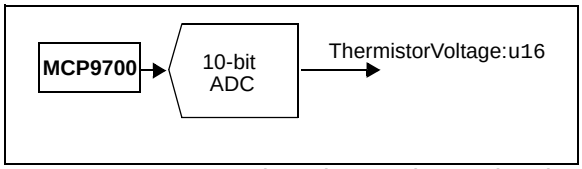


FIGURE 5-5: *Thermistor Voltage Signal Flow.*

NOTES:

6.0 REGISTERS DESCRIPTION

6.1 Register Map

The following table describes the registers for the MCP39F501 device.

TABLE 6-1: MCP39F501 REGISTER MAP

Address	Register Name	Section Number	Read/ Write	Data type	Description
Output Registers					
0x0000	Address Pointer	6.2	R	u16	Address pointer for read or write commands
0x0002	System Version	6.3	R	u16	System version date code information for MCP39F501, set at the Microchip factory; format YMDD
0x0004	Current RMS	5.3	R	u32	RMS Current output
0x0008	Voltage RMS	5.3	R	u16	RMS Voltage output
0x000A	Active Power	5.5	R	u32	Active Power output
0x000E	Reactive Power	5.7	R	u32	Reactive Power output
0x0012	Apparent Power	5.4	R	u32	Apparent Power output
0x0016	Power Factor	5.6	R	s16	Power Factor output
0x0018	Line Frequency	9.7	R	u16	Line Frequency output
0x001A	Thermistor Voltage	5.9	R	u16	Temperature Monitor output
0x001C	Event Flag	7.2	R	b16	Status of all enabled events
0x001E	System Status	6.4	R	b16	System Status Register
0x0020	Reserved	—	—	u16	Reserved
0x0022	Reserved	—	—	u16	Reserved
Calibration Registers					
0x0024	Reserved	—	—	u16	Reserved
0x0026	Device Address	4.4	R/W	u16	Device Address for the device
0x0028	Gain Current RMS	9.3	R/W	u16	Gain Calibration Factor for RMS Current
0x002A	Gain Voltage RMS	9.3	R/W	u16	Gain Calibration Factor for RMS Voltage
0x002C	Gain Active Power	9.3	R/W	u16	Gain Calibration Factor for Active Power
0x002E	Gain Reactive Power	9.3	R/W	u16	Gain Calibration Factor for Reactive Power
0x0030	Offset Current RMS	9.6.1	R/W	s32	Offset Calibration Factor for RMS Current
0x0034	Offset Active Power	9.6.1	R/W	s32	Offset Calibration Factor for Active Power
0x0038	Offset Reactive Power	9.6.1	R/W	s32	Offset Calibration Factor for Reactive Power
0x003C	DC Offset Current	9.6.2	R/W	s16	Offset Calibration Factor for DC Current
0x003E	Phase Compensation	9.5	R/W	s16	Phase Compensation
0x0040	Apparent Power Divisor	5.4	R/W	u16	Number of Digits for apparent power divisor to match I_{RMS} and V_{RMS} resolution
Design Configuration Registers					
0x0042	System Configuration	6.5	R/W	b32	Control for device configuration, including ADC configuration
0x0046	DIO Configuration	8.0	R/W	b16	Configurable digital output settings for alarm, and event flags
0x0048	Range	6.6	R/W	b32	Scaling factor for Outputs

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F501 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x004C	Calibration Current	9.3.1	R/W	u32	Target Current to be used during single-point calibration
0x0050	Calibration Voltage	9.3.1	R/W	u16	Target Voltage to be used during single-point calibration
0x0052	Calibration Active Power	9.3.1	R/W	u32	Target Active Power to be used during single-point calibration
0x0056	Calibration Reactive Power	9.5.1	R/W	u32	Target Reactive Power to be used during single-point calibration
0x005A	Accumulation Interval Parameter	5.8	R/W	u16	N for 2^N number of line cycles to be used during a single computation cycle
0x005C	Reserved	—	R/W	u16	Reserved
Event Notification Registers					
0x005E	Over Current Limit	7.0	R/W	u32	RMS Current threshold at which an event flag is recorded
0x0062	Reserved	7.0	R/W	u16	Reserved
0x0064	Over Power Limit	7.0	R/W	u32	Active Power threshold at which an event flag is recorded
0x0068	Reserved	7.0	R/W	u16	Reserved
0x006A	Over Frequency Limit	7.0	R/W	u16	Line Frequency threshold at which an event flag is recorded
0x006C	Under Frequency Limit	7.0	R/W	u16	Line Frequency threshold at which an event flag is recorded
0x006E	Over Temperature Limit	7.0	R/W	u16	Temperature threshold at which an event flag is recorded
0x0070	Under Temperature Limit	7.0	R/W	u16	Temperature threshold at which an event flag is recorded
0x0072	Voltage Sag Limit	7.7	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x0074	Voltage Surge Limit	7.7	R/W	u16	RMS Voltage threshold at which an event flag is recorded
0x0076	Over Current Hold	7.0	R/W	u16	Number of computation cycles for which the Over Current Limit must be breached
0x0078	Reserved	—	R/W	u16	Reserved
0x007A	Over Power Hold	7.0	R/W	u16	Number of computation cycles for which the Over Power Limit must be held
0x007C	Reserved	—	R/W	u16	Reserved
0x007E	Over Frequency Hold	7.0	R/W	u16	Number of computation cycles for which the Over Frequency Limit must be held
0x0080	Under Frequency Hold	7.0	R/W	u16	Number of computation cycles for which the Under Frequency Limit must be held
0x0082	Over Temperature Hold	7.0	R/W	u16	Number of computation cycles for which the Over Temperature Limit must be held
0x0084	Under Temperature Hold	7.0	R/W	u16	Hold time for which the Under Temperature Limit must be held
0x0086	Reserved	—	R/W	u16	Reserved

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

TABLE 6-1: MCP39F501 REGISTER MAP (CONTINUED)

Address	Register Name	Section Number	Read/ Write	Data type	Description
0x0088	Reserved	—	R/W	u16	Reserved
0x008A	Event Enable	7.1	R/W	u16	Enable Event Register
0x008C	Event Mask Critical	7.3	R/W	u16	Mask for event notifications to be put on DIO pin selected as “Event Critical”
0x008E	Event Mask Standard	7.4	R/W	u16	Mask for event notification to be put on DIO pin selected as “Event Standard”
0x0090	Event Test	7.5	R/W	u16	Register used to set events for testing purposes
0x0092	Event Clear	7.6	R/W	u16	Register used to clear events
0x0094	Line Frequency Ref.	9.7.1	R/W	u16	Reference Value for the nominal line frequency
0x0096	Reserved	—	R	u16	Reserved
0x00AE	Gain Line Frequency	9.7	R/W	u16	Correction Factor for Line Frequency Indication
EMI Filter Compensation Registers (Note 1)					
0x0098	Reserved	—	R	u16	Reserved
0x009A	Reserved	—	R	u16	Reserved
0x009C	Reserved	—	R	u16	Reserved
0x009E	Reserved	—	R	u16	Reserved
0x00A0	Reserved	—	R	u16	Reserved
0x00A2	Reserved	—	R	u16	Reserved
0x00A4	Reserved	—	R	u16	Reserved
0x00A6	Reserved	—	R	u16	Reserved
0x00A8	Reserved	—	R	u16	Reserved
0x00AA	Reserved	—	R	u16	Reserved
0x00AC	Reserved	—	R	u16	Reserved
TEMPERATURE COMPENSATION REGISTERS					
0x00B0	Temperature Compensation for Frequency	9.8	R/W		Correction factor for compensating the line frequency indication over temperature
0x00B2	Temperature Compensation for Current	9.8	R/W		Correction factor for compensating the Current RMS indication over temperature
0x00B4	Temperature Compensation for Power	9.8	R/W		Correction factor for compensating the active power indication over temperature
0x0B6	Ambient Temperature Reference Voltage	9.8	R/W		Register for storing the reference temperature during calibration

Note 1: These registers are reserved for EMI filter compensation when necessary for power supply monitoring. They may require specific adjustment depending on PSU parameters, please contact the local Microchip office for further support.

6.2 Address Pointer (0x0000)

This unsigned 16-bit register contains the address to which all read and write instructions occur. This register is only written through the `Set Address Pointer` command and is otherwise outside the writable range of register addresses.

6.3 System Version (0x0002)

The System Version register is hard-coded by Microchip Technology Inc. and contains calculation engine date code information. The System Version register is a date code in the `YMDD` format, with year and month in hex, day in decimal (e.g. 0xD220 = 2013, Feb. 20th).

6.4 System Status (0x001E)

The System Status register is a read-only register and can be used to detect the various states of pin levels as defined below.

REGISTER 6-1: SYSTEM STATUS REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R-n	R-n	R-n	R-n	R-n	R-n	R-n
—	DIO3_S	DIO2_S	DIO1_S	DIO0_S	ADDRESS[1]	ADDRESS[0]	MULTIPLE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 6-3 **DIOn_S:** State of DIO pin when configured as an input
`1` = State of DIO pin is HIGH
`0` = State of DIO pin is LOW

bit 2-1 **ADDRESS[1:0]:** State of A1/A0 pins at POR
`1` = Pin is logic high
`0` = Pin is logic low

bit 0 **MULTIPLE:** Multiple or Single Device mode
`1` = State of MODE/DIR pin was LOW at POR (Multiple Device mode)
`0` = State of MODE/DIR pin was HIGH at POR (Single Device mode)

6.5 System Configuration (0x0042)

The System Configuration register contains bits for the following control:

- PGA setting
- ADC Reset State
- ADC Shutdown State
- Voltage Reference Trim
- Single Wire Auto-transmission

These options are described in the following sections.

6.5.1 PROGRAMMABLE GAIN AMPLIFIERS (PGA)

The two Programmable Gain Amplifiers (PGAs) reside at the front-end of each 24-bit Delta-Sigma ADC. They have two functions:

- Translate the common-mode of the input from A_{GND} to an internal level between A_{GND} and A_{VDD}
- Amplify the input differential signal

The translation of the common mode does not change the differential signal but recenters the common-mode so that the input signal can be properly amplified.

The PGA block can be used to amplify very low signals, but the differential input range of the delta-sigma modulator must not be exceeded. The PGA is controlled by the PGA_CHn<2:0> bits in Register 6-2 the System Configuration register. Table 6-2 represents the gain settings for the PGAs:

TABLE 6-2: PGA CONFIGURATION SETTING (Note 1)

Gain PGA_CHn<2:0>			Gain (V/V)	Gain (dB)	V_{IN} Range (V)
0	0	0	1	0	±0.5
0	0	1	2	6	±0.25
0	1	0	4	12	±0.125
0	1	1	8	18	±0.0625
1	0	0	16	24	±0.03125
1	0	1	32	30	±0.015625

Note 1: The two undefined settings (110, 111) are G = 1.

6.5.2 24-BIT ADC RESET MODE (SOFT RESET MODE)

24-bit ADC Reset mode (also called Soft Reset) can only be entered through setting high the RESET<1:0> bits in the System Configuration register. This mode is defined as the condition where the converters are active but their output is forced to '0'.

6.5.3 ADC SHUTDOWN MODE

ADC Shutdown mode is defined as a state where the converters and their biases are off, consuming only leakage current. When the Shutdown bit is reset to '0', the analog biases will be enabled, as well as the clock and the digital circuitry.

Each converter can be placed in Shutdown mode independently. This mode is only available through programming of the SHUTDOWN<1:0> bits in the SystemConfiguration register.

6.5.4 V_{REF} TEMPERATURE COMPENSATION

If desired, the user can calibrate out the temperature drift for ultra-low V_{REF} drift.

The internal voltage reference comprises a proprietary circuit and algorithm to compensate first order and second order temperature coefficients. The compensation allows very low temperature coefficients (typically 10 ppm/°C) on the entire range of temperatures from -40°C to +125°C. This temperature coefficient varies from part to part.

The temperature coefficient can be adjusted on each part through the System Configuration register (0x0042). The default value of this register is set to 0x42. The typical variation of the temperature coefficient of the internal voltage reference, with respect to VREFCAL register code, is given by Figure 6-1.

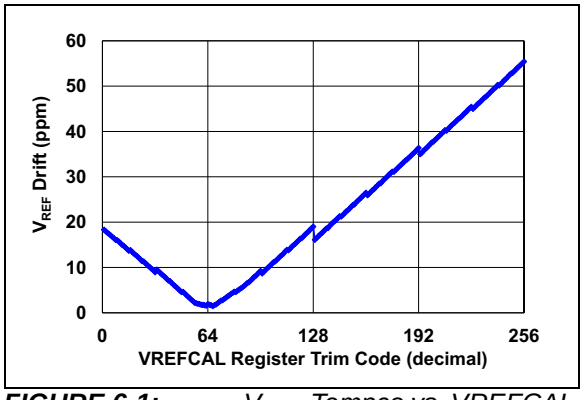


FIGURE 6-1: *V_{REF} Tempco vs. VREFCAL Trimcode Chart.*

REGISTER 6-2: SYSTEM CONFIGURATION REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	PGA_CH1[2]	PGA_CH1[1]	PGA_CH1[0]	PGA_CH0[2]	PHA_CH0[1]	PGA_CH0[0]
bit 31							bit 24

R/W-0	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-0
VREFCAL[7]	VREFCAL[6]	VREFCAL[5]	VREFCAL[4]	VREFCAL[3]	VREFCAL[2]	VREFCAL[1]	VREFCAL[0]
bit 23							bit 16

U-0	U-0	U-0	U-0	U-0	U-0	U-0	R/W-0
—	—	—	—	—	—	—	SINGLE_WIRE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	U-0	U-0
RESET[1]	RESET[0]	SHUTDOWN[1]	SHUTDOWN[0]	—	VREFEXT	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 29-27 **PGA_CH1 [2:0]:** PGA Setting for Channel 1
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 **(DEFAULT)**

bit 26-24 **PGA_CH0 [2:0]:** PGA Setting for Channel 0
111 = Reserved (Gain = 1)
110 = Reserved (Gain = 1)
101 = Gain is 32
100 = Gain is 16
011 = Gain is 8
010 = Gain is 4
001 = Gain is 2
000 = Gain is 1 **(DEFAULT)**

bit 23-16 **VREFCAL[n]:** Internal voltage reference temperature coefficient register value (See **Section 6.5.4 "V_{REF} Temperature Compensation"** for complete description)

bit 15-9 **Unimplemented:** Read as '0'

bit 8 **SINGLE_WIRE:** single wire enable bit
1 = Single Wire transmission is enabled
0 = Single Wire transmission is disabled **(DEFAULT)**

bit 7-6 **RESET [1:0]:** Reset mode setting for ADCs
11 = Both I1 and V1 are in Reset mode
10 = V1 ADC is in Reset mode
01 = I1 ADC is in Reset mode
00 = Neither ADC is in Reset mode **(DEFAULT)**

bit 5-4 **SHUTDOWN [1:0]:** Shutdown mode setting for ADCs
11 = Both I1 and V1 are in Shutdown
10 = V1 ADC is in Shutdown
01 = I1 ADC is in Shutdown
00 = Neither ADC is in Shutdown **(DEFAULT)**

bit 2 **VREFEXT:** Internal Voltage Reference Shutdown Control
1 = Internal Voltage Reference Disabled
0 = Internal Voltage Reference Enabled **(DEFAULT)**

bit 1-0 **Unimplemented:** Read as '0'

6.6 Range Register (0x0048)

The Range register is a 32-bit register that contains the number of right bit shifts for the following outputs, divided into separate bytes defined below:

- RMS Current
- RMS Voltage
- Power

Note that the power range byte operates across both the active and reactive output registers and sets the same scale.

The purpose of this register is two-fold: the number of right bit shifting (division by 2^{RANGE}) must be high enough to prevent overflow in the output register, and low enough to allow for the desired output resolution. It is the user's responsibility to set this register correctly to ensure proper output operation for a given meter design.

For further information and example usage, see **Section 9.3 "Single Point Gain Calibrations (Calibrations at Unity Power Factor)"**.

REGISTER 6-3: RANGE REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 31							bit 24

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
POWER[7]	POWER[6]	POWER[5]	POWER[4]	POWER[3]	POWER[2]	POWER[1]	POWER[0]
bit 23							bit 16

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CURRENT[7]	CURRENT[6]	CURRENT[5]	CURRENT[4]	CURRENT[3]	CURRENT[2]	CURRENT[1]	CURRENT[0]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
VOLTAGE[7]	VOLTAGE[6]	VOLTAGE[5]	VOLTAGE[4]	VOLTAGE[3]	VOLTAGE[2]	VOLTAGE[1]	VOLTAGE[0]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 32-24 **Unimplemented:** Read as '0'

bit 23-16 **POWER[7:0]:** Sets the number of right bit shifts for the Active and Reactive Power output registers.

bit 15-8 **CURRENT[7:0]:** Sets the number of right bit shifts for the Current RMS output register.

bit 7-0 **VOLTAGE[7:0]:** Sets the number of right bit shifts for the Voltage RMS output register.

NOTES:

7.0 EVENT NOTIFICATIONS

There are six registers that correspond to the event notifications that can occur when using the MCP39F501:

- Event Enabled
- Event Flag
- Event Mask Critical
- Event Mask Standard
- Event Test
- Event Clear

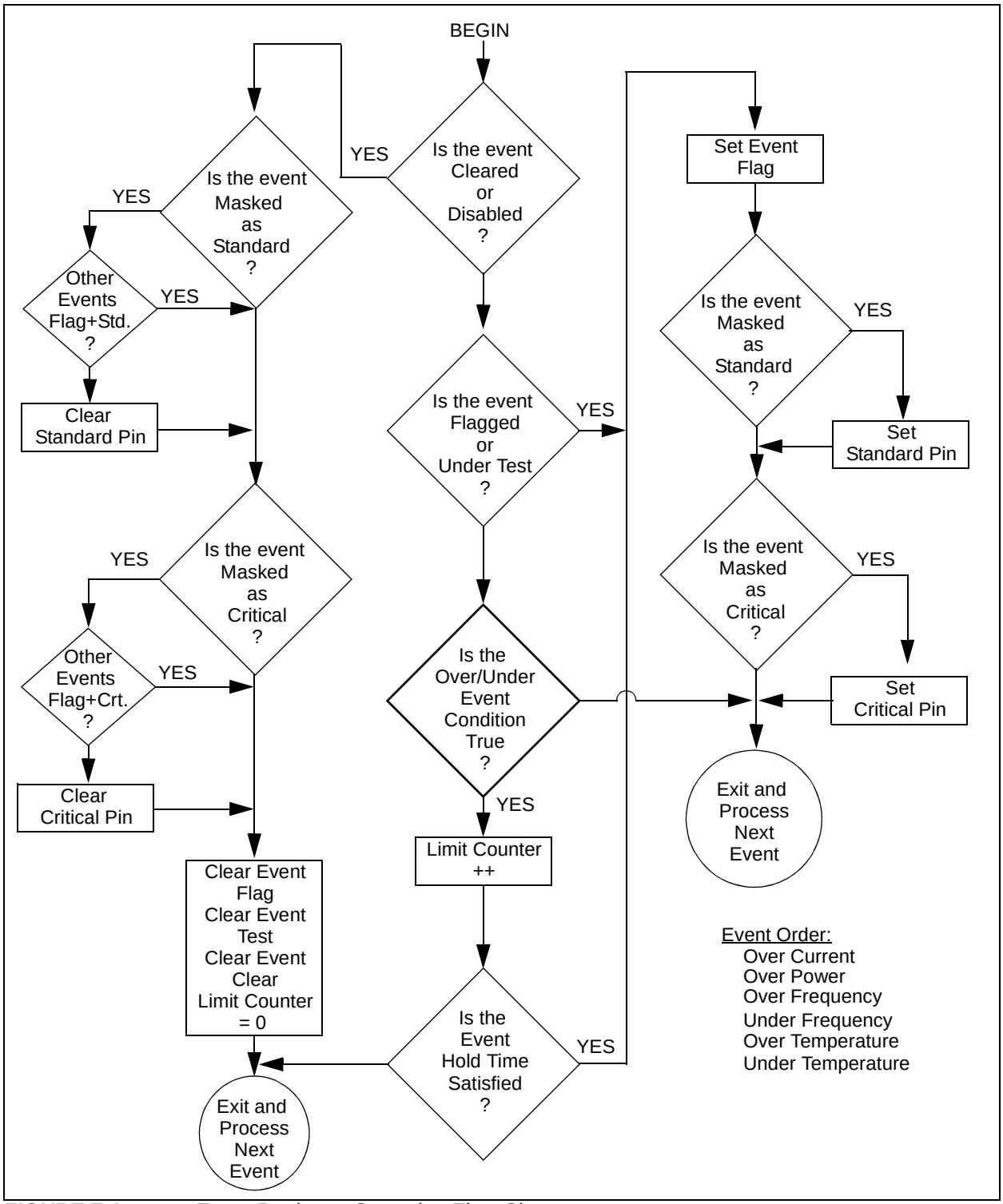


FIGURE 7-1: *Event Registers Operation Flow Chart.*

7.1 Event Enable Register (0x008A)

The Event Enable register is a read-only register that flags when an event is enabled per the limit and hold registers.

REGISTER 7-1: EVENT ENABLE REGISTER

R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R/W	R/W	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Over Current
1 = Fault event is enabled
0 = No Fault

bit 14 **OV:** Over Voltage
1 = Fault event is enabled
0 = No Fault

bit 13 **OP:** Over Power
1 = Fault event is enabled
0 = No Fault

bit 12 **UV:** Under Voltage
1 = Fault event is enabled
0 = No Fault

bit 11 **OF:** Over Frequency
1 = Fault event is enabled
0 = No Fault

bit 10 **UF:** Under Frequency
1 = Fault event is enabled
0 = No Fault

bit 9 **OT:** Over Temperature
1 = Fault event is enabled
0 = No Fault

bit 8 **UT:** Under Temperature
1 = Fault event is enabled
0 = No Fault

bit 7 **VSA:** Voltage Sag
1 = Fault event is enabled
0 = No Fault

bit 6 **VSU:** Voltage Surge
1 = Fault event is enabled
0 = No Fault

bit 5-0 **Unimplemented:** Read as '0'

7.2 Event Flag Register (0x001C)

The Event Flag register is a read-only register that flags when an event has occurred per the limit and hold registers.

Note that event flags are latched until the event has passed and the bit has been cleared by the Event Clear register.

REGISTER 7-2: EVENT FLAG REGISTER

R-0	R-0	R-0	R-0	R-0	R-0	R-0	R-0
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R-0	R-0	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Over Current
1 = Fault event has occurred
0 = No Fault

bit 14 **OV:** Over Voltage
1 = Fault event has occurred
0 = No Fault

bit 13 **OP:** Over Power
1 = Fault event has occurred
0 = No Fault

bit 12 **UV:** Under Voltage
1 = Fault event has occurred
0 = No Fault

bit 11 **OF:** Over Frequency
1 = Fault event has occurred
0 = No Fault

bit 10 **UF:** Under Frequency
1 = Fault event has occurred
0 = No Fault

bit 9 **OT:** Over Temperature
1 = Fault event has occurred
0 = No Fault

bit 8 **UT:** Under Temperature
1 = Fault event has occurred
0 = No Fault

bit 7 **VSA:** Voltage Sag
1 = Fault event has occurred
0 = No Fault

bit 6 **VSU:** Voltage Surge
1 = Fault event has occurred
0 = No Fault

bit 5-0 **Unimplemented:** Read as '0'

7.3 Event Mask Critical Register (0x008C)

The Event Mask Critical register is used to mask which events will have an impact on the digital I/O pin that has been designated to the Notification Critical status in the Configurable Digital I/O (DIO) control register. Any number of events can be set here to create activity on the corresponding DIO pin.

REGISTER 7-3: EVENT MASK CRITICAL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Over Current
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 14 **OV:** Over Voltage
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 13 **OP:** Over Power
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 12 **UV:** Under Voltage
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 11 **OF:** Over Frequency
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 10 **UF:** Under Frequency
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 9 **OT:** Over Temperature
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 8 **UT:** Under Temperature
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 7 **VSA:** Voltage Sag
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 6 **VSU:** Voltage Surge
1 = If a fault event occurs, the DIO pin assigned to Notification Critical will be driven high
0 = If a fault event occurs, there is no effect on DIO pin assigned to Notification Critical

bit 5-0 **Unimplemented:** Read as '0'

7.4 Event Mask Standard Register (0x008E)

The Event Mask Standard register is used to mask which events will have an impact on the digital I/O pin that has been designated to the Notification Standard status in the DIO control register. Any number of events can be set here to create activity on the corresponding DIO pin.

REGISTER 7-4: EVENT MASK STANDARD REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Over Current
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 14 **OV:** Over Voltage
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 13 **OP:** Over Power
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 12 **UV:** Under Voltage
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 11 **OF:** Over Frequency
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 10 **UF:** Under Frequency
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 9 **OT:** Over Temperature
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 8 **UT:** Under Temperature
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 7 **VSA:** Voltage Sag
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 6 **VSU:** Voltage Surge
1 = If a fault event occurs, the DIO pin assigned to Notification Standard will be driven high
0 = If a fault event occurs, there is no effect on the DIO pin assigned to Notification Standard

bit 5-0 **Unimplemented:** Read as ‘0‘

7.5 Event Test Register (0x0090)

The Event Test register is used when the system designer wants to initiate and test event conditions without being able to apply the appropriate currents, voltages, powers, temperature or frequencies that would normally trigger an event notification.

Here, when a corresponding bit is set, the MCP39F501 device acts as though the appropriate limit and the hold registers have been breached, and the corresponding event is triggered. These registers should not be used to clear a true event that is triggered from the limit and hold registers, rather the Event Clear register is used for this purpose.

REGISTER 7-5: EVENT TEST REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Overcurrent
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 14 **OV:** Overvoltage
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 13 **OP:** Over Power
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 12 **UV:** Undervoltage
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 11 **OF:** Over Frequency
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 10 **UF:** Under Frequency
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

REGISTER 7-5: EVENT TEST REGISTER (CONTINUED)

bit 9 **OT:** Over Temperature
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 8 **UT:** Under Temperature
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 7 **VSA:** Voltage Sag
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 6 **VSU:** Voltage Surge
1 = Triggers an event and the corresponding event flag bits and Critical/Standard pins will follow per the mask registers
0 = Clears any event set using the event test register. Writing a zero here has no effect on true events, for clearing true events use the event clear register

bit 5-0 **Unimplemented:** Read as '0'

7.6 Event Clear Register (0x0092)

The Event Test register is used to clear an event that has been triggered by either real conditions that have breached the corresponding limit and hold registers for a given event, or an event that has been triggered by setting the corresponding bit in the Event Test register. By clearing an event using the EventClear register, if the corresponding event has been set using the Event Test register, this bit, along with the Event Flag register, will be automatically cleared.

The Event Clear register bits are not latched, and once set, will be automatically cleared after the Event Flag and Event Test registers have been cleared.

REGISTER 7-6: EVENT CLEAR REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
OC	OV	OP	UV	OF	UF	OT	UT
bit 15							bit 8

R/W-0	R/W-0	U-0	U-0	U-0	U-0	U-0	U-0
VSA	VSU	—	—	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **OC:** Overcurrent
1 = Clears the event
0 = No effect

REGISTER 7-6: EVENT CLEAR REGISTER (CONTINUED)

bit 14	**OV:** Overvoltage 1 = Clears the event 0 = No effect
bit 13	**OP:** Over Power 1 = Clears the event 0 = No effect
bit 12	**UV:** Undervoltage 1 = Clears the event 0 = No effect
bit 11	**OF:** Over Frequency 1 = Clears the event 0 = No effect
bit 10	**UF:** Under Frequency 1 = Clears the event 0 = No effect
bit 9	**OT:** Over Temperature 1 = Clears the event 0 = No effect
bit 8	**UT:** Under Temperature 1 = Clears the event 0 = No effect
bit 7	**VSA:** Voltage Sag 1 = Clears the event 0 = No effect
bit 6	**VSU:** Voltage Surge 1 = Clears the event 0 = No effect
bit 5-0	**Unimplemented:** Read as '0'

7.7 Voltage Sag and Voltage Surge Detection

The event alarms for Voltage Sag and Voltage Surge work differently compared to the other event alarms, which are tested against every computation cycle. These two event alarms are designed to provide a much faster interrupt if the condition occurs. Note that neither of these two events have a respective Hold register associated with them, since the detection time is less than one line cycle.

The calculation engine keeps track of a trailing mean square of the input voltage, as defined by the following equation:

EQUATION 7-1:

$$V_{SA} = \frac{2 \times f_{LINE}}{f_{SAMPLE}} \times \sum_{n = -\frac{f_{SAMPLE}}{2 \times f_{LINE}} - 1}^{0} V_n^2$$

Therefore, at each data ready occurrence, the value of V_{SA} is compared to the programmable threshold set in the Voltage Sag Limit register (0x0086) and Voltage Surge Limit register (0x0088) to determine if a flag should be set. If either of these events are masked to either the standard or critical event pin, a logic-high interrupt will be given on these pins. These events, like all the other events, are latched, and must be cleared after the event has passed by using the appropriate clear event bit.

The sag or surge events can be used to quickly determine if a power failure has occurred in the system. Using the on-chip EEPROM of the MCP39F501, these events can be quickly logged to memory to keep track of damaging events for the PSU.

8.0 CONFIGURABLE DIGITAL I/O PINS (DIO CONFIGURATION – 0X0046)

8.1 Overview

The MCP39F501 device has four pins that can be configured in five possible configurations. These configurations are:

- Notification Standard Output
- Notification Critical Output
- Logic Input
- Device Address Bit Input (DIO0/DIO1 only)
- Temperature Input (DIO2 only)

8.1.1 NOTIFICATION OUTPUTS (STANDARD AND CRITICAL)

When a pin is defined to be a notification for either a standard or critical event, the associated pin will become active based on the masks set through the event registers (see **Section 7.0 "Event Notifications"**).

8.1.2 LOGIC INPUTS

The default assignment for all DIO pins are logic input. In this assignment, the state of the DIO pin is reflected in the SystemStatus register, and can be used to flag for various system events and read through the serial interface.

8.1.3 DEVICE ADDRESS BIT INPUT (A0/DIO0, A1/DIO1 ONLY)

There are two digital IO pins that are multiplexed with the address pins for a multi-device bus. DIO0 is also A0 and DIO1 is also A1. For systems with multiple devices on a single bus, the MODE/DIR pin should have a weak pull-down resistor to GND, as seen in Figure 4-2. At POR, the MCP39F501 tests the state of this pin, and if the MODE/DIR is logic low, then the DIO0 and DIO1 are disabled and these pins become input pins for the A0 and A1 bits of the Device Address device address, the beginning of the calibration register block. If the MODE/DIR pin is logic high, then the device is considered to be in Single Device mode, the address pins are not needed, and DIO0 and DIO1 can then be configured as any of the seven possible configurations.

8.1.4 TEMPERATURE INPUT (DIO2 ONLY)

When DIO2 is configured as a temperature input, the Thermistor Voltage register (0x001A) contains the scaled value of the ADC reading from an attached temperature sensor.

If DIO2 is configured as an output, the value in the Thermistor Voltage register will be equal to zero.

REGISTER 8-1: DIO CONFIGURATION REGISTER

U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	—	—	DIO3[2]	DIO3[1]	DIO[0]	DIO2[2]
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
DIO2[1]	DIO2[0]	DIO1[2]	DIO1[1]	DIO1[0]	DIO0[2]	DIO0[1]	DIO0[0]
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-12 **Unimplemented:** Read as '0'

bit 11-9 **DIO3[n]:** DIO3 Configuration

111 = Not Used
110 = Not Used
101 = Notification Standard Output
100 = Notification Critical Output
011 = Not Used
010 = Input **(Default)**
001 = Not Used
000 = Not Used

REGISTER 8-1: DIO CONFIGURATION REGISTER (CONTINUED)

bit 8-6 **DIO2[n]:** DIO2 Configuration
111 = Not Used
110 = Not Used
101 = Notification Standard Output
100 = Notification Critical Output
011 = Temperature Input
010 = Input **(Default)**
001 = Not Used
000 = Not Used

bit 5-3 **DIO1[n]:** DIO1 Configuration
111 = Not Used
110 = Not Used
101 = Notification Standard Output
100 = Notification Critical Output
011 = Device Address Bit Input
010 = Input **(Default)**
001 = Not Used
000 = Not Used

bit 2-0 **DIO0[n]:** DIO0 Configuration
111 = Not Used
110 = Not Used
101 = Notification Standard Output
100 = Notification Critical Output
011 = Device Address Bit Input
010 = Input **(Default)**
001 = Not Used
000 = Not Used

9.0 MCP39F501 CALIBRATION

9.1 Overview

Calibration compensates for ADC gain error, component tolerances and overall noise in the system. The device provides an on-chip calibration algorithm that allows simple system calibration to be performed quickly. The excellent analog performance of the A/D converters on the MCP39F501 allows for a single point calibration and a single calibration command to achieve accurate measurements.

Calibration can be done by either using the predefined auto-calibration commands, or by writing directly to the calibration registers. If additional calibration points are required (AC offset, Phase Compensation, DC offset), the corresponding calibration registers are available to the user and will be described separately in this section.

9.2 Calibration Order

The proper steps for calibration need to be maintained.

If the device has an external temperature sensor attached, temperature calibration should be done first by reading the value from the Thermistor Voltage register (0x001A) and copying the value by writing to the Ambient Temperature Reference Voltage register (0x00B6).

If the device runs on the internal oscillator, the line frequency must be calibrated next using the `Auto-Calibration Frequency` command.

The single point gain calibration at unity power factor should be performed next.

If non-unity displacement power factor measurements are a concern, then the next step should be phase calibration, followed by reactive power gain calibration.

To summarize the order of calibration:

1. Temperature Calibration (optional)
2. Line Frequency Calibration (optional)
3. Gain Calibration at PF = 1
4. Phase Calibration at PF ≠ 1 (optional)
5. Reactive Gain Calibration at PF ≠ 1(optional)

9.3 Single Point Gain Calibrations (Calibrations at Unity Power Factor)

When using the device in AC mode with the high-pass filters turned on, most offset errors are removed and only a single point gain calibration is required.

Setting the gain registers to properly produce the desired outputs can be done manually by writing to the appropriate register. The alternative method is to use the auto-calibration commands described in this section.

9.3.1 USING THE `Auto-Calibration Gain` COMMAND

By applying stable reference voltages and currents that are equivalent to the values that reside in the target Calibration Current (0x004C), Calibration Voltage (0x0050) and Calibration Active Power (0x0052) registers, the `Auto-Calibration Gain` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following registers are set when the `Auto-Calibration Gain` command is issued:

- Gain Current RMS (0x0028)
- Gain Voltage RMS (0x002A)
- Gain Active Power (0x002C)

When this command is issued, the MCP39F501 attempts to match the expected values to the measured values for all three output quantities by changing the gain register based on the following formula:

EQUATION 9-1:

$$GAIN_{NEW} = GAIN_{OLD} \bullet \frac{Expected}{Measured}$$

The same formula applies for voltage RMS, current RMS and active power. Since the gain registers for all three quantities are 16-bit numbers, the ratio of the expected value to the measured value (which can be modified by changing the Range register) and the previous gain must be such that the equation yields a valid number. Here the limits are set to be from 25,000 to 65,535. A new gain within this range for all three limits will return an ACK for a successful calibration, otherwise the command returns a NAK for a failed calibration attempt.

It is the user's responsibility to ensure that the proper range settings, PGA settings and hardware design settings are correct to allow for successful calibration using this command.

9.3.2 EXAMPLE OF RANGE SELECTION FOR VALID CALIBRATION

In this example, a user applies a calibration current of 1A to an uncalibrated system. The indicated value in the Current RMS register (0x0004) is 2300 with the system's specific shunt value, PGA gain, etc. The user expects to see a value of 1000 in the Current RMS register when 1A current is applied, meaning 1.000 A with 1 mA resolution. Other given values are:

- The existing value for Gain Current RMS is 33480.
- The existing value for Range is 12.

By using Equation 9-1, the calculation for $Gain_{NEW}$ yields:

EQUATION 9-2:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{2300} = 14556$$

$$14556 < 20000$$

When using the `Auto-Calibration Gain` command, the result would be a failed calibration or a NAK returned form the MCP39F501, because the resulting $Gain_{NEW}$ is less than 20,000.

The solution is to use the Range register to bring the measured value closer to the expected value, such that a new gain value can be calculated within the limits specified above.

The Range register specifies the number of right-bit shifts (equivalent to divisions by 2) after the multiplication with the Gain Current RMS register. Refer to **Section 5.0 "Calculation Engine (CE) Description"** for information on the Range register.

Incrementing the Range register by 1 unit, an additional right-bit shift or ÷2 is included in the calculation. Increasing the current range from 12 to 13 yields the new measured Current RMS register value of 2300/2 = 1150. The expected (1000) and measured (1150) are much closer now, so the expected new gain should be within the limits:

EQUATION 9-3:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{1150} = 29113$$

$$20000 < 29113 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates Current RMS and returns an ACK.

It can be observed that the range can be set to 14 and the resulting new gain will still be within limits ($Gain_{NEW}$ = 58226). However, since this gain value is close to the limit of the 16-bit Gain register, variations from system to system (component tolerances, etc.) might create a scenario where the calibration is not successful on some units and there would be a yield issue. The best approach is to choose a range value that places the new gain in the middle of the bounds of the gain registers described above.

In a second example, when applying 1A, the user expects an output of 1.0000A with 0.1 mA resolution. The example is starting with the same initial values:

EQUATION 9-4:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{1000}{2300} = 145565$$

$$145565 < 65535$$

The $Gain_{NEW}$ is much larger than the 16-bit limit of 65535, so fewer right-bit shifts must be introduced to get the measured value closer to the expected value. The user needs to compute the number of bit shifts that will give a value lower than 65535. To estimate this number:

EQUATION 9-5:

$$\frac{145565}{65535} = 2.2$$

2.2 rounds to the closest integer value of 2. The range value changes to 12 – 2 = 10; there are 2 less right-bit shifts.

The new measured value will be 2300 x 2^2 = 9200.

EQUATION 9-6:

$$GAIN_{NEW} = GAIN_{OLD} \times \frac{Expected}{Measured} = 33480 \times \frac{10000}{9200} = 36391$$

$$20000 < 36391 < 65535$$

The resulting new gain is within the limits and the device successfully calibrates Current RMS and returns an ACK.

9.4 Calibrating the Phase Compensation Register (0x003E)

Phase compensation is provided to adjust for any phase delay between the current and voltage path. This procedure requires sinusoidal current and voltage waveforms, with a significant phase shift between them, and significant amplitudes. The recommended displacement power factor for calibration is 0.5. The procedure for calculating the phase compensation register is the following:

1. Determine what is the difference between the angle corresponding to the measured power factor (PF_{MEAS}) and the angle corresponding to the expected power factor (PF_{EXP}), in degrees.

EQUATION 9-7:

$$PF_{MEAS} = \frac{Value\ in\ PowerFactor\ Register}{32768}$$

$$ANGLE_{MEAS}(^\circ) = acos(PF_{MEAS}) \times \frac{180}{\Pi}$$

$$ANGLE_{EXP}(^\circ) = acos(PF_{EXP}) \times \frac{180}{\Pi}$$

2. Convert this from degrees to the resolution provided by the Equation 9-8:

EQUATION 9-8:

$$\Phi = (ANGLE_{MEAS} - ANGLE_{EXP}) \times 40$$

3. Combine this additional phase compensation to whatever value is currently in the phase compensation, and update the register. Equation 9-9 should be computed in terms of a 8-bit 2's complement signed value. The 8-bit result is placed in the least significant byte of the 16-bit Phase Compensation register (0x003E).

EQUATION 9-9:

$$PhaseCompensation_{NEW} = PhaseCompensation_{OLD} + \Phi$$

Based on Equation 9-9, the maximum angle in degrees that can be compensated is ±3.2 degrees. If a larger phase shift is required, contact your local Microchip sales office.

9.5 Reactive Power Calibration and Phase Compensation (Calibrations at Non-unity Power Factor)

In order to correctly calibrate the reactive power calculation through the Gain Reactive Power register (0x002E), and to properly correct for any phase error through the Phase Compensation register, the calibration must be done at a power factor other than PF = 1, typically at PF = 0.5.

9.5.1 USING THE AUTO-CALIBRATION REACTIVE GAIN COMMAND

By applying the equivalent current, voltage and phase lag (or lead) that correspond to the target reactive power in the Calibration Reactive Power register (0x0056), the `Auto-Calibration Gain` command (0x7A) can be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following register is set when the `Auto-Calibration Gain` command is issued:

- Gain Reactive Power

When this command is issued, the MCP39F501 attempts to match the expected value of the reactive power to the measured value of reactive power by changing the GainReactivePower register.

9.6 Offset/No Load Calibrations

During offset calibrations, no line voltage or current should be applied to the system. The system should be in a No Load condition.

9.6.1 AC OFFSET CALIBRATION

There are three registers associated with the AC Offset Calibration:

- Offset Current RMS(0x0030)
- Offset Active Power(0x0034)
- Offset Reactive Power(0x0038)

When computing the AC offset values, the respective gain and Range registers should be taken into consideration according to the block diagrams in Figures 5-2, 5-3 and 5-4.

After a successful offset calibration, a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

9.6.2 DC OFFSET CALIBRATION

In DC applications, the high-pass filter on the current and voltage channels is turned off. To remove any residual DC value on the current, the DCOffsetCurrent (0x003C) register adds to the A/D conversion immediately after the ADC and prior to any other function.

9.7 Calibrating the Line Frequency Register (0x0018)

The Line Frequency register contains a 16-bit number with a value equivalent to the input line frequency as it is measured on the voltage channel. When in DC mode, this calculation is turned off and the register will be equal to zero.

The measurement of the line frequency is only valid from 45 to 65 Hz.

9.7.1 USING THE Auto-Calibration Frequency COMMAND

By a applying stable reference voltage with a constant line frequency that is equivalent to the value that reside in the Line Frequency Ref (0x0094), the `Auto-Calibration Frequency` command can then be issued to the device.

After a successful calibration (response = ACK), a `Save Registers to Flash` command can then be issued to save the calibration constants calculated by the device.

The following register is set when the `Auto-Calibration Frequency` command is issued:

• Gain Line Frequency (0x00AE)

Note that the command is only required when running off the internal oscillator. The formula used to calculate the new gain is given in Equation 9-1.

9.8 Temperature Compensation (Addresses 0x00B0/B2/B4/B6)

MCP39F501 measures the indication of the temperature sensor and uses the value to compensate the temperature variation of the shunt resistance and the frequency of the internal RC oscillator.

The same formula applies for Line Frequency, Current RMS, Active Power and Reactive Power. The temperature compensation coefficient depends on the 16-bit signed integer value of the corresponding compensation register.

EQUATION 9-10:

$$y = x \times (1 + c \times (T - T_{CAL}))$$

$$c = \frac{Temperature Compensation\ Register}{2^M}$$

Where:

- x = Uncompensated Output (corresponding to Line Frequency, Current RMS, Active Power and Reactive Power)
- y = Compensated Output
- c = Temperature Compensation Coefficient (depending on the shunt's Temperature Coefficient of Resistance or on the internal RC oscillator temperature frequency drift)
- T = Thermistor Voltage (in 10-bit ADC units)
- T_{CAL} = Ambient Temperature Reference Voltage. It should be set at the beginning of the calibration procedure, by reading the thermistor voltage and writing its value to the ambient temperature reference voltage register.
- M = 26 (for Line Frequency compensation)
  = 27 (for Current, Active Power and Reactive Power)

At the calibration temperature, the effect of the compensation coefficients is minimal. The coefficients need to be tuned when the difference between the calibration temperature and the device temperature is significant. It is recommended to use the default values as starting points.

10.0 EEPROM

The data EEPROM is organized as 16-bit wide memory. Each word is directly addressable, and is readable and writable across the entire V_{DD} range. The MCP39F501 has 256 16-bit words of EEPROM that is organized in 32 pages for a total of 512 bytes.

There are three commands that support access to the EEPROM array.

- `EEPROM Page Read` (0x42)
- `EEPROM Page Write` (0x50)
- `EEPROM Bulk Erase` (0x4F)

TABLE 10-1: EXAMPLE EEPROM COMMANDS AND DEVICE RESPONSE

Command	Command ID BYTE 0	BYTE 1-N	# Bytes	Successful Response
`Page Read EEPROM`	0x42	PAGE	2	ACK, Data, CRC
`Page Write EEPROM`	0x50	PAGE + 16 BYTES OF DATA	18	ACK
`Bulk Erase EEPROM`	0x4F	---------	1	ACK

TABLE 10-2: MCP39F501 EEPROM ORGANIZATION

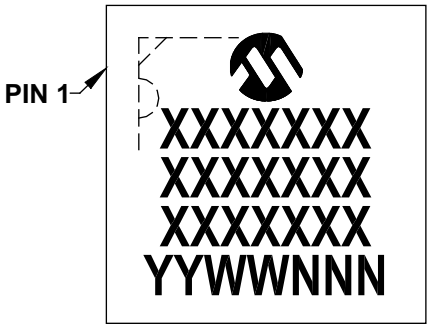
Page		00	02	04	06	08	0A	0C	0E
0	0000	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
1	0010	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
2	0020	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
3	0030	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
4	0040	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
5	0050	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
6	0060	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
7	0070	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
8	0080	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
9	0090	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
10	00A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
11	00B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
12	00C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
13	00D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
14	00E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
15	00F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
16	0100	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
17	0110	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
18	0120	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
19	0130	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
20	0140	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
21	0150	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
22	0160	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
23	0170	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
24	0180	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
25	0190	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
26	01A0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
27	01B0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
28	01C0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
29	01D0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
30	01E0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF
31	01F0	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF	FFFF

NOTES:

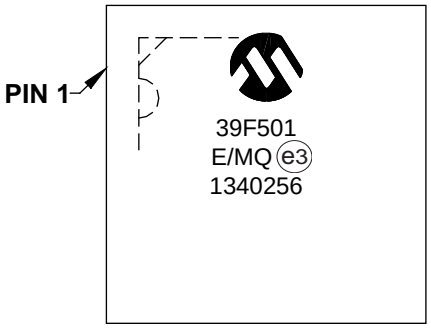
11.0 PACKAGING INFORMATION

11.1 Package Marking Information

28-Lead QFN (5x5x0.9 mm)



Example

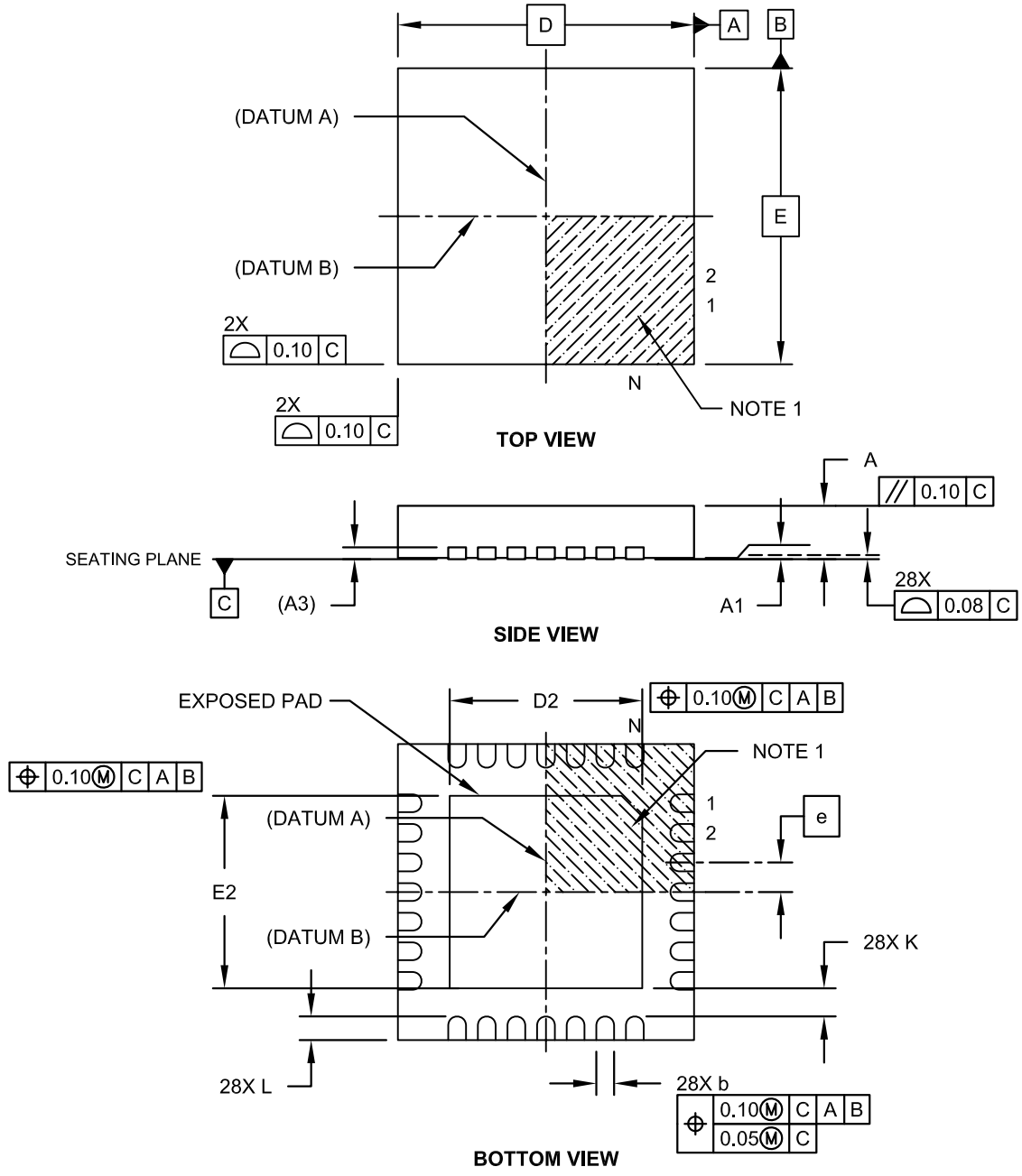


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

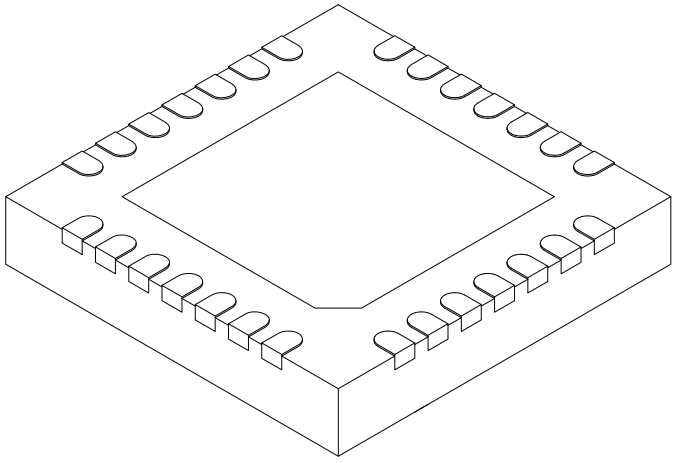
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-140B Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5x0.9 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		28	
Pitch	e		0.50 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.15	3.25	3.35
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.15	3.25	3.35
Contact Width	b	0.18	0.25	0.30
Contact Length	L	0.35	0.40	0.45
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

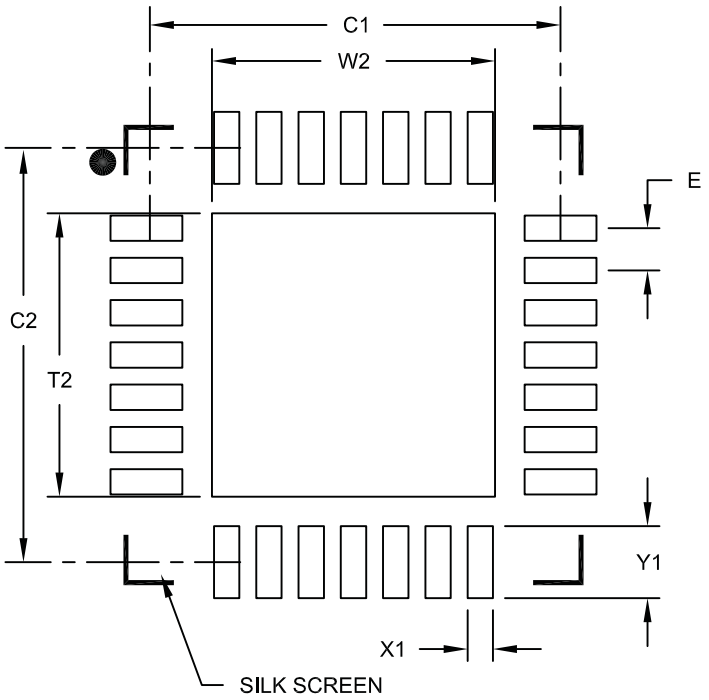
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-140B Sheet 2 of 2

28-Lead Plastic Quad Flat, No Lead Package (MQ) – 5x5 mm Body [QFN] Land Pattern With 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Optional Center Pad Width	W2			3.35
Optional Center Pad Length	T2			3.35
Contact Pad Spacing	C1		4.90	
Contact Pad Spacing	C2		4.90	
Contact Pad Width (X28)	X1			0.30
Contact Pad Length (X28)	Y1			0.85

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2140A

APPENDIX A: REVISION HISTORY

Revision A (December 2013)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	MCP39F501: Single Phase Energy and Power Monitoring IC with Calculation
Tape and Reel Option:	Blank = Standard packaging (tube or tray) T = Tape and Reel(1)
Temperature Range:	E = -40°C to +125°C
Package:	MQ = Plastic Quad Flat, No Lead Package – 5x5x0.9 mm Body (QFN)

Examples:

a) MCP39F501-E/MQ: Extended Temperature, 28LD 5x5 QFN package.

b) MCP39F501T-E/MQ: Tape and Reel, Extended Temperature, 28LD 5x5 QFN package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip sales office for package availability for the Tape and Reel option.

NOTES:

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