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# R8C/28 Group, R8C/29 Group SINGLE-CHIP 16-BIT CMOS MCU

REJ03B0169-0210 Rev.2.10 Sep 26, 2008

# 1. Overview

These MCUs are fabricated using a high-performance silicon gate CMOS process, embedding the R8C CPU core, and are packaged in a 20-pin molded-plastic LSSOP. It implements sophisticated instructions for a high level of instruction efficiency. With 1 Mbyte of address space, they are capable of executing instructions at high speed.

Furthermore, the R8C/29 Group has on-chip data flash (1 KB  $\times$  2 blocks).

The difference between the R8C/28 Group and R8C/29 Group is only the presence or absence of data flash. Their peripheral functions are the same.

# 1.1 Applications

Electronic household appliances, office equipment, audio equipment, consumer products, automotive, etc.



# 1.2 Performance Overview

Table 1.1 outlines the Functions and Specifications for R8C/28 Group and Table 1.2 outlines the Functions and Specifications for R8C/29 Group.

Table 1.1 Functions and Specifications for R8C/28 Group

	Item	Specification
CPU	Number of fundamental	89 instructions
	instructions	
	Minimum instruction	50 ns (f(XIN) = 20 MHz, VCC = 3.0 to 5.5 V) (other than K version)
	execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version)
		100 ns (f(XIN) = 10 MHz, VCC = 2.7 to 5.5 V)
		200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.3 Product Information for R8C/28 Group
Peripheral	Ports	I/O ports: 13 pins, Input port: 3 pins
Functions	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits × 1 channel
		Timer RB: 8 bits x 1 channel
		(Each timer equipped with 8-bit prescaler)
		Timer RC: 16 bits x 1 channel
		(Input capture and output compare circuits)
		Timer RE: With real-time clock and compare match function (For J, K version, compare match function only.)
	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART
	Serial interfaces	1 channel (UART1): UART
	Clock synchronous serial	1 channel
	interface	I <sup>2</sup> C bus Interface <sup>(1)</sup>
	Interface	Clock synchronous serial I/O with chip select
	LIN module	Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler)
	Watchdog timer	Reset start selectable
	Interrupts	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)
	interrupts	External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits
	Clock goneration chodite	XIN clock generation circuit (with on-chip feedback resistor)
		On-chip oscillator (high speed, low speed)
		High-speed on-chip oscillator has a frequency adjustment function
		XCIN clock generation circuit (32 kHz) (N, D version)
		Real-time clock (timer RE) (N, D version)
	Oscillation stop detection	XIN clock oscillation stop detection function
	function	·
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip On-chip
Electrical	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)
Characteristics		VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)
		VCC = 2.7  to  5.5  V  (f(XIN) = 10  MHz)
		VCC = 2.2  to  5.5  V  (f(XIN) = 5  MHz) (N, D  version)
	Current consumption	Typ. 10 mA (VCC = $5.0 \text{ V}$ , $f(XIN) = 20 \text{ MHz}$ )
	(N, D version)	Typ. 6 mA (VCC = $3.0 \text{ V}$ , $f(XIN) = 10 \text{ MHz}$ )
		Typ. 2.0 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)
CII- NA	December 1	Typ. 0.7 μA (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure endurance	100 times
Operating Ambie		-20 to 85°C (N version)
,	r	-40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>
Package		20-pin molded-plastic LSSOP
. aditago		1-0 p

- 1. I<sup>2</sup>C bus is a trademark of Koninklijke Philips Electronics N. V.
- 2. Specify the D, K version if D, K version functions are to be used.



Table 1.2 Functions and Specifications for R8C/29 Group

	Item	Specification
CPU	Number of fundamental	89 instructions
	instructions	
	Minimum instruction	50 ns ( $f(XIN) = 20 \text{ MHz}$ , VCC = 3.0 to 5.5 V) (other than K version)
	execution time	62.5 ns (f(XIN) = 16 MHz, VCC = 3.0 to 5.5 V) (K version)
		100 ns ( $f(XIN) = 10 \text{ MHz}$ , VCC = 2.7 to 5.5 V)
		200 ns (f(XIN) = 5 MHz, VCC = 2.2 to 5.5 V) (N, D version)
	Operating mode	Single-chip
	Address space	1 Mbyte
	Memory capacity	Refer to Table 1.4 Product Information for R8C/29 Group
Peripheral	Ports	I/O ports: 13 pins, Input port: 3 pins
Functions	LED drive ports	I/O ports: 8 pins (N, D version)
	Timers	Timer RA: 8 bits x 1 channel
		Timer RB: 8 bits x 1 channel
		(Each timer equipped with 8-bit prescaler)
		Timer RC: 16 bits x 1 channel
		(Input capture and output compare circuits)
		Timer RE: With real-time clock and compare match function
	Carial interferes	(For J, K version, compare match function only.)
	Serial interfaces	1 channel (UART0): Clock synchronous serial I/O, UART
	Clock overshrongua agrical	1 channel (UART1): UART 1 channel
	Clock synchronous serial interface	
	Interface	I <sup>2</sup> C bus Interface <sup>(1)</sup>
	LIN module	Clock synchronous serial I/O with chip select
		Hardware LIN: 1 channel (timer RA, UART0)
	A/D converter	10-bit A/D converter: 1 circuit, 4 channels
	Watchdog timer	15 bits × 1 channel (with prescaler) Reset start selectable
	Interrupte	Internal: 15 sources (N, D version), Internal: 14 sources (J, K version)
	Interrupts	External: 4 sources, Software: 4 sources, Priority levels: 7 levels
	Clock generation circuits	3 circuits
	Clock generation circuits	XIN clock generation circuit (with on-chip feedback resistor)
		On-chip oscillator (high speed, low speed)
		High-speed on-chip oscillator has a frequency adjustment function
		XCIN clock generation circuit (32 kHz) (N, D version)
		Real-time clock (timer RE) (N, D version)
	Oscillation stop detection	XIN clock oscillation stop detection function
	function	
	Voltage detection circuit	On-chip
	Power-on reset circuit	On-chip
Electrical	Supply voltage	VCC = 3.0 to 5.5 V (f(XIN) = 20 MHz) (other than K version)
Characteristics		VCC = 3.0 to 5.5 V (f(XIN) = 16 MHz) (K version)
		VCC = 2.7 to 5.5 V (f(XIN) = 10 MHz)
		VCC = 2.2 to 5.5 V (f(XIN) = 5 MHz) (N, D version)
	Current consumption	Typ. 10 mA (VCC = 5.0 V, f(XIN) = 20 MHz)
	(N, D version)	Typ. 6 mA (VCC = 3.0 V, f(XIN) = 10 MHz)
		Typ. 2.0 $\mu$ A (VCC = 3.0 V, wait mode (f(XCIN) = 32 kHz)
		Typ. 0.7 $\mu$ A (VCC = 3.0 V, stop mode)
Flash Memory	Programming and erasure voltage	VCC = 2.7 to 5.5 V
	Programming and erasure	10,000 times (data flash)
	endurance	1,000 times (program ROM)
Operating Ambie	ent Temperature	-20 to 85°C (N version)
	•	-40 to 85°C (D, J version) <sup>(2)</sup> , -40 to 125°C (K version) <sup>(2)</sup>
Package		20-pin molded-plastic LSSOP
		F

- 1.  $I^2C$  bus is a trademark of Koninklijke Philips Electronics N. V.
- 2. Specify the D, K version if D, K version functions are to be used.



# 1.3 Block Diagram

Figure 1.1 shows a Block Diagram.

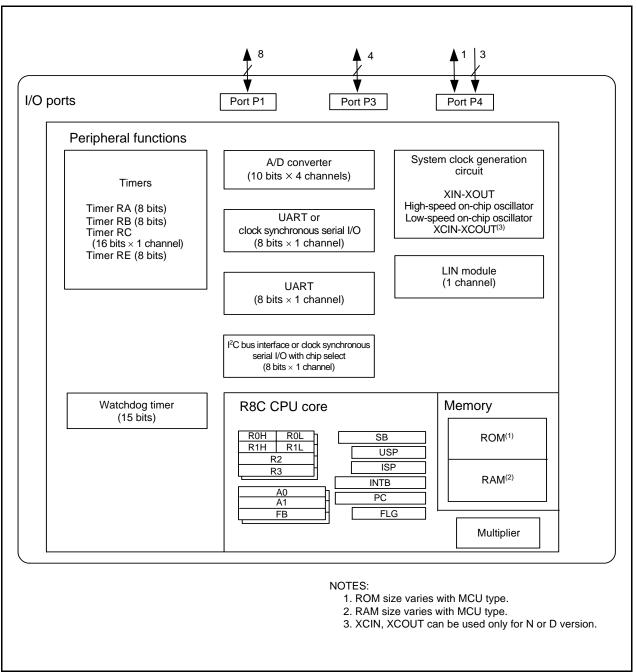


Figure 1.1 Block Diagram

#### 1.4 Product Information

Table 1.3 lists the Product Information for R8C/28 Group and Table 1.4 lists the Product Information for R8C/29 Group.

Table 1.3 Product Information for R8C/28 Group

Current of Sep. 2008

Type No.	ROM	RAM	Package Type	Ror	narks
Type No.	Capacity	Capacity	Tackage Type	Remarks	
R5F21282SNSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	
R5F21284SNSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21282SDSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	
R5F21284SDSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21284KSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		
R5F21282SNXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	N version	Factory
R5F21284SNXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		programming
R5F21282SDXXXSP	8 Kbytes	512 bytes	PLSP0020JB-A	D version	product <sup>(1)</sup>
R5F21284SDXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A		
R5F21284JXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	J version	
R5F21286JXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A	]	
R5F21284KXXXSP	16 Kbytes	1 Kbyte	PLSP0020JB-A	K version	
R5F21286KXXXSP	32 Kbytes	1.5 Kbyte	PLSP0020JB-A		

#### NOTE:

1. The user ROM is programmed before shipment.

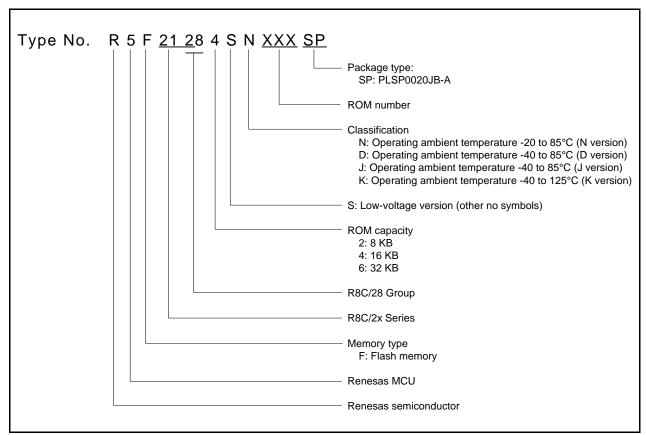


Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group

Table 1.4 Product Information for R8C/29 Group

#### Current of Sep. 2008

	ROM (	Capacity	RAM			
Type No.	Program ROM	Data flash	Capacity	Package Type	Re	marks
R5F21292SNSP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	N version	
R5F21294SNSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A		
R5F21292SDSP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	D version	
R5F21294SDSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A		
R5F21294JSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	J version	
R5F21296JSP	32 Kbytes	1 Kbyte x 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KSP	32 Kbytes	1 Kbyte x 2	1.5 Kbyte	PLSP0020JB-A		
R5F21292SNXXXSP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	N version	Factory
R5F21294SNXXXSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A		programming
R5F21292SDXXXSP	8 Kbytes	1 Kbyte x 2	512 bytes	PLSP0020JB-A	D version	product <sup>(1)</sup>
R5F21294SDXXXSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A		
R5F21294JXXXSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	J version	1
R5F21296JXXXSP	32 Kbytes	1 Kbyte x 2	1.5 Kbyte	PLSP0020JB-A		
R5F21294KXXXSP	16 Kbytes	1 Kbyte x 2	1 Kbyte	PLSP0020JB-A	K version	
R5F21296KXXXSP	32 Kbytes	1 Kbyte x 2	1.5 Kbyte	PLSP0020JB-A		

#### NOTE:

1. The user ROM is programmed before shipment.

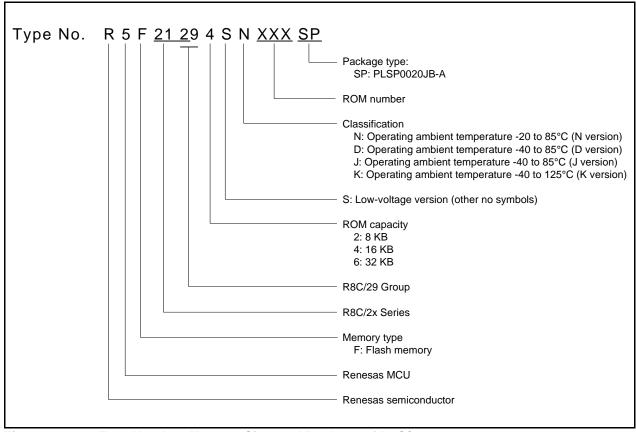


Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group

# 1.5 Pin Assignments

Figure 1.4 shows Pin Assignments (Top View).

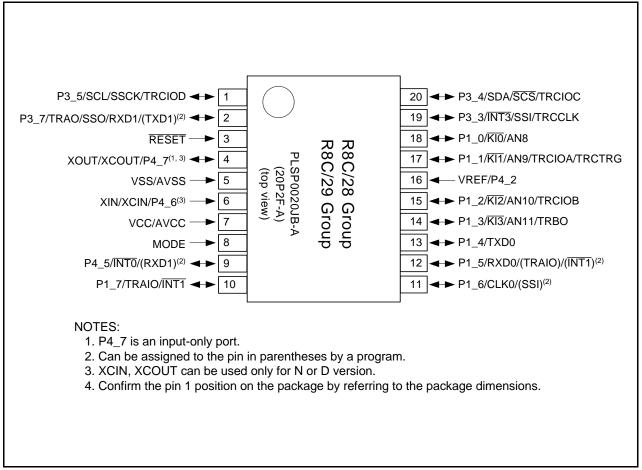


Figure 1.4 Pin Assignments (Top View)

#### 1.6 **Pin Functions**

Table 1.5 lists Pin Functions.

Table 1.5 **Pin Functions** 

Type	Symbol	I/O Type	Description	
Power supply input	VCC, VSS	I	Apply 2.2 to 5.5 V (J, K version are 2.7 to 5.5 V) to the VCC pin. Apply 0 V to the VSS pin.	
Analog power supply input	AVCC, AVSS	I	Power supply for the A/D converter. Connect a capacitor between AVCC and AVSS.	
Reset input	RESET	ı	Input "L" on this pin resets the MCU.	
MODE	MODE	I	Connect this pin to VCC via a resistor.	
XIN clock input	XIN	I	These pins are provided for XIN clock generation circuit Connect a ceramic resonator or a crystal oscillator between the XIN and XOUT pins. To use an external clock, input it	
XIN clock output	XOUT	0	the XIN and XOUT pins. To use an external clock, input it to the XIN pin and leave the XOUT pin open.	
XCIN clock input (N, D version)	XCIN	I	These pins are provided for XCIN clock generation circuit I/O. Connect a crystal oscillator between the XCIN and XCOUT	
XCIN clock output (N, D version)	XCOUT	0	pins. To use an external clock, input it to the XCIN pin and leave the XCOUT pin open.	
INT interrupt input	INTO, INT1, INT3	I	INT interrupt input pins	
Key input interrupt	KI0 to KI3	I	Key input interrupt input pins	
Timer RA	TRAO	0	Timer RA output pin	
	TRAIO	I/O	Timer RA I/O pin	
Timer RB	TRBO	0	Timer RB output pin	
Timer RC	TRCCLK	I	External clock input pin	
	TRCTRG	- 1	External trigger input pin	
	TRCIOA, TRCIOB, TRCIOC, TRCIOD	I/O	Sharing output-compare output / input-capture input / PWM / PWM2 output pins	
Serial interface	CLK0	I/O	Clock I/O pin	
	RXD0, RXD1	I	Receive data input pin	
	TXD0, TXD1	0	Transmit data output pin	
I <sup>2</sup> C bus interface	SCL	I/O	Clock I/O pin	
	SDA	I/O	Data I/O pin	
Clock synchronous	SSI	I/O	Data I/O pin	
serial I/O with chip	SCS	I/O	Chip-select signal I/O pin	
select	SSCK	I/O	Clock I/O pin	
	SSO	I/O	Data I/O pin	
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter	
A/D converter	AN8 to AN11	I	Analog input pins to A/D converter	
I/O port	P1_0 to P1_7, P3_3 to P3_5, P3_7, P4_5	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually.  Any port set to input can be set to use a pull-up resistor or not by a program.	
			P1_0 to P1_7 also function as LED drive ports (N, D version).	
Input port	P4_2, P4_6, P4_7	I	Input-only ports	

I: Input

O: Output

I/O: Input and output



Table 1.6 **Pin Name Information by Pin Number** 

			I/O Pin Functions for of Peripheral Modules					
Pin Number	Control Pin	Port	Interrupt	Timer	Serial Interface	Clock Synchronous Serial I/O with Chip Select	I <sup>2</sup> C bus Interface	A/D Converter
1		P3_5		TRCIOD		SSCK	SCL	
2		P3_7		TRAO	RXD1/(TXD1) <sup>(1)</sup>	SSO		
3	RESET							
4	XOUT/ XCOUT <sup>(2)</sup>	P4_7						
5	VSS/AVSS							
6	XIN/XCIN(2)	P4_6						
7	VCC/AVCC							
8	MODE							
9		P4_5	ĪNT0		(RXD1) <sup>(1)</sup>			
10		P1_7	ĪNT1	TRAIO				
11		P1_6			CLK0	(SSI) <sup>(1)</sup>		
12		P1_5	(INT1) <sup>(1)</sup>	(TRAIO) <sup>(1)</sup>	RXD0			
13		P1_4			TXD0			
14		P1_3	KI3	TRBO				AN11
15		P1_2	KI2	TRCIOB				AN10
16	VRFF	P4_2						
17		P1_1	KI1	TRCIOA/ TRCTRG				AN9
18		P1_0	KI0					AN8
19		P3_3	ĪNT3	TRCCLK		SSI		
20		P3_4		TRCIOC		SCS	SDA	

- This can be assigned to the pin in parentheses by a program.
   XCIN, XCOUT can be used only for N or D version.

#### 2. **Central Processing Unit (CPU)**

Figure 2.1 shows the CPU Registers. The CPU contains 13 registers. R0, R1, R2, R3, A0, A1, and FB configure a register bank. There are two sets of register bank.

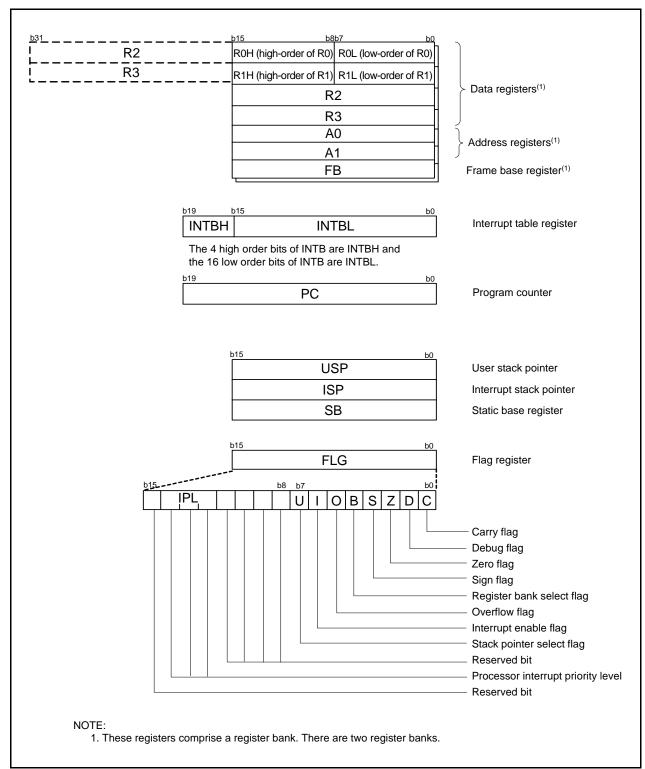


Figure 2.1 **CPU Registers** 

# 2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

### 2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

# 2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

# 2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of an interrupt vector table.

### 2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

# 2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP, and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

# 2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

### 2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

# 2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

### 2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

# 2.8.3 **Zero Flag (Z)**

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

# 2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

#### 2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

#### 2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.



# 2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.

Interrupt are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

# 2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.

The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

# 2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

#### 2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.



# 3. Memory

# 3.1 R8C/28 Group

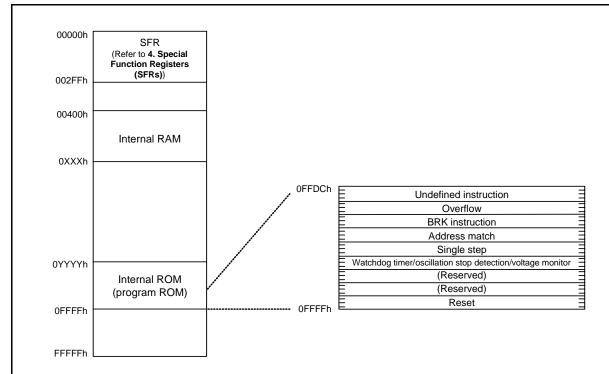
Figure 3.1 is a Memory Map of R8C/28 Group. The R8C/28 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

The internal ROM is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM area is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



#### NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

5	Internal ROM		Internal RAM	
Part Number	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21282SNSP, R5F21282SDSP, R5F21282SNXXXSP, R5F21282SDXXXSP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21284SNSP, R5F21284SDSP, R5F21284JSP, R5F21284KSP, R5F21284SNXXXSP, R5F21284SDXXXSP, R5F21284JXXXSP, R5F21284KXXXSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21286JSP, R5F21286KSP, R5F21286JXXXSP, R5F21286KXXXSP	32 Kbytes	08000h	1.5 Kbytes	009FFh

Figure 3.1 Memory Map of R8C/28 Group

#### 3.2 R8C/29 Group

Figure 3.2 is a Memory Map of R8C/29 Group. The R8C/29 group has 1 Mbyte of address space from addresses 00000h to FFFFFh.

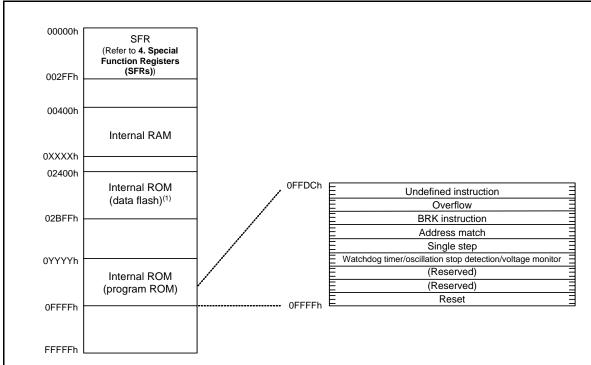
The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 16-Kbyte internal ROM area is allocated addresses 0C000h to 0FFFFh.

The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. They store the starting address of each interrupt routine.

The internal ROM (data flash) is allocated addresses 02400h to 02BFFh.

The internal RAM area is allocated higher addresses, beginning with address 00400h. For example, a 1-Kbyte internal RAM is allocated addresses 00400h to 007FFh. The internal RAM is used not only for storing data but also for calling subroutines and as stacks when interrupt requests are acknowledged.

Special function registers (SFRs) are allocated addresses 00000h to 002FFh. The peripheral function control registers are allocated here. All addresses within the SFR, which have nothing allocated are reserved for future use and cannot be accessed by users.



- 1. Data flash block A (1 Kbyte) and B (1 Kbyte) are shown.
- 2. The blank regions are reserved. Do not access locations in these regions.

Post Month on	Internal ROM		Internal RAM	
Part Number	Size	Address 0YYYYh	Size	Address 0XXXXh
R5F21292SNSP, R5F21292SDSP, R5F21292SNXXXSP, R5F21292SDXXXSP	8 Kbytes	0E000h	512 bytes	005FFh
R5F21294SNSP, R5F21294SDSP, R5F21294JSP, R5F21294KSP, R5F21294SNXXXSP, R5F21294SDXXXSP, R5F21294JXXXSP, R5F21294KXXXSP	16 Kbytes	0C000h	1 Kbyte	007FFh
R5F21296JSP, R5F21296KSP, R5F21296JXXXSP, R5F21296KXXXSP	32 Kbytes	08000h	1.5 Kbytes	009FFh

Figure 3.2 Memory Map of R8C/29 Group

# 4. Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 4.1 to 4.7 list the special function registers.

Table 4.1 SFR Information (1)<sup>(1)</sup>

Address	Register	Symbol	After reset
0000h			
0001h			
0002h			
0003h			
0004h	Processor Mode Register 0	PM0	00h
0005h	Processor Mode Register 1	PM1	00h
0006h	System Clock Control Register 0	CM0	01101000b
0007h	System Clock Control Register 1	CM1	00100000b
0008h			
0009h			
000Ah	Protect Register	PRCR	00h
000Bh			
000Ch	Oscillation Stop Detection Register	OCD	00000100b
000Dh	Watchdog Timer Reset Register	WDTR	XXh
000Eh	Watchdog Timer Start Register	WDTS	XXh
000Fh	Watchdog Timer Control Register	WDC	00X11111b
0010h	Address Match Interrupt Register 0	RMAD0	00h
0011h			00h
0012h			00h
0013h	Address Match Interrupt Enable Register	AIER	00h
0014h	Address Match Interrupt Register 1	RMAD1	00h
0015h			00h
0016h			00h
0017h			
0018h			
0019h			
001Ah			
001Bh			
001Ch	Count Source Protection Mode Register	CSPR	00h 10000000b <sup>(2)</sup>
001Dh			
001Eh			
001Fh			
0020h			
0021h			
0022h			
0023h	High-Speed On-Chip Oscillator Control Register 0	FRA0	00h
0024h	High-Speed On-Chip Oscillator Control Register 1	FRA1	When shipping
0025h	High-Speed On-Chip Oscillator Control Register 2	FRA2	00h
0026h			
0027h			
0028h	Clock Prescaler Reset Flag	CPSRF	00h
0029h	High-Speed On-Chip Oscillator Control Register 4(3)	FRA4	When shipping
002Ah			
002Bh	High-Speed On-Chip Oscillator Control Register 6(3)	FRA6	When shipping
002Ch	High-Speed On-Chip Oscillator Control Register 7(3)	FRA7	When shipping
002Dh			1
002Eh			
002Fh			

X: Undefined

- 1. The blank regions are reserved. Do not access locations in these regions.
- 2. The CSPROINI bit in the OFS register is set to 0.
- 3. In J, K version these regions are reserved. Do not access locations in these regions.

Table 4.2 SFR Information (2)<sup>(1)</sup>

Address	Register	Symbol	After reset
0030h			
0031h	Voltage Detection Register 1 <sup>(2)</sup>	VCA1	00001000b
0032h	Voltage Detection Register 2 <sup>(2)</sup>	VCA2	N, D version 00h <sup>(3)</sup>
			00100000b <sup>(4)</sup>
			• J, K version 00h <sup>(7)</sup>
			01000000b <sup>(8)</sup>
0033h			01000000000
0033H			
003411 0035h			
0035h	Value of Manitan A Circuit Control Denistra(5)	VW1C	• N, D version 00001000b
003611	Voltage Monitor 1 Circuit Control Register <sup>(5)</sup>	VVVIC	T
			• J, K version 0000X000b(7)
	7-1		0100X001b <sup>(8)</sup>
0037h	Voltage Monitor 2 Circuit Control Register <sup>(5)</sup>	VW2C	00h
0038h	Voltage Monitor 0 Circuit Control Register <sup>(6)</sup>	VW0C	0000X000b <sup>(3)</sup>
			0100X001b <sup>(4)</sup>
0039h			
		•	<u> </u>
003Fh			
0040h			
0041h			
0042h			
0043h			
0044h			
0045h			
0046h			
0047h	Timer RC Interrupt Control Register	TRCIC	XXXXX000b
0048h			
0049h			
004Ah	Timer RE Interrupt Control Register	TREIC	XXXXX000b
004Bh			
004Ch			
004Dh	Key Input Interrupt Control Register	KUPIC	XXXXX000b
004Eh	A/D Conversion Interrupt Control Register	ADIC	XXXXX000b
004Fh	SSU/IIC bus Interrupt Control Register <sup>(9)</sup>	SSUIC/IICIC	XXXXX000b
0050h	3		
0051h	UART0 Transmit Interrupt Control Register	SOTIC	XXXXX000b
0052h	UARTO Receive Interrupt Control Register	SORIC	XXXXX000b
0053h	UART1 Transmit Interrupt Control Register	S1TIC	XXXXX000b
0054h	UART1 Receive Interrupt Control Register	S1RIC	XXXXX000b
0055h			
0056h	Timer RA Interrupt Control Register	TRAIC	XXXXX000b
0057h	Times to times apt control register		7,000,000
0058h	Timer RB Interrupt Control Register	TRBIC	XXXXX000b
0059h	INT1 Interrupt Control Register	INT1IC	XX00X000b
005Ah	INT3 Interrupt Control Register	INT3IC	XX00X000b
005Bh	and and appropriate the second		1
005Ch	+		<del> </del>
005Dh	INT0 Interrupt Control Register	INTOIC	XX00X000b
005Eh		1141010	7.5100/10005
005Eh			
0060h			
000011		L	
006Fh			
0070h			
007011			
007Fh	T		
K: Undefined			

- 1. The blank regions are reserved. Do not access locations in these regions.
- 2. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register. (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect this register.
- 3. The LVD0ON bit in the OFS register is set to 1 and hardware reset.
- 4. Power-on reset, voltage monitor 0 reset, or the LVD00N bit in the OFS register is set to 0 and hardware reset.
- 5. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect b2 and b3. (J, K version) Software reset, watchdog timer reset, or voltage monitor 2 reset do not affect b2 and b3.
- 6. (N, D version) Software reset, watchdog timer reset, voltage monitor 1 reset, or voltage monitor 2 reset do not affect this register. (J, K version) These regions are reserved. Do not access locations in these regions.
- 7. The LVD1ON bit in the OFS register is set to 1 and hardware reset.
- 8. Power-on reset, voltage monitor 1 reset, or the LVD10N bit in the OFS register is set to 0 and hardware reset.
- 9. Selected by the IICSEL bit in the PMR register.



SFR Information (3)<sup>(1)</sup> Table 4.3

Address	Register	Symbol	After reset
0080h	i rogisto.		7 11.0. 10001
0081h			
0082h			
0083h			
0084h			
0085h			
0086h			
0087h			
0088h			
0089h			
008Ah			
008Bh			
008Ch			
008Dh			
008Eh			
008Fh			
0090h			
0091h			
0092h			
0093h			
0094h			
0095h			
0096h			
0097h			
0098h			
0099h			
009Ah			
009Bh			
009Ch			
009Dh			
009Eh			
009Fh		LIONAR	
00A0h	UARTO Transmit/Receive Mode Register	U0MR	00h
00A1h	UARTO Bit Rate Register	U0BRG	XXh
00A2h	UART0 Transmit Buffer Register	U0TB	XXh
00A3h	LIADTO Transmit/Descript Control Descriptor O	11000	XXh
00A4h	UART0 Transmit/Receive Control Register 0	U0C0	00001000b
00A5h 00A6h	UART0 Transmit/Receive Control Register 1	U0C1 U0RB	00000010b XXh
00A6fi 00A7h	UART0 Receive Buffer Register	UURB	XXh
00A711	LIADTA Transmit/Dessive Made Desister	U1MR	00h
00A9h	UART1 Transmit/Receive Mode Register UART1 Bit Rate Register	U1BRG	XXh
00A9H	UART1 Transmit Buffer Register	U1TB	XXh
00AAII 00ABh	Onter Transmit Duller Negleter	0110	XXh
00ABII	UART1 Transmit/Receive Control Register 0	U1C0	00001000b
00ACH	UART1 Transmit/Receive Control Register 1	U1C1	00001000b
00AEh	UART1 Receive Buffer Register	U1RB	XXh
00AFh	The state of the		XXh
00B0h			
00B1h			
00B2h			
00B3h			
00B4h			
00B5h			
00B6h			
00B7h			
00B8h	SS Control Register H / IIC bus Control Register 1 <sup>(2)</sup>	SSCRH / ICCR1	00h
00B9h	SS Control Register L / IIC bus Control Register 2 <sup>(2)</sup>	SSCRL / ICCR2	01111101b
00BAh	SS Mode Register / IIC bus Mode Register <sup>(2)</sup>	SSMR / ICMR	00011000b
00BBh	SS Enable Register / IIC bus Interrupt Enable Register <sup>(2)</sup>	SSER / ICIER	00h
00BCh	SS Status Register / IIC bus Status Register <sup>(2)</sup>	SSSR / ICSR	00h / 0000X000b
00BDh	SS Mode Register 2 / Slave Address Register <sup>(2)</sup>	SSMR2 / SAR	00h
00BDH		SSTDR / ICDRT	FFh
	SS Transmit Data Register / IIC bus Transmit Data Register (2)	SSRDR / ICDRT	
00BFh X: Undefined	SS Receive Data Register / IIC bus Receive Data Register <sup>(2)</sup>	SOKUK / ICUKK	FFh

X: Undefined

- NOTES:

  1. The blank regions are reserved. Do not access locations in these regions.
  2. Selected by the IICSEL bit in the PMR register.

SFR Information (4)<sup>(1)</sup> Table 4.4

Address	Register	Symbol	After reset
00C0h	A/D Register	AD	XXh
00C1h	- No Register	AB.	XXh
00C2h			7001
00C3h			
00C3h			
00C4n		<u> </u>	
00C6h		+	
00C7h			
00C7h			
00C9h			
00CAh			
00CBh			
00CCh			
00CDh			
00CEh			
00CFh			
00D0h			
00D1h			
00D2h			
00D3h			
00D4h	A/D Control Register 2	ADCON2	00h
00D5h		İ	
00D6h	A/D Control Register 0	ADCON0	00h
00D7h	A/D Control Register 1	ADCON1	00h
00D8h	, , , , , , , , , , , , , , , , , , ,		
00D9h			
00DAh			
00DBh			
00DCh			
00DDh		+	
00DEh			
00DEII			
00E0h			
	Don't DA Don't to	D4	201-
00E1h	Port P1 Register	P1	00h
00E2h	D (D(D) () D ()	DD4	1001
00E3h	Port P1 Direction Register	PD1	00h
00E4h	B . B B B . L .		
00E5h	Port P3 Register	P3	00h
00E6h			
00E7h	Port P3 Direction Register	PD3	00h
00E8h	Port P4 Register	P4	00h
00E9h			
00EAh	Port P4 Direction Register	PD4	00h
00EBh			
00ECh			
00EDh			
00EEh			
00EFh			
00F0h			
00F1h			
00F2h			
00F3h			
00F4h		+	<del>-  </del>
00F5h	Pin Select Register 1	PINSR1	00h
00F6h	Pin Select Register 2	PINSR2	00h
00F7h	Pin Select Register 3	PINSR3	00h
00F8h	Port Mode Register	PMR	00h
00F9h	External Input Enable Register	INTEN	00h
	INT Input Eilter Select Pegister		
00FAh	INT Input Filter Select Register	INTF	00h
00FBh	Key Input Enable Register	KIEN	00h
00FCh	Pull-Up Control Register 0	PUR0	00h
00FDh	Pull-Up Control Register 1	PUR1	00h
00FEh 00FFh	Port P1 Drive Capacity Control Register <sup>(2)</sup>	P1DRR	00h

X: Undefined

2. In J, K version these regions are reserved. Do not access locations in these regions.

<sup>1.</sup> The blank regions are reserved. Do not access locations in these regions.

SFR Information (5)<sup>(1)</sup> Table 4.5

Address	Register	Symbol	After reset
0100h	Timer RA Control Register	TRACR	00h
0101h	Timer RA I/O Control Register	TRAIOC	00h
0102h	Timer RA Mode Register	TRAMR	00h
0103h	Timer RA Prescaler Register	TRAPRE	FFh
0104h	Timer RA Register	TRA	FFh
0105h			
0106h	LIN Control Register	LINCR	00h
0100h	LIN Status Register	LINST	00h
0108h	Timer RB Control Register	TRBCR	00h
0109h	Timer RB One-Shot Control Register	TRBOCR	00h
010Ah	Timer RB I/O Control Register	TRBIOC	00h
010Bh	Timer RB Mode Register	TRBMR	00h
010Ch	Timer RB Prescaler Register	TRBPRE	FFh
010Dh	Timer RB Secondary Register	TRBSC	FFh
010Eh	Timer RB Primary Register	TRBPR	FFh
010Fh	Times the state of the state	1112111	1
0110h			
0111h			
0112h			
0113h			
0114h			
0115h			
0116h			
0117h			
0118h	Timer RE Second Data Register / Counter Data Register	TRESEC	00h
0119h	Timer RE Minute Data Register / Compare Data Register	TREMIN	00h
			00h
011Ah	Timer RE Hour Data Register <sup>(2)</sup>	TREHR	
011Bh	Timer RE Day of Week Data Register <sup>(2)</sup>	TREWK	00h
011Ch	Timer RE Control Register 1	TRECR1	00h
011Dh	Timer RE Control Register 2	TRECR2	00h
011Eh	Timer RE Count Source Select Register	TRECSR	00001000b
011Fh	········		
0120h	Timer RC Mode Register	TRCMR	01001000b
012011 0121h	Timer RC Control Register 1		
		TRCCR1	00h
0122h	Timer RC Interrupt Enable Register	TRCIER	01110000b
0123h	Timer RC Status Register	TRCSR	01110000b
0124h	Timer RC I/O Control Register 0	TRCIOR0	10001000b
0125h	Timer RC I/O Control Register 1	TRCIOR1	10001000b
0126h	Timer RC Counter	TRC	00h
0127h		1112	00h
0128h	Timer RC General Register A	TRCGRA	FFh
0129h	Timer No General Negister /	moore	FFh
	Time and DO Comment Deminton D	TDCCDD	FFh
012Ah	Timer RC General Register B	TRCGRB	
012Bh			
012Ch	T DOO ID II D	TD	FFh
	Timer RC General Register C	TRCGRC	FFh
012Dh			FFh FFh
012Eh	Timer RC General Register C Timer RC General Register D	TRCGRC	FFh
			FFh FFh
012Eh	Timer RC General Register D		FFh FFh FFh
012Eh 012Fh 0130h	Timer RC General Register D Timer RC Control Register 2	TRCGRD TRCCR2	FFh FFh FFh FFh
012Eh 012Fh 0130h 0131h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h	Timer RC General Register D Timer RC Control Register 2	TRCGRD TRCCR2	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 0139h	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 013Ah 013Bh	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 013Ah 013Bh 013Bh 013Bh 013Bh 013Dh	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b
012Eh 012Fh 0130h 0131h 0132h 0133h 0134h 0135h 0136h 0137h 0138h 0139h 013Ah 013Bh	Timer RC General Register D  Timer RC Control Register 2  Timer RC Digital Filter Function Select Register	TRCGRD TRCCR2 TRCDF	FFh FFh FFh FFh 000111111b

- The blank regions are reserved. Do not access locations in these regions.
   In J, K version these regions are reserved. Do not access locations in these regions.

SFR Information (6)<sup>(1)</sup> Table 4.6

Address	Register	Symbol	After reset
0140h	Negistei	Symbol	Aiter reset
0141h			
0141h			
0142h			
0143h			
0144H			
0145h			
01460			
0147h			
0148h			
0149h			
014Ah			
014Bh			
014Ch			
014Dh			
014Eh			
014Fh			
0150h			
0151h			
0152h			
0153h			
0154h			
0155h			
0156h			
0157h			
0158h			
0159h			
015Ah			
015Bh			
015Ch			
015Dh			
015Eh			
015Fh			
0160h			
0161h			
0162h			
0163h			
0164h			
0165h			
0166h			
0167h			
0168h			
0169h			
016Ah			
016Bh			
016Ch			
016Dh			
016Eh			
016Fh			
0170h			
0171h			
0171h			
0172h			
0173h			
017411 0175h			
0176h			
0177h			
0177h 0178h			
0178h 0179h			
017Ah			
017Bh			
017Ch			
017Dh			
017Eh			
017Fh			
NOTE:			

NOTE:

1. The blank regions are reserved. Do not access locations in these regions.

Table 4.7 SFR Information (7)<sup>(1)</sup>

Address	Register	Symbol	After reset
0180h	9	ŕ	
0181h			
0182h			
0183h			
0184h			
0185h			
0186h			
0187h			
0188h			
0189h			
018Ah			
018Bh			
018Ch			
018Dh			
018Eh			
018Fh			
0190h			
0191h			
0192h			
0193h			
0194h			
0195h			
0196h			
0197h			
0198h			
0199h			
019Ah			
019Bh			
019Ch			
019Dh			
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			1
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Floob Momony Control Projector 4	EMD4	0100000h
01B3h 01B4h	Flash Memory Control Register 4	FMR4	01000000b
01B4fi 01B5h	Flash Memory Control Register 1	FMR1	1000000Xb
01B5H	I radii womery Control (Cegister 1	1 IVIIX I	100000000
01B0H	Flash Memory Control Register 0	FMR0	00000001b
01B7fi	i idan manary control register o	I IVIINO	000000010
01B9h			
01BAh			
01BBh			1
01BCh			
01BDh			
01BEh			
01BFh			
0.0111	1	<u> </u>	1
	LOsting Function Colort Posister	LOFO	[ (NI=4= 0)
FFFFh	Option Function Select Register	OFS	(Note 2)
Y. Undofined			

FFFFh X: Undefined

NOTES:

<sup>1.</sup> The blank regions are reserved. Do not access locations in these regions.

<sup>2.</sup> The OFS register cannot be changed by a program. Use a flash programmer to write to it.

# 5. Electrical Characteristics

# 5.1 N, D Version

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	Topr = 25°C	500	mW
Topr	Operating ambient temperature		-20 to 85 (N version) / -40 to 85 (D version)	°C
Tstg	Storage temperature		-65 to 150	°C

**Table 5.2** Recommended Operating Conditions

Company of	Darameter	Conditions		Standard		Linit	
Symbol	1	Parameter	Conditions	Min.	Тур.	Max.	Unit
Vcc/AVcc	Supply voltage			2.2	-	5.5	V
Vss/AVss	Supply voltage			-	0	-	V
VIH	Input "H" voltage			0.8 Vcc	=	Vcc	V
VIL	Input "L" voltage			0	=	0.2 Vcc	V
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		_	_	-160	mA
IOH(sum)	Average sum output "H" current	Sum of all pins IOH(avg)		_	_	-80	mA
IOH(peak)	Peak output "H"	Except P1_0 to P1_7		-	=	-10	mA
	current	P1_0 to P1_7		-	-	-40	mA
IOH(avg)	Average output	Except P1_0 to P1_7		_	_	-5	mA
	"H" current	P1_0 to P1_7		_	_	-20	mA
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		=	-	160	mA
IOL(sum)	Average sum output "L" currents	Sum of all pins IOL(avg)		=	_	80	mA
IOL(peak)	Peak output "L"	Except P1_0 to P1_7		_	-	10	mA
	currents	P1_0 to P1_7		_	=	40	mA
IOL(avg)	Average output	Except P1_0 to P1_7		_	=	5	mA
	"L" current	P1_0 to P1_7		-	-	20	mA
f(XIN)	XIN clock input osc	cillation frequency	3.0 V ≤ Vcc ≤ 5.5 V	0	-	20	MHz
			2.7 V ≤ Vcc < 3.0 V	0	-	10	MHz
			2.2 V ≤ Vcc < 2.7 V	0	-	5	MHz
f(XCIN)	XCIN clock input o	scillation frequency	2.2 V ≤ Vcc ≤ 5.5 V	0	-	70	kHz
_	System clock	OCD2 = 0	3.0 V ≤ Vcc ≤ 5.5 V	0	-	20	MHz
		XIN clock selected	2.7 V ≤ Vcc < 3.0 V	0	-	10	MHz
			2.2 V ≤ Vcc < 2.7 V	0	=	5	MHz
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	-	125	-	kHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 3.0 V ≤ Vcc ≤ 5.5 V	-	-	20	MHz
			FRA01 = 1 High-speed on-chip oscillator clock selected 2.7 V ≤ Vcc ≤ 5.5 V	_	=	10	MHz
NOTES:			FRA01 = 1 High-speed on-chip oscillator clock selected 2.2 V ≤ Vcc ≤ 5.5 V	=	-	5	MHz

<sup>1.</sup> Vcc = 2.2 to 5.5 V at Topr = -20 to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), unless otherwise specified.

<sup>2.</sup> The average output current indicates the average value of current measured during 100 ms.

Table 5.3	A/D Converter	Characteristics
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Symbol	Parameter	Conditions	Standard			Unit	
Symbol	'	- arameter	Conditions		Тур.	Max.	Offic
-	Resolution		Vref = AVCC	-	-	10	Bits
-	Absolute	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	-	-	±3	LSB
	accuracy	8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	-	-	±2	LSB
		10-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	-	-	±5	LSB
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	-	-	±2	LSB
		10-bit mode	φAD = 5 MHz, Vref = AVCC = 2.2 V	-	-	±5	LSB
		8-bit mode	φAD = 5 MHz, Vref = AVCC = 2.2 V	-	-	±2	LSB
Rladder	Resistor ladder		Vref = AVCC	10	-	40	kΩ
tconv	Conversion time	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	3.3	-	-	μS
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	2.8	-	-	μS
Vref	Reference voltag	e		2.2	-	AVcc	V
VIA	Analog input volta	age <sup>(2)</sup>		0	=	AVcc	V
-	A/D operating	Without sample and hold	Vref = AVCC = 2.7 to 5.5 V	0.25	_	10	MHz
	clock frequency	With sample and hold	Vref = AVCC = 2.7 to 5.5 V	1	-	10	MHz
		Without sample and hold	Vref = AVCC = 2.2 to 5.5 V	0.25	-	5	MHz
		With sample and hold	Vref = AVCC = 2.2 to 5.5 V	1	-	5	MHz

- 1. AVCC = 2.2 to 5.5 V at  $T_{OPT}$  = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

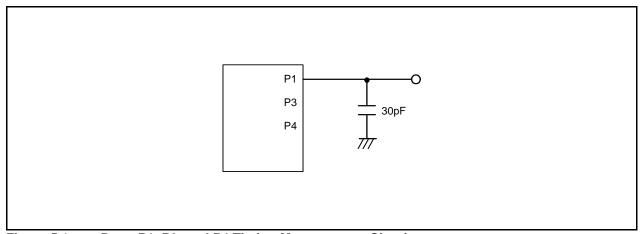


Figure 5.1 Ports P1, P3, and P4 Timing Measurement Circuit

Table 5.4 Flash Memory (Program ROM) Electrical Characteristics

Symbol	Parameter	Conditions		Unit		
Syllibol		Conditions	Min.	Тур.	Max.	Unit
_	Program/erase endurance <sup>(2)</sup>	R8C/28 Group	100(3)	=	=	times
		R8C/29 Group	1,000(3)	-	-	times
-	Byte program time		-	50	400	μS
=	Block erase time		=	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		_	_	97 + CPU clock × 6 cycles	μS
=	Interval from erase start/restart until following suspend request		650	=	_	μS
=	Interval from program start/restart until following suspend request		0	=	_	ns
=	Time from suspend until program/erase restart		=	=	3 + CPU clock × 4 cycles	μS
-	Program, erase voltage		2.7	-	5.5	V
_	Read voltage		2.2	-	5.5	V
_	Program, erase temperature		0	-	60	°C
_	Data hold time <sup>(7)</sup>	Ambient temperature = 55°C	20	_		year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.5 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions		Unit		
Symbol	Falanielei	Conditions	Min. Typ. Max		Max.	Offic
-	Program/erase endurance <sup>(2)</sup>		10,000(3)	_	-	times
_	Byte program time (program/erase endurance ≤ 1,000 times)		-	50	400	μS
_	Byte program time (program/erase endurance > 1,000 times)		-	65	-	μ\$
_	Block erase time (program/erase endurance ≤ 1,000 times)		-	0.2	9	S
_	Block erase time (program/erase endurance > 1,000 times)		-	0.3	_	S
td(SR-SUS)	Time delay from suspend request until suspend		-	=	97 + CPU clock × 6 cycles	μ\$
_	Interval from erase start/restart until following suspend request		650	=	_	μS
_	Interval from program start/restart until following suspend request		0	-	_	ns
_	Time from suspend until program/erase restart		-	=	3 + CPU clock × 4 cycles	μS
=	Program, erase voltage		2.7	_	5.5	V
=	Read voltage		2.2	_	5.5	V
=	Program, erase temperature		-20 <sup>(8)</sup>	-	85	°C
=	Data hold time <sup>(9)</sup>	Ambient temperature = 55°C	20	-	=	year

- 1. Vcc = 2.7 to 5.5 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.
  - If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
  - However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 8. -40°C for D version.
- 9. The data hold time includes time that the power supply is off or the clock is not supplied.

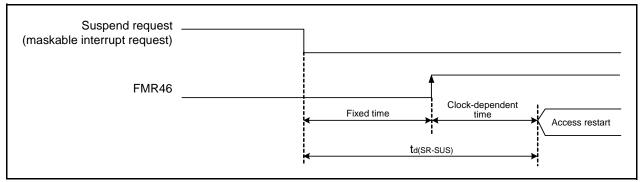


Figure 5.2 Time delay until Suspend

Table 5.6 **Voltage Detection 0 Circuit Electrical Characteristics** 

Symbol	Parameter	Condition		Unit		
Syllibol	Falametei	Condition	Min.	Тур.	Max.	Offic
Vdet0	Voltage detection level		2.2	2.3	2.4	V
-	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	-	0.9	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(2)</sup>		=	=	300	μS
Vccmin	MCU operating voltage minimum value		2.2	=	=	V

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 5.7 **Voltage Detection 1 Circuit Electrical Characteristics** 

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level <sup>(4)</sup>		2.70	2.85	3.00	V
-	Voltage monitor 1 interrupt request generation time <sup>(2)</sup>		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	-	0.6	-	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		=	=	100	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 1 interrupt request is generated after the voltage passes Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.

Table 5.8 **Voltage Detection 2 Circuit Electrical Characteristics** 

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max. 3.9	Offic
Vdet2	Voltage detection level		3.3	3.6	3.9	V
-	Voltage monitor 2 interrupt request generation time <sup>(2)</sup>		_	40	_	μS
=	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	-	0.6	-	μА
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		II	=	100	μ\$

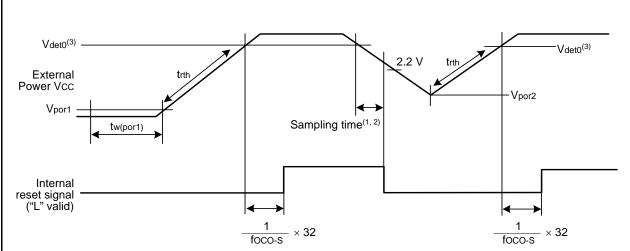
- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = -20 to 85°C (N version) / -40 to 85°C (D version).
- 2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes Vdet2.
- 3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.



Table 5.9	Power-on Reset Circuit.	<b>Voltage Monitor 0 Reset Electrical Characteristics</b> (3)

Svmbol	Parameter	Condition		Standard		Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vpor1	Power-on reset valid voltage <sup>(4)</sup>		_	-	0.1	V
Vpor2	Power-on reset or voltage monitor 0 reset valid voltage		0	_	Vdet0	V
trth	External power Vcc rise gradient(2)		20	_	_	mV/msec

- 1. The measurement condition is Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.
- 2. This condition (external power Vcc rise gradient) does not apply if  $Vcc \ge 1.0 \text{ V}$ .
- 3. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVD0ON bit in the OFS register to 0, the VW0C0 and VW0C6 bits in the VW0C register to 1 respectively, and the VCA25 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if -20°C ≤ Topr ≤ 85°C, maintain tw(por1) for 3,000 s or more if  $-40^{\circ}C \le T_{opr} < -20^{\circ}C$ .



- 1. When using the voltage monitor 0 digital filter, ensure that the voltage is within the MCU operation voltage range (2.2 V or above) during the sampling time.

  2. The sampling clock can be selected. Refer to **6. Voltage Detection Circuit** of Hardware Manual for details.
- Vdeto indicates the voltage detection level of the voltage detection 0 circuit. Refer to 6. Voltage Detection Circuit of Hardware Manual for details.

**Reset Circuit Electrical Characteristics** Figure 5.3

**Table 5.10 High-speed On-Chip Oscillator Circuit Electrical Characteristics** 

Cymphol	Darameter	Condition		Standard		Unit
Symbol	Parameter	Condition	Min.	Тур.	Max.	Unit
fOCO40M	High-speed on-chip oscillator frequency	Vcc = 4.75 to 5.25 V	39.2	40	40.8	MHz
	temperature • supply voltage dependence	$0^{\circ}C \leq T_{opr} \leq 60^{\circ}C^{(2)}$				
		Vcc = 3.0  to  5.5  V	38.8	40	41.2	MHz
		$-20^{\circ}C \leq T_{opr} \leq 85^{\circ}C^{(2)}$				
		Vcc = 3.0  to  5.5  V	38.4	40	41.6	MHz
		$-40$ °C $\leq$ Topr $\leq$ 85°C <sup>(2)</sup>				
		Vcc = 2.7  to  5.5  V	38	40	42	MHz
		$-20^{\circ}C \le T_{opr} \le 85^{\circ}C^{(2)}$				
		Vcc = 2.7  to  5.5  V	37.6	40	42.4	MHz
		$-40$ °C $\leq$ Topr $\leq$ 85°C(2)				
		Vcc = 2.2 to 5.5 V	35.2	40	44.8	MHz
		$-20^{\circ}C \leq Topr \leq 85^{\circ}C^{(3)}$				
		Vcc = 2.2 to 5.5 V	34	40	46	MHz
		$-40^{\circ}C \leq Topr \leq 85^{\circ}C^{(3)}$				
		$Vcc = 5.0 V \pm 10\%$	38.8		MHz	
		$-20^{\circ}C \le Topr \le 85^{\circ}C^{(2)}$				
		$Vcc = 5.0 V \pm 10\%$	38.4	40	44.8	MHz
		$-40^{\circ}C \leq Topr \leq 85^{\circ}C^{(2)}$				
	High-speed on-chip oscillator frequency when	$Vcc = 5.0 \text{ V}, Topr = 25^{\circ}C$	_	36.864	_	MHz
	correction value in FRA7 register is written to FRA1 register <sup>(4)</sup>	Vcc = 3.0 to 5.5 V -20°C ≤ Topr ≤ 85°C	-3%	_	3%	%
_	Value in FRA1 register after reset		08h <sup>(3)</sup>	-	F7h <sup>(3)</sup>	-
=	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	-	+0.3	-	MHz
_	Oscillation stability time		_	10	41.2 41.6 42 42.4 44.8 46 40.8 40.8	μS
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	400	-	μА

- 1. Vcc = 2.2 to 5.5 V,  $T_{opr} = -20$  to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), unless otherwise specified.
- 2. These standard values show when the FRA1 register value after reset is assumed.
- 3. These standard values show when the corrected value of the FRA6 register is written to the FRA1 register.
- 4. This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.

**Table 5.11** Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Standard			
Symbol	Falametei	Condition	Min.	Тур.	Max.	Unit	
fOCO-S	Low-speed on-chip oscillator frequency		30	125	250	kHz	
_	Oscillation stability time		_	10	100	μS	
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	_	15	-	μА	

1. Vcc = 2.2 to 5.5 V,  $T_{opr} = -20$  to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), unless otherwise specified.

**Table 5.12 Power Supply Circuit Timing Characteristics** 

Symbol	Parameter	Condition	,	Unit		
Symbol	Falametei	Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on <sup>(2)</sup>		1	=	2000	μS
td(R-S)	STOP exit time <sup>(3)</sup>		=	-	150	μS

- 1. The measurement condition is Vcc = 2.2 to 5.5 V and Topr = 25°C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.



**Table 5.13** Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Courada ad	Parameter		Conditions		Standard				
Symbol	Paramete	er Er	Conditions	Min.	Тур.	Max.	1		
tsucyc	SSCK clock cycle tim	е		4	-	=	tcyc(2)		
tHI	SSCK clock "H" width			0.4	_	0.6	tsucyc		
tLO	SSCK clock "L" width			0.4	-	0.6	tsucyc		
trise	SSCK clock rising	Master		=	-	1	tcyc(2)		
	time	Slave		-	-	1	μS		
tfall	SSCK clock falling time	Master		=	=	1	tcyc(2)		
		Slave		-	_	1	μS		
tsu	SSO, SSI data input setup time			100	-	=	ns		
tH	SSO, SSI data input hold time			1	=	=	tcyc(2)		
tLEAD	SCS setup time	Slave		1tcyc + 50	_	-	ns		
tLAG	SCS hold time	Slave		1tcyc + 50	_	_	ns		
top	SSO, SSI data output delay time			=	-	1	tcyc(2)		
tsa	SSI slave access time	e	2.7 V ≤ Vcc ≤ 5.5 V	-	-	1.5tcyc + 100	ns		
				-	-	1.5tcyc + 200	ns		
tor	SSI slave out open til	me	2.7 V ≤ Vcc ≤ 5.5 V	-	-	1.5tcyc + 100	ns		
			2.2 V ≤ Vcc < 2.7 V	_	_	1.5tcyc + 200	ns		

<sup>1.</sup> Vcc = 2.2 to 5.5 V, Vss = 0 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.

2. 1tcyc = 1/f1(s)

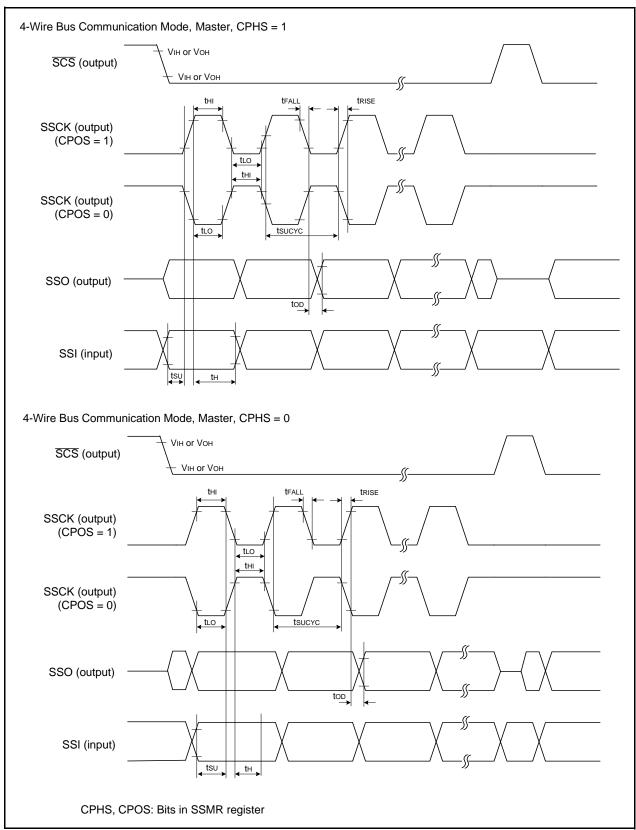


Figure 5.4 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

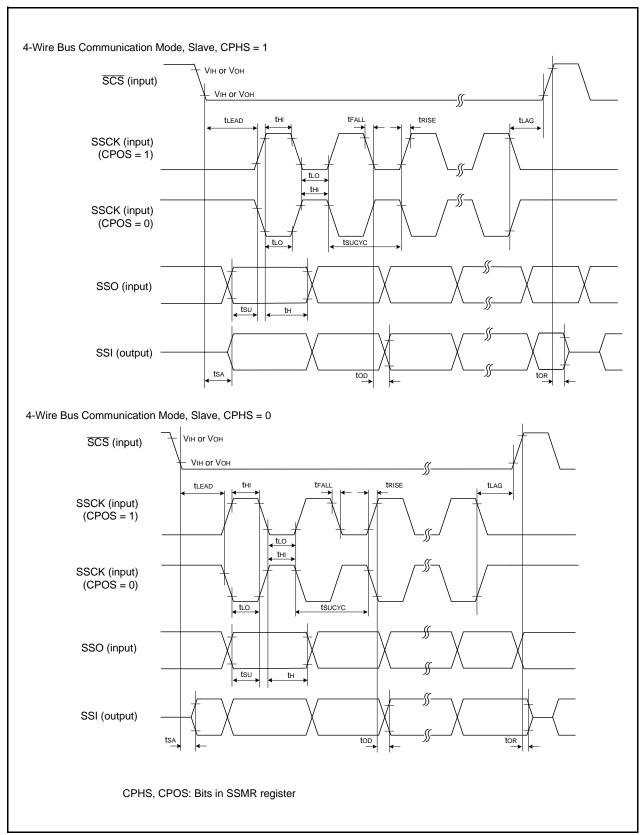


Figure 5.5 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

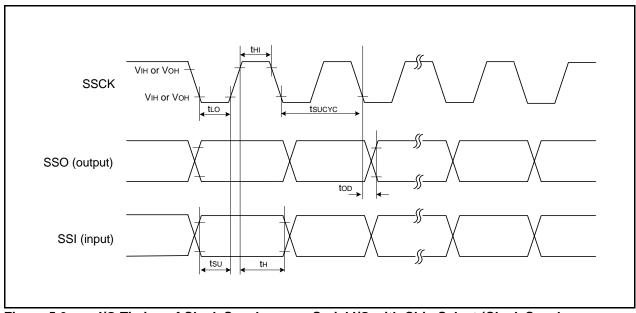


Figure 5.6 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 3.17 Illining Nequillements of 1-6 bus interface.	<b>Table 5.14</b>	Timing Requirements of I <sup>2</sup> C bus Interface <sup>(1)</sup>
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Symbol	Parameter	Condition	St	andard		Unit
Symbol	Farameter	Condition	Min.	Тур.	Max.	
tscl	SCL input cycle time		12tcyc + 600 <sup>(2)</sup>	-	-	ns
tsclh	SCL input "H" width		3tcyc + 300 <sup>(2)</sup>	-	-	ns
tscll	SCL input "L" width		5tcyc + 500 <sup>(2)</sup>	=	-	ns
tsf	SCL, SDA input fall time		=	-	300	ns
tsp	SCL, SDA input spike pulse rejection time		-	-	1tcyc(2)	ns
tBUF	SDA input bus-free time		5tcyc(2)	=	-	ns
tstah	Start condition input hold time		3tcyc(2)	-	-	ns
tstas	Retransmit start condition input setup time		3tcyc(2)	-	-	ns
tstop	Stop condition input setup time		3tcyc(2)	-	-	ns
tsdas	Data input setup time		1tcyc + 20 <sup>(2)</sup>	=	=	ns
tsdah	Data input hold time		0	-	-	ns

- 1. Vcc = 2.2 to 5.5 V, Vss = 0 V and Topr = -20 to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), unless otherwise specified.
- 2. 1 tcyc = 1/f1(s)

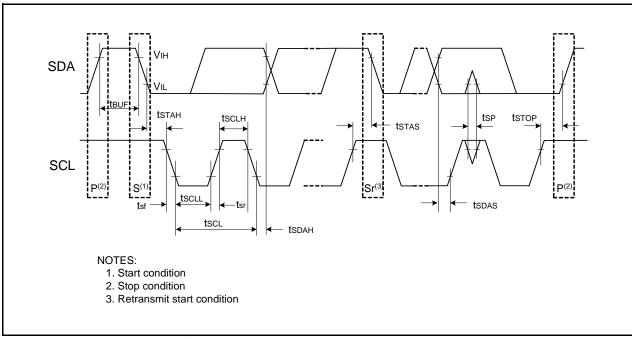


Figure 5.7 I/O Timing of I<sup>2</sup>C bus Interface

Table 5.15 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Do	rameter	Conditio	n	S	tandard		Unit
Symbol	Fai	ametei	Conditio	111	Min.	Тур.	Max.	Offic
Vон	Output "H" voltage	Except P1_0 to P1_7,	Iон = -5 mA		Vcc - 2.0	-	Vcc	V
		XOUT	Іон = -200 μА		Vcc - 0.5	-	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	Iон = -20 mA	Vcc - 2.0	-	Vcc	V
			Drive capacity LOW	Iон = -5 mA	Vcc - 2.0	_	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -1 mA	Vcc - 2.0	_	Vcc	V
			Drive capacity LOW	IOH = -500 μA	Vcc - 2.0	_	Vcc	V
Vol	Output "L" voltage	Except P1_0 to P1_7,	IoL = 5 mA			_	2.0	V
		XOUT	IoL = 200 μA			_	0.45	V
		P1_0 to P1_7	Drive capacity HIGH	IoL = 20 mA		_	2.0	V
			Drive capacity LOW	IoL = 5 mA		_	2.0	V
		XOUT	Drive capacity HIGH	IoL = 1 mA		_	2.0	V
			Drive capacity LOW	IoL = 500 μA		_	2.0	V
VT+-VT-	Hysteresis	NT0, INT1, INT3,   KI0, KI1, KI2, KI3,   TRAIO, RXD0, RXD1,   CLK0, SSI, SCL,   SDA, SSO			0.1	0.5	-	V
		RESET			0.1	1.0	-	V
Іін	Input "H" current		VI = 5 V, Vcc = 5V		-	-	5.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 5V		=	-	-5.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 5V		30	50	167	kΩ
RfXIN	Feedback resistance	XIN			-	1.0	=	ΜΩ
RfXCIN	Feedback resistance	XCIN			-	18	_	ΜΩ
VRAM	RAM hold voltage	•	During stop mode		1.8	-	-	V

<sup>1.</sup> Vcc = 4.2 to 5.5 V at  $T_{opr} = -20$  to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.16 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Parameter Condition	;	Unit			
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	10	17	mA
	other pins are Vss		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	9	15	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	6	_	mA
			XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	5	-	mA
			XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	4	-	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.5	-	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	10	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	4	_	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	I	5.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	2.5	_	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	1	130	300	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	=	30	_	μА

Table 5.17 Electrical Characteristics (3) [Vcc = 5 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter		Condition		Condition			d	Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit		
Icc	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	25	75	μА		
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	23	60	μА		
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	4.0	-	μА		
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	2.2	-	μА		
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	0.8	3.0	μА		
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.2	_	μА		

### **Timing Requirements**

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at Topr = 25°C) [Vcc = 5 V]

Table 5.18 XIN Input, XCIN Input

Symbol	Parameter		Standard		
Symbol	Faranietei	Min.	Max.	Unit	
tc(XIN)	XIN input cycle time	50	-	ns	
twh(xin)	XIN input "H" width	25	-	ns	
twl(xin)	XIN input "L" width	25	-	ns	
tc(XCIN)	XCIN input cycle time	14	=	μS	
twh(xcin)	XCIN input "H" width	7	=	μS	
twl(xcin)	XCIN input "L" width	7	=	μS	

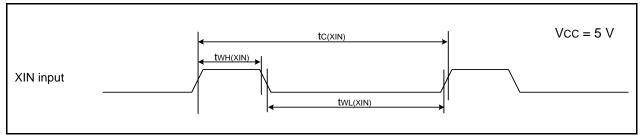


Figure 5.8 XIN Input and XCIN Input Timing Diagram when Vcc = 5 V

Table 5.19 TRAIO Input

Symbol	Symbol Parameter		dard	Unit
Symbol	Faidilletei	Min.	Max.	Offic
tc(TRAIO)	TRAIO input cycle time	100	=	ns
twh(traio)	TRAIO input "H" width	40	=	ns
twl(traio)	TRAIO input "L" width	40	=	ns

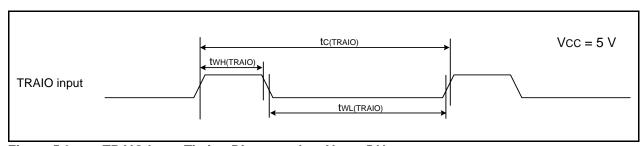


Figure 5.9 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.20 Serial Interface	.20 Seria	I Interface
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Symbol	Parameter	Stan	Unit	
Symbol	Farameter	Min.	Max.	Offic
tc(CK)	CLK0 input cycle time	200	-	ns
tw(ckh)	CLK0 input "H" width	100	-	ns
tW(CKL)	CLK0 input "L" width	100	=	ns
td(C-Q)	TXDi output delay time	-	50	ns
th(C-Q)	TXDi hold time	0	=	ns
tsu(D-C)	RXDi input setup time	50	=	ns
th(C-D)	RXDi input hold time	90	-	ns

i = 0 or 1

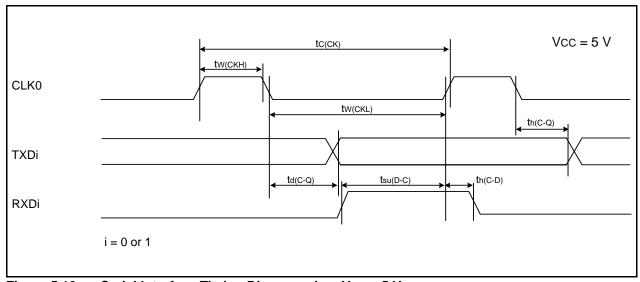


Figure 5.10 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.21 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter		Standard	
Symbol	Symbol	Min.	Max.	Unit
tw(INH)	ĪNTi input "H" width	250 <sup>(1)</sup>	-	ns
tW(INL)	INTi input "L" width	250 <sup>(2)</sup>	-	ns

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

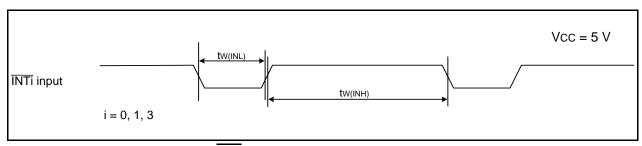


Figure 5.11 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Table 5.22 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Parameter Condition		Si		Unit			
Symbol	Pala	imeter	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except P1_0 to P1_7, XOUT	Iон = -1 mA		Vcc - 0.5	=	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	Iон = -5 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	Iон = -1 mA	Vcc - 0.5	-	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -0.1 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	ΙΟΗ = -50 μΑ	Vcc - 0.5	=	Vcc	V
Vol	Output "L" voltage	Except P1_0 to P1_7, XOUT	IOL = 1 mA		=	=	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	IoL = 5 mA	=	=	0.5	V
			Drive capacity LOW	IoL = 1 mA	=	=	0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1 mA	=	=	0.5	V
			Drive capacity LOW	Ιοι = 50 μΑ	=	-	0.5	V
VT+-VT-	Hysteresis	NT0, INT1, INT3,   KI0, KI1, KI2, KI3,   TRAIO, RXD0, RXD1,   CLK0, SSI, SCL,   SDA, SSO			0.1	0.3	=	V
		RESET			0.1	0.4	-	V
Іін	Input "H" current	I	VI = 3 V, Vcc = 3	3V	=	_	4.0	μА
lıL	Input "L" current		VI = 0 V, Vcc = 3	3V	_	_	-4.0	μА
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3	SV .	66	160	500	kΩ
RfXIN	Feedback resistance	XIN			1	3.0	-	МΩ
RfXCIN	Feedback resistance	XCIN		_	_	18	_	ΜΩ
VRAM	RAM hold voltage		During stop mod	е	1.8	-		V

<sup>1.</sup> Vcc = 2.7 to 3.3 V at Topr = -20 to 85°C (N version) / -40 to 85°C (D version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.23 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Parameter Condition		Standard			Unit
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division		6	=	mA
	other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	1	2	_	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division		5	9	mA
		mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2	_	mA
on-cl oscill mode Low- clock		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz FMR47 = 1	П	130	300	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	-	30	-	μА
	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	25	70	μА	
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	1	23	55	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	3.8	-	μА
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	2.0	-	μА	
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	0.7	3.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	1.1	_	μА

### **Timing requirements**

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C) [Vcc = 3 V]

Table 5.24 XIN Input, XCIN Input

Symbol	Parameter		Standard		
Symbol	raianielei	Min.	Max.	Unit	
tc(XIN)	XIN input cycle time	100	=	ns	
twh(xin)	XIN input "H" width	40	=	ns	
twl(XIN)	XIN input "L" width	40	=	ns	
tc(XCIN)	XCIN input cycle time	14	=	μS	
twh(xcin)	XCIN input "H" width	7		μS	
twl(xcin)	XCIN input "L" width	7	=	μS	

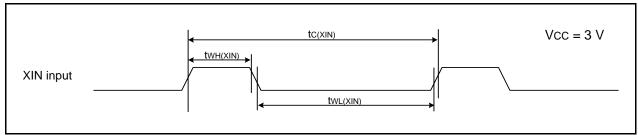


Figure 5.12 XIN Input and XCIN Input Timing Diagram when Vcc = 3 V

Table 5.25 TRAIO Input

Symbol	Parameter		Standard		
Symbol	Falanielei	Min.	Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	300	=	ns	
twh(traio)	TRAIO input "H" width	120	=	ns	
twl(traio)	TRAIO input "L" width	120	=	ns	

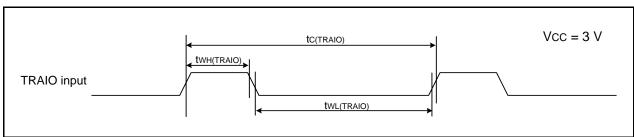


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.26 Serial Interface

Symbol	Parameter	Standard		Unit	
Syllibol	raidilletei	Min.	Max.	Offic	
tc(CK)	CLK0 input cycle time	300	=	ns	
tW(CKH)	CLK0 input "H" width	150	=	ns	
tW(CKL)	CLK0 Input "L" width	150	=	ns	
td(C-Q)	TXDi output delay time	=	80	ns	
th(C-Q)	TXDi hold time	0	=	ns	
tsu(D-C)	RXDi input setup time	70	=	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 or 1

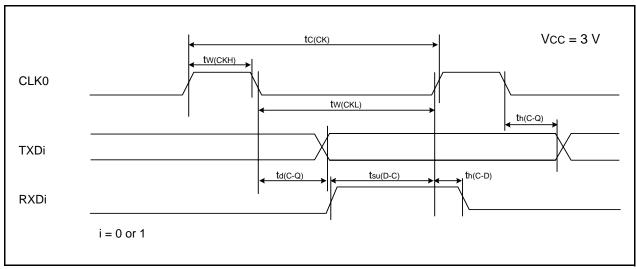


Figure 5.14 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.27 External Interrupt  $\overline{INTi}$  (i = 0, 1, 3) Input

Symbol	Parameter		Standard		
	Falanielei	Min.	Max.	Unit	
tW(INH)	INTi input "H" width	380(1)	-	ns	
tW(INL)	INTi input "L" width	380(2)	-	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

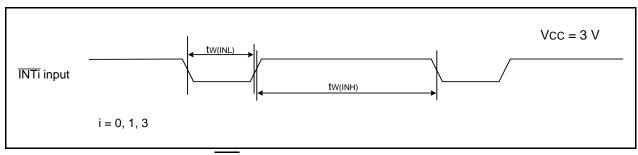


Figure 5.15 External Interrupt INTi Input Timing Diagram when Vcc = 3 V

Table 5.28 Electrical Characteristics (5) [Vcc = 2.2 V]

Compleal	Dave	Parameter		Condition		tandard		Unit
Symbol	Para	ameter	Condition		Min.	Тур.	Max.	Unit
Vон	Output "H" voltage	Except P1_0 to P1_7, XOUT	Iон = -1 mA		Vcc - 0.5	-	Vcc	V
		P1_0 to P1_7	Drive capacity HIGH	Iон = -2 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	Iон = -1 mA	Vcc - 0.5	=	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -0.1 mA	Vcc - 0.5	-	Vcc	V
			Drive capacity LOW	IOH = -50 μA	Vcc - 0.5	-	Vcc	V
Vol	Output "L" voltage	Except P1_0 to P1_7, XOUT	IOL = 1 mA		=	=	0.5	V
		P1_0 to P1_7	Drive capacity HIGH	IoL = 2 mA	=	=	0.5	V
			Drive capacity LOW	IoL = 1 mA	=	=	0.5	V
		XOUT	Drive capacity HIGH	IOL = 0.1 mA	=	=	0.5	V
			Drive capacity LOW	IoL = 50 μA	=	-	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, RXDO, RXD1, CLKO, SSI, SCL, SDA, SSO			0.05	0.3	-	V
		RESET			0.05	0.15	-	V
lін	Input "H" current	1	VI = 2.2 V		_	_	4.0	μА
lıL	Input "L" current		VI = 0 V		-	_	-4.0	μA
RPULLUP	Pull-up resistance		VI = 0 V		100	200	600	kΩ
RfXIN	Feedback resistance	XIN			-	5	-	МΩ
RfXCIN	Feedback resistance	XCIN			-	35	-	МΩ
VRAM	RAM hold voltage		During stop mod	е	1.8	_	_	V

<sup>1.</sup> Vcc = 2.2 V at Topr = -20 to  $85^{\circ}C$  (N version) / -40 to  $85^{\circ}C$  (D version), f(XIN) = 5 MHz, unless otherwise specified.

Table 5.29 Electrical Characteristics (6) [Vcc = 2.2 V] (Topr = -20 to 85°C (N version) / -40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Parameter Condition			Standar	b	Unit
Gyllibol	i alametei		Condition	Min.	Тур.	Max.	Offic
Icc	Power supply current (Vcc = 2.2 to 2.7 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	3.5	_	mA
other pins are Vss		XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	1.5	=	mA	
	High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	3.5	-	mA	
		mode	XIN clock off High-speed on-chip oscillator on fOCO = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	1.5		mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	_	100	230	μА
		Low-speed clock mode XIN clock off High-speed on-ch Low-speed on-ch XCIN clock oscilla FMR47 = 1	High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz	_	100	230	μА
	Wai		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz Program operation on RAM Flash memory off, FMSTP = 1	_	25		μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	22	60	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	20	55	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (high drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	3.0	-	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (low drive) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	1.8	-	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	0.7	3.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	1.1	_	μА

### **Timing requirements**

(Unless Otherwise Specified: Vcc = 2.2 V, Vss = 0 V at Topr = 25°C) [Vcc = 2.2 V]

Table 5.30 XIN Input, XCIN Input

Symbol	Symbol Parameter		Standard		
Symbol			Max.	Unit	
tc(XIN)	XIN input cycle time	200	-	ns	
twh(xin)	XIN input "H" width		=	ns	
twl(XIN)	XIN input "L" width	90	-	ns	
tc(XCIN)	XCIN input cycle time	14	-	μS	
twh(xcin)	XCIN input "H" width	7	=	μS	
twl(xcin)	XCIN input "L" width	7	-	μS	

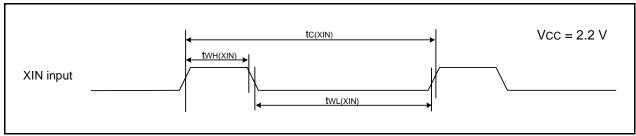


Figure 5.16 XIN Input and XCIN Input Timing Diagram when Vcc = 2.2 V

Table 5.31 TRAIO Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	500	-	ns	
twh(traio)	TRAIO input "H" width	200	-	ns	
twl(traio)	TRAIO input "L" width	200	-	ns	

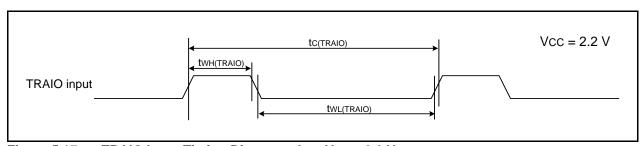


Figure 5.17 TRAIO Input Timing Diagram when Vcc = 2.2 V

Table 5.32 Serial Interface	Table	5.32	Serial	Interface
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Symbol	Parameter		Standard		
Symbol	Faranietei	Min.	Max.	Unit	
tc(CK)	CLK0 input cycle time	800	-	ns	
tw(ckh)	CLK0 input "H" width	400	-	ns	
tW(CKL)	CLK0 input "L" width	400	-	ns	
td(C-Q)	TXDi output delay time	=	200	ns	
th(C-Q)	TXDi hold time	0	-	ns	
tsu(D-C)	RXDi input setup time	150	=	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 or 1

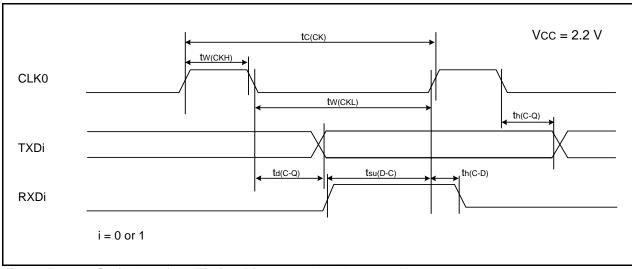


Figure 5.18 Serial Interface Timing Diagram when Vcc = 2.2 V

Table 5.33 External Interrupt  $\overline{\text{INTi}}$  (i = 0, 1, 3) Input

Symbol	Parameter		Standard		
Symbol	i didilicici	Min.	Max.	Unit	
tw(INH)	INTi input "H" width	1000(1)	-	ns	
tw(INL)	INTi input "L" width	1000 <sup>(2)</sup>	=	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.

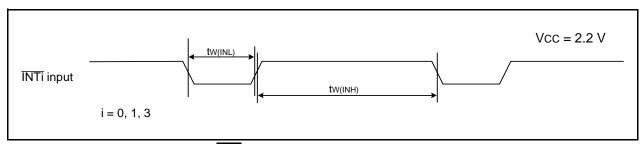


Figure 5.19 External Interrupt INTi Input Timing Diagram when VCC = 2.2 V

## 5.2 J, K Version

Table 5.34 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc	Supply voltage		-0.3 to 6.5	V
Vı	Input voltage		-0.3 to Vcc + 0.3	V
Vo	Output voltage		-0.3 to Vcc + 0.3	V
Pd	Power dissipation	-40 °C ≤ Topr ≤ 85 °C	300	mW
		85 °C ≤ Topr ≤ 125 °C	125	mW
Topr	Operating ambient temperature		-40 to 85 (J version) / -40 to 125 (K version)	°C
Tstg	Storage temperature		-65 to 150	°C

 Table 5.35
 Recommended Operating Conditions

Company of	Dow		Conditions		Standard			
Symbol	Para	ameter	Conditions	Min.	Тур.	Max.	Unit	
Vcc/AVcc	Supply voltage			2.7	_	5.5	V	
Vss/AVss	Supply voltage			_	0	-	V	
ViH	Input "H" voltage			0.8 Vcc	-	Vcc	V	
VIL	Input "L" voltage			0	-	0.2 Vcc	V	
IOH(sum)	Peak sum output "H" current	Sum of all pins IOH(peak)		-	=	-60	mA	
IOH(peak)	Peak output "H" current			-	=	-10	mA	
IOH(avg)	Average output "H" current			-	=	-5	mA	
IOL(sum)	Peak sum output "L" currents	Sum of all pins IOL(peak)		-	=	60	mA	
IOL(peak)	Peak output "L" currents			-	-	10	mA	
IOL(avg)	Average output "L" current			-	=	5	mA	
f(XIN)	XIN clock input oscillation frequency		3.0 V ≤ Vcc ≤ 5.5 V (other than K version)	0	=	20	MHz	
			3.0 V ≤ Vcc ≤ 5.5 V (K version)	0	-	16	MHz	
			2.7 V ≤ Vcc < 3.0 V	0	_	10	MHz	
=	System clock	OCD2 = 0 XIN clock selected	$3.0 \text{ V} \le \text{Vcc} \le 5.5 \text{ V}$ (other than K version)	0	=	20	MHz	
			3.0 V ≤ Vcc ≤ 5.5 V (K version)	0	_	16	MHz	
			2.7 V ≤ Vcc < 3.0 V	0	_	10	MHz	
		OCD2 = 1 On-chip oscillator clock selected	FRA01 = 0 Low-speed on-chip oscillator clock selected	-	125	-	kHz	
			FRA01 = 1 High-speed on-chip oscillator clock selected (other than K version)	-	-	20	MHz	
			FRA01 = 1 High-speed on-chip oscillator clock selected	-	_	10	MHz	

- 1. Vcc = 2.7 to 5.5 V at Topr = -40 to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), unless otherwise specified.
- 2. The average output current indicates the average value of current measured during 100 ms.

Table 5.36	A/D Converter	Characteristics
------------	---------------	-----------------

Symbol		Parameter	Conditions	Standard			Unit
Symbol	'	diameter		Min.	Тур.	Max.	Offic
_	Resolution		Vref = AVCC	-	-	10	Bits
_	Absolute	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	-	-	±3	LSB
	accuracy	8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	-	-	±2	LSB
		10-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	-	-	±5	LSB
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 3.3 V	-	-	±2	LSB
Rladder	Resistor ladder		Vref = AVCC	10	-	40	kΩ
tconv	Conversion time	10-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	3.3	-	=	μS
		8-bit mode	φAD = 10 MHz, Vref = AVCC = 5.0 V	2.8	-	=	μS
Vref	Reference voltag	e		2.7	-	AVcc	V
VIA	Analog input volta	age <sup>(2)</sup>		0	-	AVcc	V
_	A/D operating	Without sample and hold		0.25	-	10	MHz
	clock frequency	With sample and hold		1	=	10	MHz

- 1. AVcc = 2.7 to 5.5 V at  $T_{opr} = -40$  to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), unless otherwise specified.
- 2. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

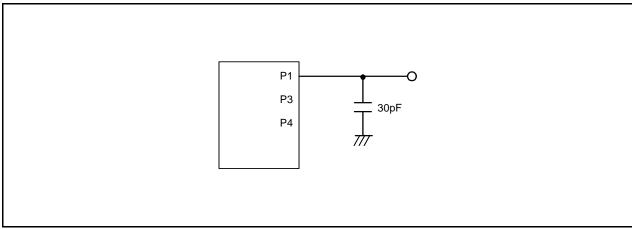


Figure 5.20 Ports P1, P3, and P4 Timing Measurement Circuit

Table 5.37 Flash Memory (Program ROM) Electrical Characteristics

Cumbal	Doromotor	Conditions		Stand	ard	Unit
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Unit
=	Program/erase endurance <sup>(2)</sup>	R8C/28 Group	100 <sup>(3)</sup>	=	=	times
		R8C/29 Group	1,000(3)	-	-	times
-	Byte program time		ı	50	400	μS
=	Block erase time		=	0.4	9	S
td(SR-SUS)	Time delay from suspend request until suspend		_	_	97 + CPU clock × 6 cycles	μS
_	Interval from erase start/restart until following suspend request		650	_	_	μS
=	Interval from program start/restart until following suspend request		0	=	_	ns
=	Time from suspend until program/erase restart		=	-	3 + CPU clock × 4 cycles	μS
-	Program, erase voltage		2.7	-	5.5	V
-	Read voltage		2.7	-	5.5	V
=	Program, erase temperature		0	=	60	°C
_	Data hold time <sup>(7)</sup>	Ambient temperature = 55°C	20	_	-	year

- 1. Vcc = 2.7 to 5.5 V at Topr = 0 to 60°C, unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.

If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.

However, the same address must not be programmed more than once per erase operation (overwriting prohibited).

- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 5. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 6. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 7. The data hold time includes time that the power supply is off or the clock is not supplied.

Table 5.38 Flash Memory (Data flash Block A, Block B) Electrical Characteristics(4)

Symbol	Parameter	Conditions		Stand	dard	Unit
Symbol	Falanielei	Conditions	Min.	Тур.	Max.	Offic
-	Program/erase endurance <sup>(2)</sup>		10,000(3)	_	-	times
_	Byte program time (program/erase endurance ≤ 1,000 times)		-	50	400	μS
_	Byte program time (program/erase endurance > 1,000 times)		_	65	_	μ\$
_	Block erase time (program/erase endurance ≤ 1,000 times)		_	0.2	9	S
_	Block erase time (program/erase endurance > 1,000 times)		-	0.3	_	S
td(SR-SUS)	Time delay from suspend request until suspend		_	=	97 + CPU clock × 6 cycles	μ\$
_	Interval from erase start/restart until following suspend request		650	=	_	μS
_	Interval from program start/restart until following suspend request		0	-	_	ns
_	Time from suspend until program/erase restart		_	-	3 + CPU clock × 4 cycles	μS
=	Program, erase voltage		2.7	_	5.5	V
=	Read voltage		2.7	_	5.5	V
=	Program, erase temperature		-40	-	85 <sup>(8)</sup>	°C
=	Data hold time <sup>(9)</sup>	Ambient temperature = 55°C	20	-	=	year

- 1. Vcc = 2.7 to 5.5 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. Definition of programming/erasure endurance
  - The programming and erasure endurance is defined on a per-block basis.
  - If the programming and erasure endurance is n (n = 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
  - However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
- 3. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
- 4. Standard of block A and block B when program and erase endurance exceeds 1,000 times. Byte program time to 1,000 times is the same as that in program ROM.
- 5. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A and B can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
- 6. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
- 7. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
- 8. 125°C for K version.
- 9. The data hold time includes time that the power supply is off or the clock is not supplied.

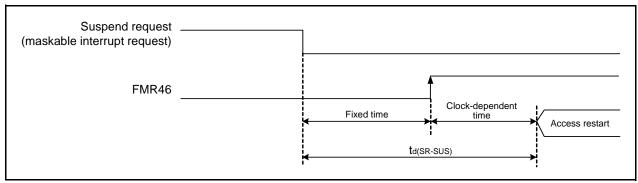


Figure 5.21 Time delay until Suspend

Table 5.39 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Farameter	Condition	Min.	Тур.	Max.	Offic
Vdet1	Voltage detection level <sup>(2, 4)</sup>		2.70	2.85	3.0	V
td(Vdet1-A)	Voltage monitor 1 reset generation time <sup>(5)</sup>		_	40	200	μS
_	Voltage detection circuit self power consumption	VCA26 = 1, Vcc = 5.0 V	-	0.6	_	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(3)</sup>		=	=	100	μS
Vccmin	MCU operating voltage minimum value		2.70	-	-	V

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and  $T_{opr} = -40$  to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version).
- 2. Hold Vdet2 > Vdet1.
- 3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.
- 4. This parameter shows the voltage detection level when the power supply drops. The voltage detection level when the power supply rises is higher than the voltage detection level when the power supply drops by approximately 0.1 V.
- 5. Time until the voltage monitor 1 reset is generated after the voltage passes V<sub>det1</sub> when V<sub>CC</sub> falls. When using the digital filter, its sampling time is added to t<sub>d</sub>(V<sub>det1-A</sub>). When using the voltage monitor 1 reset, maintain this time until V<sub>CC</sub> = 2.0 V after the voltage passes V<sub>det1</sub> when the power supply falls.

Table 5.40 Voltage Detection 2 Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Faranteter	Condition	Min.	Тур.	Max.	Offic
Vdet2	Voltage detection level <sup>(2)</sup>		3.3	3.6	3.9	V
td(Vdet2-A)	Voltage monitor 2 reset/interrupt request generation time <sup>(3., 5)</sup>		=	40	200	μS
=	Voltage detection circuit self power consumption	VCA27 = 1, Vcc = 5.0 V	=	0.6	=	μΑ
td(E-A)	Waiting time until voltage detection circuit operation starts <sup>(4)</sup>		=	=	100	μS

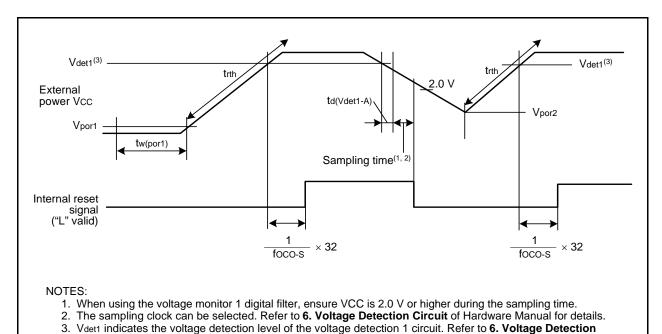
- 1. The measurement condition is Vcc = 2.7 to 5.5 V and Topr = -40 to 85°C (J version) / -40 to 125°C (K version).
- 2. Hold Vdet2 > Vdet1
- 3. Time until the voltage monitor 2 reset/interrupt request is generated after the voltage passes Vdet2.
- 4. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.
- 5. When using the digital filter, its sampling time is added to td(Vdet2-A). When using the voltage monitor 2 reset, maintain this time until Vcc = 2.0 V after the voltage passes Vdet2 when the power supply falls.



	<b>Table 5.41</b>	Power-on Reset Circuit.	Voltage Monitor 1 Reset Electrical Characteristics <sup>(3)</sup>
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Symbol	Parameter	Condition		Unit			
Symbol	Faranietei	Condition	Min.	Тур.	Max.	Offic	
Vpor1	Power-on reset valid voltage <sup>(4)</sup>		_	_	0.1	V	
Vpor2	Power-on reset or voltage monitor 1 reset valid voltage		0	_	Vdet1	V	
trth	External power Vcc rise gradient	Vcc ≤ 3.6 V	20(2)	-	-	mV/msec	
		Vcc > 3.6 V	20(2)	-	2,000	mV/msec	

- 1. The measurement condition is Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. This condition (the minimum value of external power Vcc rise gradient) does not apply if V<sub>por2</sub> ≥ 1.0 V.
- 3. To use the power-on reset function, enable voltage monitor 1 reset by setting the LVD1ON bit in the OFS register to 0, the VW1C0 and VW1C6 bits in the VW1C register to 1 respectively, and the VCA26 bit in the VCA2 register to 1.
- 4. tw(por1) indicates the duration the external power Vcc must be held below the effective voltage (Vpor1) to enable a power on reset. When turning on the power for the first time, maintain tw(por1) for 30 s or more if -20°C ≤ Topr ≤ 125°C, maintain tw(por1) for 3,000 s or more if -40°C ≤ Topr < -20°C.</p>



Circuit of Hardware Manual for details.

Figure 5.22 Reset Circuit Electrical Characteristics

Table 5.42 High-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition			Unit	
Symbol	Faranielei	Condition	Min.	Тур.	Max.	Offic
fOCO40M	High-speed on-chip oscillator frequency temperature • supply voltage dependence	Vcc = 4.75 to 5.25 V $0^{\circ}$ C $\leq$ Topr $\leq$ $60^{\circ}$ C <sup>(2)</sup>	39.2	40	40.8	MHz
		Vcc = 3.0 to 5.5 V -20°C $\leq$ Topr $\leq$ 85°C <sup>(2)</sup>	38.8	40	41.2	MHz
		Vcc = 3.0 to 5.5 V -40°C $\leq$ Topr $\leq$ 85°C <sup>(2)</sup>	38.4	40	41.6	MHz
		Vcc = 3.0 to 5.5 V -40°C $\leq$ Topr $\leq$ 125°C <sup>(2)</sup>	38	40	42	MHz
		Vcc = 2.7 to 5.5 V -40°C $\leq$ Topr $\leq$ 125°C <sup>(2)</sup>	37.6	40	42.4	MHz
_	Value in FRA1 register after reset		08h	_	F7h	_
_	Oscillation frequency adjustment unit of high- speed on-chip oscillator	Adjust FRA1 register (value after reset) to -1	-	+0.3	_	MHz
=	Oscillation stability time		=	10	100	μS
=	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	=	400	=	μΑ

- 1. Vcc = 2.7 to 5.5 V,  $T_{opr}$  = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. These standard values show when the FRA1 register value after reset is assumed.

Table 5.43 Low-speed On-Chip Oscillator Circuit Electrical Characteristics

Symbol	Parameter	Condition		Unit		
Symbol	Falanetei	Min. Typ. Max.	Offic			
fOCO-S	Low-speed on-chip oscillator frequency		40	125	250	kHz
=	Oscillation stability time		=	10	100	μS
_	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	-	15	-	μΑ

#### NOTE:

### Table 5.44 Power Supply Circuit Timing Characteristics

Symbol	Parameter	Condition	Standard			Unit
Symbol		Condition	Min.	Тур.	Max.	Offic
td(P-R)	Time for internal power supply stabilization during power-on <sup>(2)</sup>		1	=	2000	μS
td(R-S)	STOP exit time <sup>(3)</sup>		-	-	150	μS

- 1. The measurement condition is Vcc = 2.7 to 5.5 V and  $T_{opr}$  = 25°C.
- 2. Waiting time until the internal power supply generation circuit stabilizes during power-on.
- 3. Time until system clock supply starts after the interrupt is acknowledged to exit stop mode.

<sup>1.</sup> Vcc = 2.7 to 5.5 V, Topr = -40 to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), unless otherwise specified.

**Table 5.45** Timing Requirements of Clock Synchronous Serial I/O with Chip Select(1)

Cumbal	Parameter		Conditions		Stand	lard	Unit
Symbol	Paramete	Falailletei		Min.	Тур.	Max.	1
tsucyc	SSCK clock cycle tim	е		4	_	=	tcyc(2)
tHI	SSCK clock "H" width			0.4	_	0.6	tsucyc
tLO	SSCK clock "L" width			0.4	-	0.6	tsucyc
trise	SSCK clock rising	Master		=	=	1	tcyc(2)
	time	Slave		=	_	1	μS
tfall	SSCK clock falling time	Master		=	=	1	tcyc(2)
		Slave		=	_	1	μS
tsu	SSO, SSI data input s	setup time		100	-	=	ns
tH	SSO, SSI data input h	nold time		1	=	=	tcyc(2)
tLEAD	SCS setup time	Slave		1tcyc + 50	-	-	ns
tLAG	SCS hold time	Slave		1tcyc + 50	_	-	ns
top	SSO, SSI data output	delay time		-	_	1	tcyc(2)
tsa	SSI slave access time	)		=	_	1.5tcyc + 100	ns
tor	SSI slave out open tir	ne		=	_	1.5tcyc + 100	ns

- 1. Vcc = 2.7 to 5.5 V, Vss = 0 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.

  2. 1tcyc = 1/f1(s)

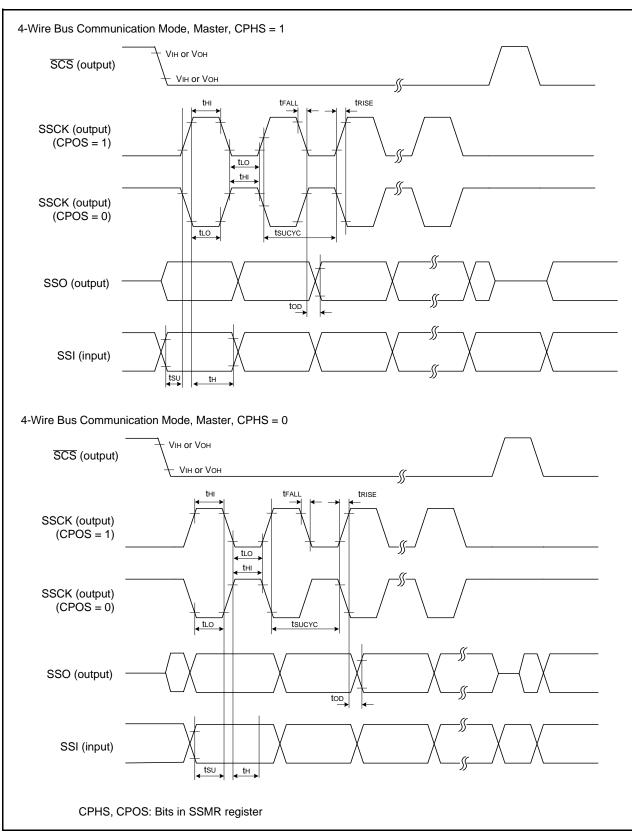


Figure 5.23 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Master)

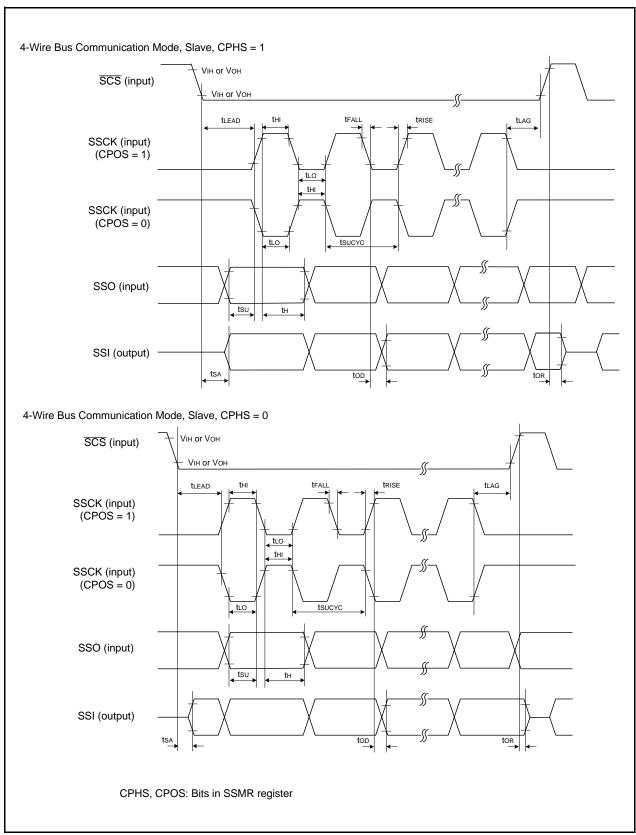


Figure 5.24 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Slave)

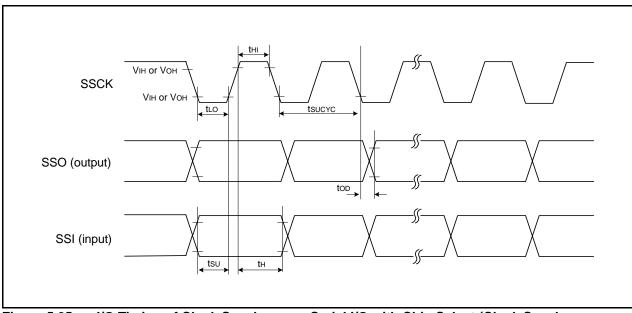


Figure 5.25 I/O Timing of Clock Synchronous Serial I/O with Chip Select (Clock Synchronous Communication Mode)

Table 5.46 Timing Requirements of I<sup>2</sup>C bus Interface<sup>(1)</sup>

Symbol	Parameter	Condition	St	Standard			
Symbol	Farameter	Condition	Min.	Тур.	Max.		
tscl	SCL input cycle time		12tcyc + 600 <sup>(2)</sup>	-	-	ns	
tsclh	SCL input "H" width		3tcyc + 300 <sup>(2)</sup>	=	=	ns	
tscll	SCL input "L" width		5tcyc + 500 <sup>(2)</sup>	-	-	ns	
tsf	SCL, SDA input fall time		=	=	300	ns	
tsp	SCL, SDA input spike pulse rejection time		-	-	1tcyc(2)	ns	
tBUF	SDA input bus-free time		5tcyc(2)	-	-	ns	
tstah	Start condition input hold time		3tcyc(2)	=	=	ns	
tstas	Retransmit start condition input setup time		3tcyc(2)	=	=	ns	
tstop	Stop condition input setup time		3tcyc(2)	=	=	ns	
tsdas	Data input setup time		1tcyc + 20 <sup>(2)</sup>	-	-	ns	
tsdah	Data input hold time		0	-	-	ns	

- 1. Vcc = 2.7 to 5.5 V, Vss = 0 V at Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.
- 2. 1tcyc = 1/f1(s)

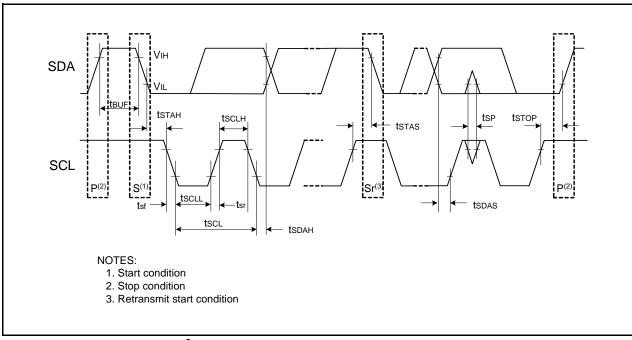


Figure 5.26 I/O Timing of I<sup>2</sup>C bus Interface

Table 5.47 Electrical Characteristics (1) [Vcc = 5 V]

Symbol	Parameter		Conditio	n	Standard			Unit	
Syllibol	Fai	rameter	Conditio	111	Min.	Тур.	Max.	Offic	
Vон	Output "H" voltage	Except XOUT	Iон = -5 mA		Vcc - 2.0	-	Vcc	V	
			Ioн = -200 μA		Vcc - 0.3	-	Vcc	V	
		XOUT	Drive capacity HIGH	Iон = -1 mA	Vcc - 2.0	=	Vcc	V	
			Drive capacity LOW	IOH = -500 μA	Vcc - 2.0	=	Vcc	V	
Vol	Output "L" voltage Except XOUT IoL = 5 mA		=	-	2.0	V			
			IoL = 200 μA		=	-	0.45	V	
		XOUT	Drive capacity HIGH	IoL = 1 mA	=	-	2.0	V	
			Drive capacity LOW	IoL = 500 μA	=	-	2.0	V	
VT+-VT-	Hysteresis	INTO, INT1, INT3,   KIO, KI1, KI2, KI3,   TRAIO, RXDO, RXD1,   CLKO, SSI, SCL,   SDA, SSO			0.1	0.5	-	>	
		RESET			0.1	1.0	_	V	
Іін	Input "H" current		VI = 5 V, Vcc = 5V		_	_	5.0	μА	
lı∟	Input "L" current		VI = 0 V, Vcc = 5V		-	_	-5.0	μА	
RPULLUP	Pull-up resistance	-up resistance VI = 0 V, Vcc = 5V		30	50	167	kΩ		
RfXIN	Feedback resistance	XIN			=	1.0	_	ΜΩ	
VRAM	RAM hold voltage		During stop mode		2.0	-	-	V	

<sup>1.</sup> Vcc = 4.2 to 5.5 V at Topr = -40 to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.48 Electrical Characteristics (2) [Vcc = 5 V] (Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Parameter		Condition		Standar	1	Unit
			Min.	Тур.		
Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode,	High-speed clock mode	XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	-	10	17	mA
other pins are Vss	r pins are Vss High-speed on-chip oscillator off	High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	9	15	mA
		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	ı	6	_	mA
		XIN = 20 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ĺ	5	_	mA
		XIN = 16 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	4	_	mA
		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ĺ	2.5	_	mA
	High-speed on-chip oscillator	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz No division	1	10	15	mA
	mode	XIN clock off High-speed on-chip oscillator on fOCO = 20 MHz (J version) Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	4	-	mA
		XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	-	5.5	10	mA
		XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	-	2.5	-	mA
	Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	-	130	300	μА
	Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	25	75	μА
		XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	_	23	60	μА
	Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0		0.8	3.0	μА
		XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.2	_	μА
		XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1	=	4.0	_	μА
	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open,	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss  High-speed clock mode  High-speed on-chip oscillator mode  Low-speed on-chip oscillator mode  Wait mode	Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are open, other pins are Vss	Parameter  Power supply current (Vcc = 3.3 to 5.5 V) Single-chip mode, output pins are open, other pins are Vss  Interest of the pins are open, other pins are Vss  Interest of the pins are vss of the pins are Vss  Interest of the pins are vss of	Parameter	Parameter   Power supply current   (Vicc = 3.1 to 5.5 V)   Clock mode   Ningle-chip mode, output pins are open, other pins are Vss   Vice = 3.1 to 5.5 V   Clock mode   Ningle-chip mode, output pins are open, other pins are Vss   Vice = 3.1 to 1.5 to 1.

### **Timing Requirements**

(Unless Otherwise Specified: Vcc = 5 V, Vss = 0 V at  $Topr = 25^{\circ}C$ ) [Vcc = 5 V]

### Table 5.49 XIN Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(XIN)	XIN input cycle time	50	=	ns	
twh(xin)	XIN input "H" width	25	=	ns	
twl(XIN)	XIN input "L" width	25	_	ns	

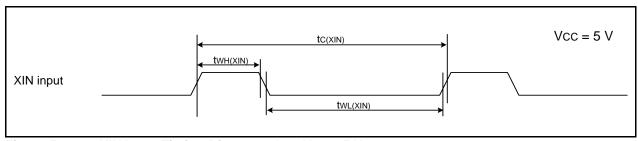


Figure 5.27 XIN Input Timing Diagram when Vcc = 5 V

### Table 5.50 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	100	=	ns	
twh(traio)	TRAIO input "H" width	40	=	ns	
twl(traio)	TRAIO input "L" width	40	=	ns	

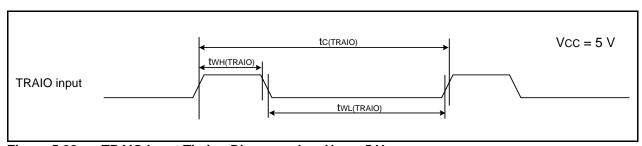


Figure 5.28 TRAIO Input Timing Diagram when Vcc = 5 V

Table 5.51 Serial Interface

Symbol	Parameter		Standard		
Symbol	raidilletei	Min.	Max.	Unit	
tc(CK)	CLK0 input cycle time	CLK0 input cycle time 200			
tW(CKH)	CLK0 input "H" width	100	-	ns	
tW(CKL)	CLK0 input "L" width	100	=	ns	
td(C-Q)	TXDi output delay time	-	50	ns	
th(C-Q)	TXDi hold time		=	ns	
tsu(D-C)	RXDi input setup time		=	ns	
th(C-D)	RXDi input hold time	90	-	ns	

i = 0 or 1

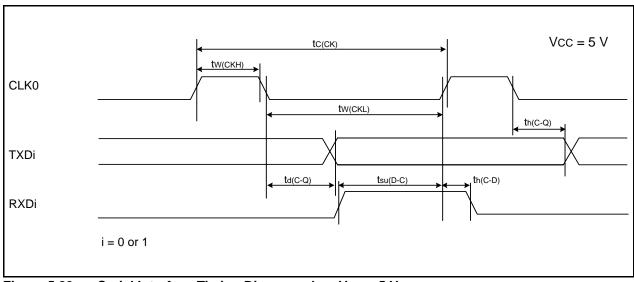


Figure 5.29 Serial Interface Timing Diagram when Vcc = 5 V

Table 5.52 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tW(INH)	INTi input "H" width	250 <sup>(1)</sup>	-	ns	
tW(INL)	INTi input "L" width	250(2)	ı	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

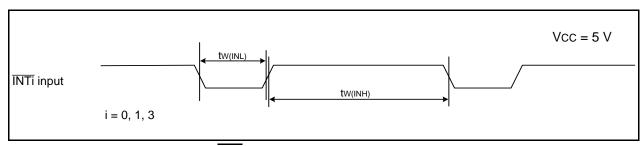


Figure 5.30 External Interrupt INTi Input Timing Diagram when Vcc = 5 V

Table 5.53 Electrical Characteristics (3) [Vcc = 3 V]

Symbol	Por	Parameter Condition		ition	S	tandard		Unit
Symbol	Faic			Min.	Тур.	Max.	Offic	
Vон	Output "H" voltage	Except XOUT	Iон = -1 mA		Vcc - 0.5	=	Vcc	V
		XOUT	Drive capacity HIGH	Iон = -0.1 mA	Vcc - 0.5	_	Vcc	V
			Drive capacity LOW	Іон = -50 μΑ	Vcc - 0.5	_	Vcc	V
Vol	Output "L" voltage	Except XOUT	IoL = 1 mA		-	1	0.5	V
		XOUT	Drive capacity HIGH	IoL = 0.1 mA	=	=	0.5	V
			Drive capacity LOW	IOL = 50 μA	=	_	0.5	V
VT+-VT-	Hysteresis	INTO, INT1, INT3, KIO, KI1, KI2, KI3, TRAIO, RXDO, RXD1, CLKO, SSI, SCL, SDA, SSO			0.1	0.3	-	V
		RESET			0.1	0.4	_	V
lін	Input "H" current		VI = 3 V, Vcc = 3	V	=	=	4.0	μΑ
lıL	Input "L" current		VI = 0 V, Vcc = 3	V	_	-	-4.0	μΑ
RPULLUP	Pull-up resistance		VI = 0 V, Vcc = 3	V	66	160	500	kΩ
RfXIN	Feedback resistance	XIN			-	3.0	_	МΩ
VRAM	RAM hold voltage	•	During stop mode	Э	2.0	1	_	V

<sup>1.</sup> Vcc = 2.7 to 3.3 V at Topr = -40 to  $85^{\circ}C$  (J version) / -40 to  $125^{\circ}C$  (K version), f(XIN) = 10 MHz, unless otherwise specified.

Table 5.54 Electrical Characteristics (4) [Vcc = 3 V] (Topr = -40 to 85°C (J version) / -40 to 125°C (K version), unless otherwise specified.)

Cumbal	Doromotor	Condition		Unit			
Symbol	Parameter		Condition	Min.	Тур.	Max.	Unit
Icc	Power supply current (Vcc = 2.7 to 3.3 V) Single-chip mode, output pins are open,	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	_	6	_	mA
	other pins are Vss		XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	ı	2	_	m <i>P</i>
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	I	5	9	mA
			XIN clock off High-speed on-chip oscillator on fOCO = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	_	2	-	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR47 = 1	I	130	300	μА
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	25	70	μА
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	-	23	55	μА
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	0.7	3.0	μА
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	-	1.1	_	μА
			XIN clock off, Topr = 125°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	_	3.8	_	μА

### **Timing requirements**

(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at  $Topr = 25^{\circ}C$ ) [Vcc = 3 V]

Table 5.55 XIN Input

Cumbal	Parameter		Standard		
Symbol			Max.	Unit	
tc(XIN)	XIN input cycle time	100	=	ns	
twh(xin)	XIN input "H" width	40	=	ns	
twl(xin)	XIN input "L" width	40	=	ns	

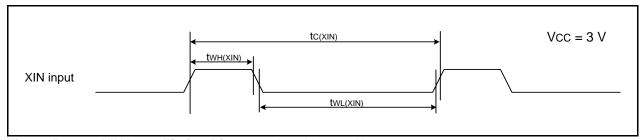


Figure 5.31 XIN Input Timing Diagram when Vcc = 3 V

Table 5.56 TRAIO Input

Symbol	Parameter		Standard		
			Max.	Unit	
tc(TRAIO)	TRAIO input cycle time	300	=	ns	
tWH(TRAIO)	TRAIO input "H" width	120	=	ns	
twl(traio)	TRAIO input "L" width	120	=	ns	

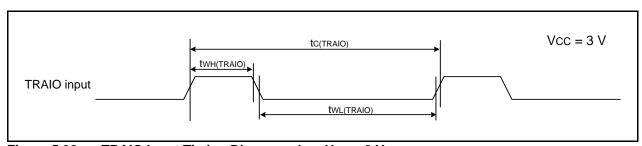


Figure 5.32 TRAIO Input Timing Diagram when Vcc = 3 V

Table 5.57 Serial Interface

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tc(CK)	CLK0 input cycle time	300	=	ns	
tw(ckh)	CLK0 input "H" width	150	=	ns	
tW(CKL)	CLK0 Input "L" width	150	=	ns	
td(C-Q)	TXDi output delay time	-	80	ns	
th(C-Q)	TXDi hold time		=	ns	
tsu(D-C)	RXDi input setup time		=	ns	
th(C-D)	RXDi input hold time		=	ns	

i = 0 or 1

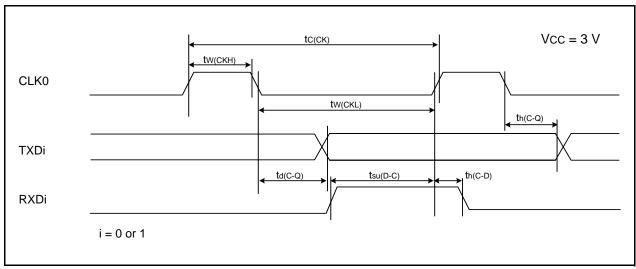


Figure 5.33 Serial Interface Timing Diagram when Vcc = 3 V

Table 5.58 External Interrupt INTi (i = 0, 1, 3) Input

Symbol	Parameter		Standard		
Symbol			Max.	Unit	
tW(INH)	INTi input "H" width	380(1)	-	ns	
tW(INL)	INTi input "L" width	380(2)	-	ns	

- 1. When selecting the digital filter by the INTi input filter select bit, use an INTi input HIGH width of either (1/digital filter clock frequency × 3) or the minimum value of standard, whichever is greater.
- 2. When selecting the digital filter by the INTi input filter select bit, use an INTi input LOW width of either (1/digital filter clock frequency x 3) or the minimum value of standard, whichever is greater.

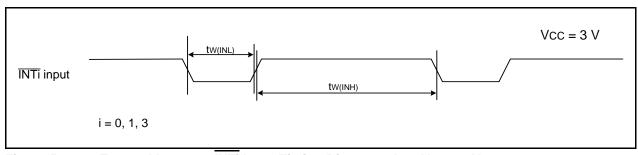
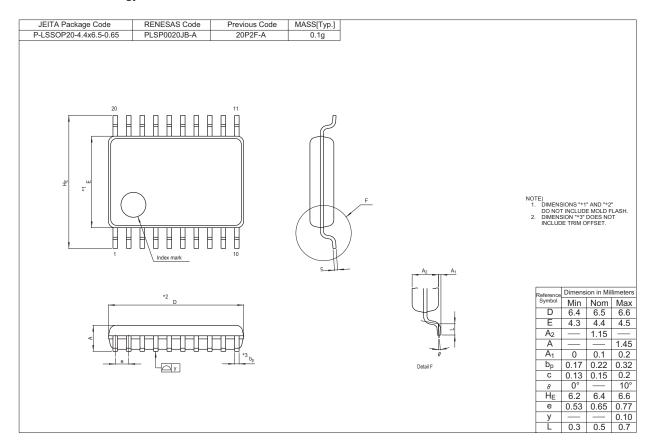


Figure 5.34 External Interrupt INTi Input Timing Diagram when Vcc = 3 V

## **Package Dimensions**

Diagrams showing the latest package dimensions and mounting information are available in the "Packages" section of the Renesas Technology website.



# REVISION HISTORY

# R8C/28 Group, R8C/29 Group Datasheet

D	Dete		Description
Rev.	Date	Page	Summary
0.10	Nov 14, 2005	-	First Edition issued
0.30	Feb 28, 2006	all pages	"J, K version" added
		1	1.1 Applications revised
		2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		4	Figure 1.1 Block Diagram; NOTE3 added
		5	Table 1.3 Product Information for R8C/28 Group and Figure 1.2 Type Number, Memory Size, and Package of R8C/28 Group revised
		6	Table 1.4 Product Information for R8C/29 Group and Figure 1.3 Type Number, Memory Size, and Package of R8C/29 Group revised
		7	Figure 1.4 Pin Assignments (Top View); NOTE3 added
		8	Table 1.5 Pin Functions revised
		9	Table 1.6 Pin Name Information by Pin Number; "XOUT" $\to$ "XOUT/XCOUT", "XIN" $\to$ "XIN/XCIN" revised and NOTE2 added
		13	Figure 3.1 Memory Map of R8C/28 Group; "R5F21284JSP, R5F21284KSP" added
		14	Figure 3.2 Memory Map of R8C/29 Group; "R5F21294JSP, R5F21294KSP" added
		15	Table 4.1 SFR Information (1); NOTE6 added
		18	Table 4.4 SFR Information (4); 00FEh: "DRR" → "P1DRR" symbol name revised
		22 to 66	5. Electrical Characteristics added
0.40	Mar 29, 2006	2	Table 1.1 Functions and Specifications for R8C/28 Group revised
		3	Table 1.2 Functions and Specifications for R8C/29 Group revised
		15	Table 4.1 SFR Information (1);
			- 0032h, 0036h, 0038h revised
		40	- NOTES 2 to 6 revised and NOTES 7 to 8 added
0.50	A== 07, 000C	19	Table 4.5 SFR Information (5); NOTE2 added
0.50	Apr 27, 2006	18	Table 4.4; 00FDh: revised
1.00	Nov 08, 2006	46	Table 5.35; System clock Conditions: revised  "PRELIMINARY" deleted
1.00	1100 06, 2006	All pages	1 "J and K versions are under developmentnotice." added
		1 2	Table 1.1 revised
		3	Table 1.1 revised  Table 1.2 revised
		4	Figure 1.1 revised
		5	Table 1.3 revised
		6	Table 1.4 revised
		l o	TUDIO 1T TUVIOUU

	D /	Description		
Rev.	Date	Page	Summary	
1.00	Nov 08, 2006	15	Table 4.1;  • "0000h to 003Fh" → "0000h to 002Fh" revised  • 000Fh: "000XXXXXb" → "00X11111b" revised  • 001Ch: "00h" → "00h, 10000000b" revised  • 0029h: "High-Speed On-Chip Oscillator Control Register 4, FRA4, When shipping" added  • 002Bh: "High-Speed On-Chip Oscillator Control Register 6, FRA6, When shipping" added  • NOTE2 revised, NOTE3 added	
		16	Table 4.2; "0040h to 007Fh" → "0030h to 007Fh" revised	
		18	Table 4.4; 00E1h, 00E5h, 00E8h "XXh" → "00h" revised	
		22	Table 5.2 revised	
		23	Figure 5.1 figure title revised	
		24	Table 5.4 revised	
		25	Table 5.5 revised	
		26	Figure 5.2 figure title revised and Table 5.7 NOTE4 added	
		27	Table 5.9 revised, Figure 5.3 revised	
		28	Table 5.10, Table 5.11revised	
		34	Table 5.15 revised	
		35	Table 5.16 revised	
		36	Table 5.17 revised	
		39	Table 5.22 revised	
		40	Table 5.23 revised	
		44	Table 5.29 revised	
		47	5.2 "J and K versions are under developmentnotice." added Table 5.34, Table 5.35 revised	
		48	Table 5.36 revised, Figure 5.20 figure title revised	
		51	Figure 5.21 figure title revised	
		52	Table 5.41, Figure 5.22 revised	
		53	Table 5.42, Table 5.43 revised	
		59	Table 5.47 revised	
		60	Table 5.48 revised	
		63	Table 5.53 revised	
		64	Table 5.54 revised	
		67	Package Dimensions; "Diagrams showing the latestwebsite." added	
1.10	May 17, 2007	2	Table 1.1 revised	
		3	Table 1.2 revised	
		5	Table 1.3 and Figure 1.2 revised	
		6	Table 1.4 and Figure 1.3 revised	
		7	Figure 1.4 NOTE4 added	

# **REVISION HISTORY**

# R8C/28 Group, R8C/29 Group Datasheet

Davi	Date	Description		
Rev.		Page	Summary	
1.10	May 17, 2007	13	Figure 3.1 revised	
		14	Figure 3.2 revised	
		18	Table 4.4 NOTE2 added	
		28	Table 20.10 revised	
		51	Table 20.39 NOTE4 added	
		53	Table 20.42 revised	
1.20a	Jun 11, 2007	1	1 "J and K versions are under development. Specifications may be changed without prior notice." deleted	
		5, 6	Table 1.3 and Table 1.4 "(D): Under development" and NOTE1 deleted	
		47	5.2 "J and K versions are under development. Specifications may be changed without prior notice." deleted	
2.00	Mar 14, 2008	5	Table 1.3, Figure 1.2 revised	
		6	Table 1.4, Figure 1.3 revised	
		13, 14	Figure 3.1, Figure 3.2 revised	
		15	Table 4.1 "002Ch" added	
		16	Table 4.2 "0036h"; J, K version "0100X000b" → "0100X001b"	
		22, 47	Table 5.2, Table 5.35; NOTE2 revised	
		28	Table 5.10 revised, NOTE4 added	
2.10	2.10 Sep 26, 2008		"RENESAS TECHNICAL UP DATE" reflected: TN-16C-A172A/E	
		24, 49	Table 5.4, Table 5.37 NOTE2, NOTE4 revised	
		25, 50	Table 5.5, Table 5.38 NOTE2, NOTE5 revised	
		51	Table 5.39 Parameter: Voltage monitor 1 reset generation time added NOTE5 added Table 5.40 revised	
		52	Table 5.41 revised	
			Figure 5.22 revised	

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