## Description

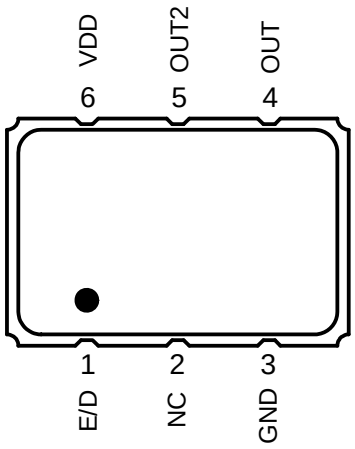
The XLP is an LVPECL crystal oscillator with 860fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the IDT XLP series crystal oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLP is an excellent choice over the conventional technologies. The XLP has stabilities as tight as ±20ppm with extremely quick delivery for both standard and custom frequencies

## Features

- Frequency range: 0.750 to 1350MHz
- Output type: LVPECL
- Frequency stability: ±20ppm, ±25ppm, ±50ppm, or ±100ppm
- Supply voltage: 2.5V or 3.3V
- Phase jitter (1.875MHz to 20MHz): 225fs typical
- Phase jitter (12kHz to 20MHz): 860fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)
  7.0mm x 5.0mm x 1.3mm (JU6)
- Operating temperatures: -20°C to +70°C or -40°C to +85°C

## Pin Assignment




**6-pin CLCC**

## Pin Descriptions

| Pin Number | Pin Name | Description |
|---|---|---|
| 1 | E/D | Enable/Disable[1] (0=Output Disabled) |
| 2 | NC | No connect |
| 3 | GND | Connect to ground |
| 4 | OUT | Output |
| 5 | OUT2 | Complementary Output |
| 6 | VDD | Supply voltage |

1. Pulled high internally.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XLP. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

| Item | Rating |
|---|---|
| VDD | -0.5 to +5.0V |
| E/D | -0.5V to VDD + 0.5V |
| OUT | -0.5V to VDD + 0.5V |
| Storage Temperature | -55°C to 125°C |
| Theta Ja (Junction to Ambient) | 102°C/W – Still Air |

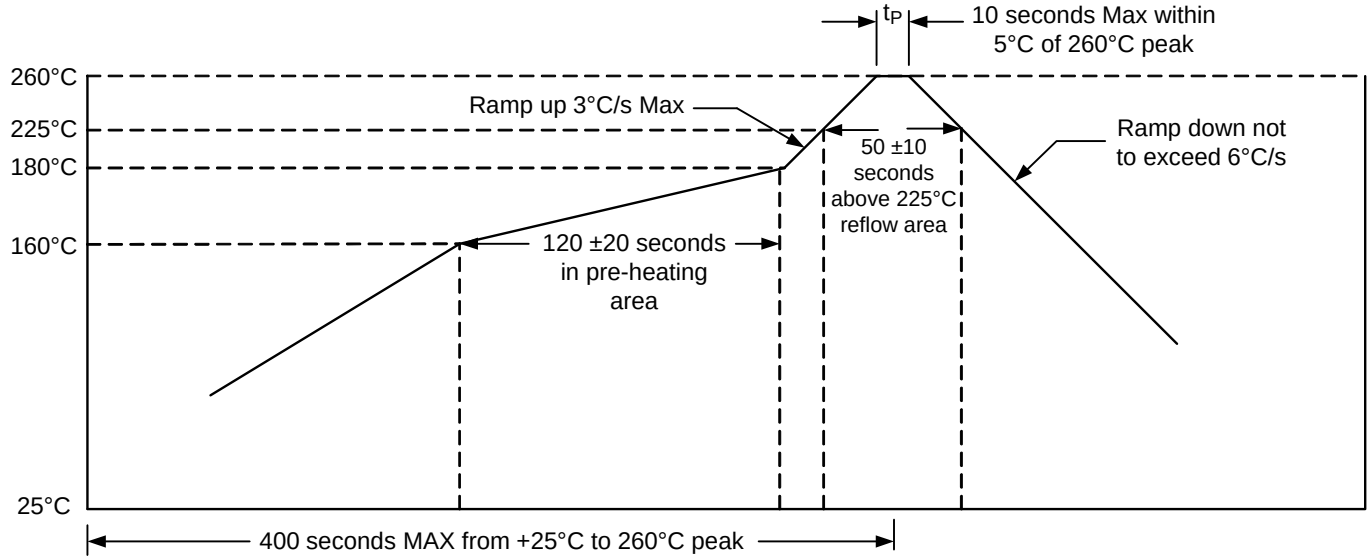
## ESD Compliance

| | |
|---|---|
| Human Body Model (HBM | 1000V |
| Machine Model (MM) | 150V |

## Mechanical Testing

| Parameter | Test Method |
|---|---|
| Mechanical Shock | Drop from 75cm to hardwood surface–3 times |
| Mechanical Vibration | 10~55Hz, 1.5mm amplitude, 1 minute sweep<br>2 hours each in 3 directions (X, Y, Z) |
| High Temperature Burn-in | Under power at 125°C for 2000 hours |
| Hermetic Seal | He pressure: 4 ±1kgf/cm$^2$ 2 hour soak |

## Solder Reflow Profile



# DC Characteristics

($V_{DD}$= **3.3V** ±5%, $T_A$= - 20°C to +70°C; -40° to +85°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{DD}$ | Common Frequencies | | | 120 | mA |
| Output HIGH Voltage | $V_{OH}$ | Standard LVPECL load | 2.055 | | 2.405 | V |
| Output LOW Voltage | $V_{OL}$ | Standard LVPECL load | 1.305 | | 1.650 | V |
| Enable/Disable Input HIGH Voltage (Output enabled)* | $V_{IH}$ | | 70%$V_{DD}$ | | | V |
| Enable/Disable Input LOW Voltage (Output disabled) | $V_{IL}$ | | | | 30%$V_{DD}$ | V |

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

# AC Characteristics

($V_{DD}$= **3.3V** ±5%, $T_A$= - 20°C to +70°C; -40° to +85°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Frequency Range | $F_{OUTR}$ | | 0.750 | | 1350 | MHz |
| Frequency Stability | | Temperature = -20°C to +70°C | ±20 | | ±100 | ppm |
| | | Temperature = -40°C to +85°C | ±25 | | ±100 | ppm |
| Aging (1st year) | | Ta = 25°C | | | 3 | |
| Aging (10 years) | | Ta = 25°C | | | 10 | |
| Output Load | | To $V_{DD}$ - 2.0V | | 50 | | Ohms |
| Start-up Time | $T_{ST}$ | Output valid time after VDD meets minimum specified level | | | 10 | ms |
| Output Rise Time | | 20% to 80% $V_{PP}$ | | | 400 | ps |
| Output Fall Time | | 80% to 20% $V_{PP}$ | | | 400 | ps |
| Output Clock Duty Cycle | $T_{DTCY}$ | 50% $V_{P-P}$ | 45 | | 55 | % |
| Output Enable/ Disable Time | $T_{OE}$ | | | | 100 | ns |
| Period Jitter, RMS | $J_{PER}$ | Frequency = 156.25MHz | | 5.80 | | ps |
| Random Jitter | $R_J$ | Frequency = 156.25MHz<br>Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications) | | 1.29 | | ps |
| Deterministic Jitter | $D_J$ | | | 9.3 | | ps |
| Total Jitter | $T_J$ | | | 27.7 | | ps |
| Phase Jitter (12kHz – 20MHz) | $\phi_{JITTER}$ | Common Frequencies | | 860 | | fs |
| Phase Noise Performance Frequency = 156.25MHz | $\phi_{NOISE}$ | 100Hz of Carrier | | -80 | | dBc/Hz |
| | | 1kHz of Carrier | | -115 | | dBc/Hz |
| | | 10kHz of Carrier | | -117 | | dBc/Hz |
| | | 100kHz of Carrier | | -121 | | dBc/Hz |
| | | 1MHz of Carrier | | -142 | | dBc/Hz |
| | | 10MHz of Carrier | | -150 | | dBc/Hz |
| Output Frequency (Common) | $F_{OUT}$ | 100MHz, 106.25MHz, 1258MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHZ, 400MHz<br>(Contact IDT for additional frequencies) | | | | |

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

## DC Characteristics

($V_{DD}$= **2.5V** ±5%, $T_A$= - 20°C to +70°C; -40° to +85°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Power Supply Current | $I_{DD}$ | Common Frequencies | 33 | | 72 | mA |
| Output HIGH Voltage | $V_{OH}$ | Standard LVPECL load | | 1.40 | | V |
| Output LOW Voltage | $V_{OL}$ | Standard LVPECL load | | 0.68 | | V |
| Enable/Disable Input HIGH Voltage (Output enabled)* | $V_{IH}$ | | 70%$V_{DD}$ | | | V |
| Enable/Disable Input LOW Voltage (Output disabled) | $V_{IL}$ | | | | 30%$V_{DD}$ | V |

* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

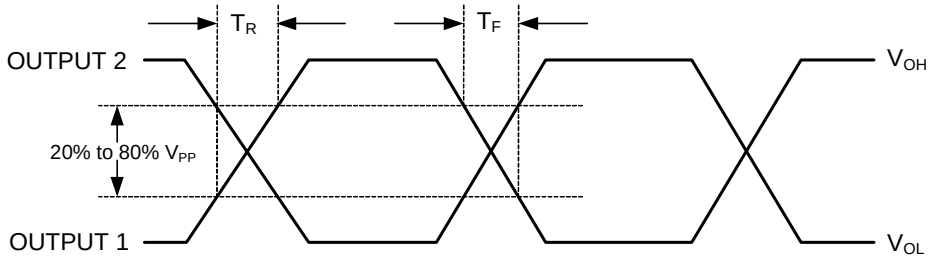
($V_{DD}$= **2.5V** ±5%, $T_A$= - 20°C to +70°C; -40° to +85°C)

| Parameter | Symbol | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Output Frequency Range | $F_{OUTR}$ | | 0.750 | | 1000 | MHz |
| Frequency Stability | | Temperature = -20°C to +70°C | ±20 | | ±100 | ppm |
| | | Temperature = -40°C to +85°C | ±25 | | ±100 | ppm |
| Output Load | | To $V_{DD}$ - 2.0V | | 50 | | Ohms |
| Start-up Time | $T_{ST}$ | Output valid time after VDD meets minimum specified level | | | 10 | ms |
| Output Rise Time | | 20% to 80% $V_{PP}$ | | | 400 | ps |
| Output Fall Time | | 80% to 20% $V_{PP}$ | | | 400 | ps |
| Output Clock Duty Cycle | $T_{DTCY}$ | 50% $V_{P-P}$ | 45 | | 55 | % |
| Output Enable/ Disable Time | $T_{OE}$ | | | | 100 | ns |
| Period Jitter, RMS | $J_{PER}$ | Frequency = 156.25MHz | | 5.12 | | ps |
| Random Jitter | $R_J$ | Frequency = 156.25MHz Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications) | | 1.36 | | ps |
| Deterministic Jitter | $D_J$ | | | 10.0 | | ps |
| Total Jitter | $T_J$ | | | 29.3 | | ps |
| Phase Jitter (12kHz – 20MHz) | $\phi_{JITTER}$ | Frequency = 156.25MHz | | 1200 | | fs |
| Phase Noise Performance Frequency = 156.25MHz | $\phi_{NOISE}$ | 100Hz of Carrier | | -83.2 | | dBc/Hz |
| | | 1kHz of Carrier | | -106.5 | | dBc/Hz |
| | | 10kHz of Carrier | | -115.6 | | dBc/Hz |
| | | 100kHz of Carrier | | -120.2 | | dBc/Hz |
| | | 1MHz of Carrier | | -136.1 | | dBc/Hz |
| | | 10MHz of Carrier | | -145.9 | | dBc/Hz |
| Output Frequency (Standards) | $F_{OUT}$ | 100MHz, 106.25MHz, 1258MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHZ, 400MHz (Contact IDT for additional frequencies) | | | | |

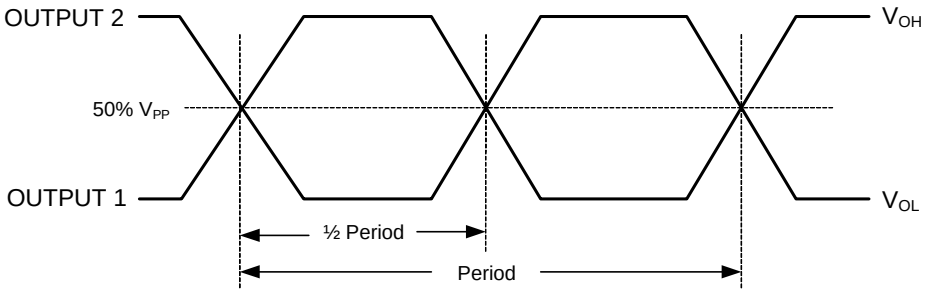
Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

## Output Waveform

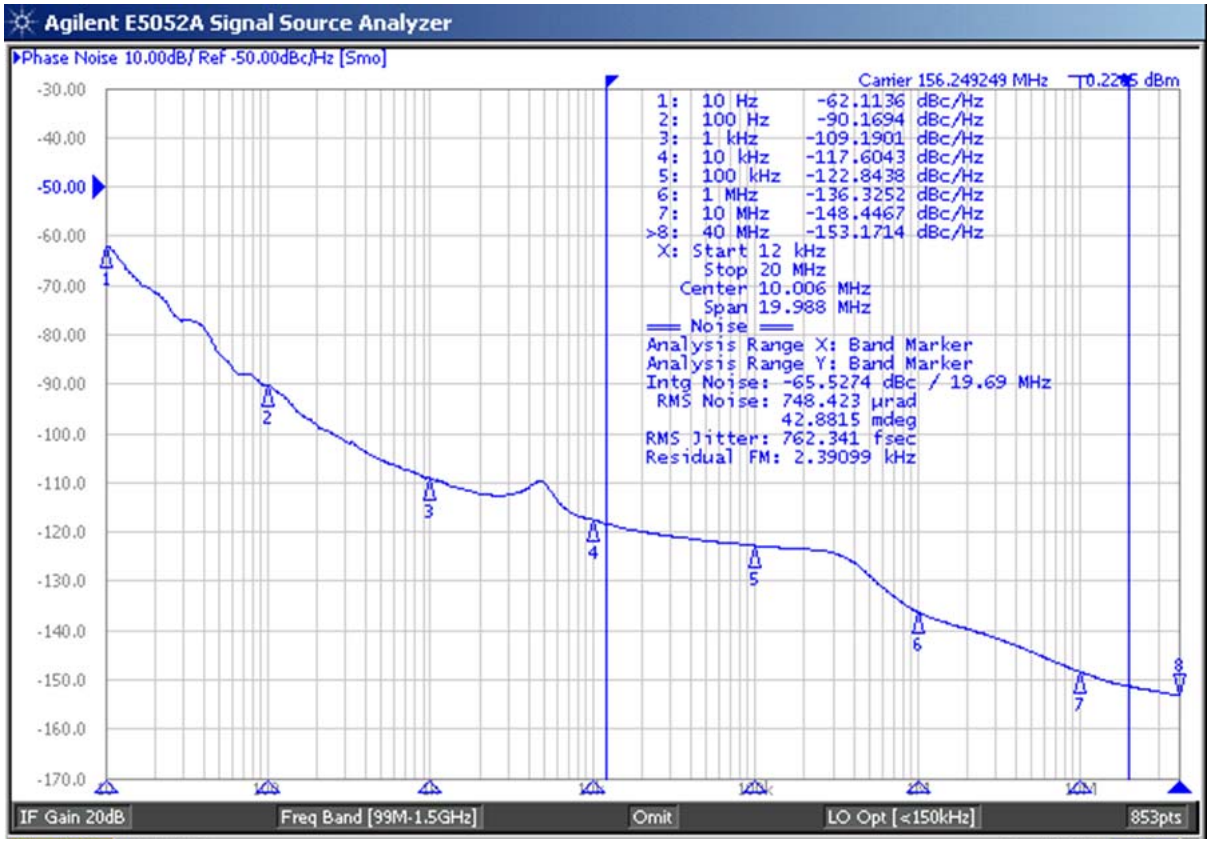
**Rise Time/Fall Time Measurements**



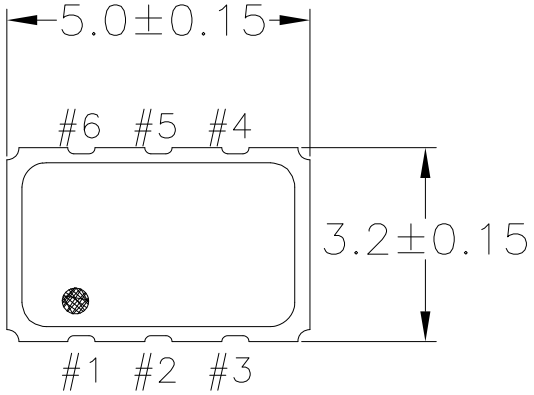

**Oscillator Symmetry**



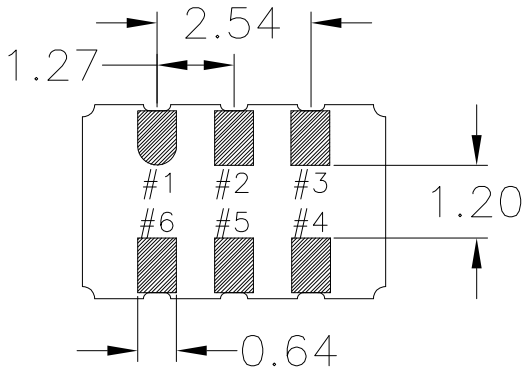

## Typical Phase Noise (3.3V)



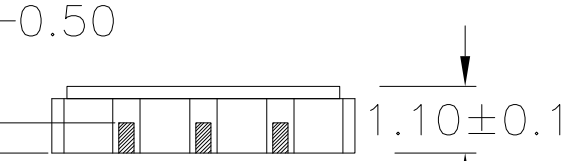
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/2/12 | DP |
| 01 | ADDED LID IN TOP VIEW | 07/12/12 | KS |
| 02 | UPDATED LID TOLERANCES | 12/03/12 | KS |
| 03 | UPDATE PACKAGE DRAWING | 8/8/14 | J.HUA |




TOP VIEW




BOTTOM VIEW

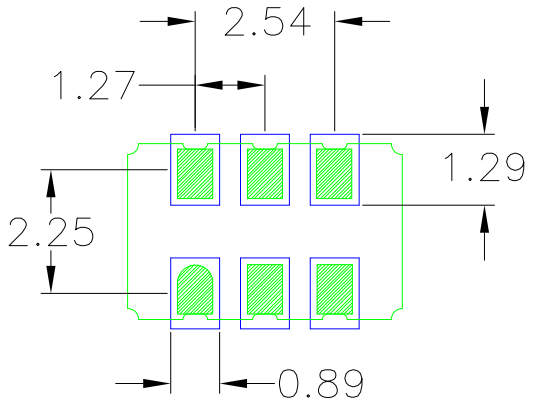



SIDE VIEW

DIMENSIONS IN MM.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JS6 PACKAGE OUTLINE<br>5.0 x 3.2 mm BODY<br>1.1 mm Thick |
| DRAWN RdC | 04/2/12 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4411 REV 03 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 04/2/12 | DP |
| 01 | ADDED LID IN TOP VIEW | 07/12/12 | KS |
| 02 | UPDATED LID TOLERANCES | 12/03/12 | KS |
| 03 | UPDATE PACKAGE DRAWING | 8/8/14 | J.HUA |

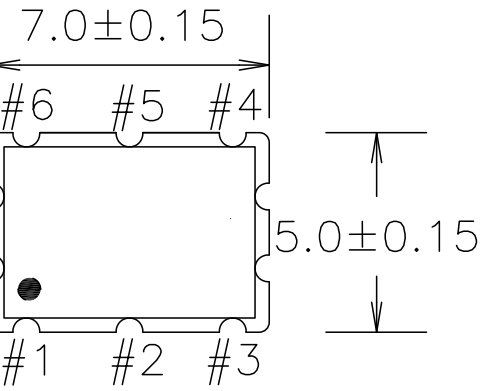



RECOMMENDED LAND PATTERN

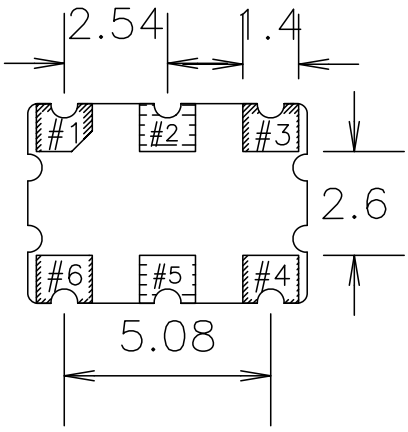
DIMENSION ARE IN mm. ANGLES IN DEGREES.
DOWN VIEW. AS VIEWED ON PCB.
MPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
D PATTERN IN BLUE. NSMD PATTERN ASSUMED.
D PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
R SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JS6 PACKAGE OUTLINE<br>5.0 x 3.2 mm BODY<br>1.1 mm Thick |
| DRAWN RAC | 04/2/12 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4411 REV 03 |
| | | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

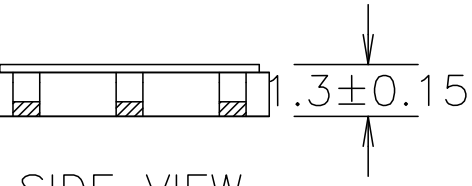
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/5/12 | KS |
| 01 | UPDATE PACKAGE DRWING | 8/12/14 | J.HUA |




TOP VIEW




BOTTOM VIEW

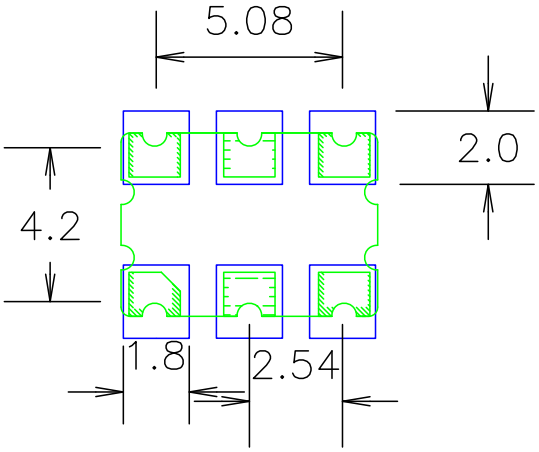



SIDE VIEW

NOTES:
1. ALL DIMENSIONS IN MM.

| | | | |
|---|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS | DATE | TITLE | JU6 PACKAGE OUTLINE<br>7.0 x 5.0 mm BODY<br>1.3 mm Thick |
| DRAWN JCS | 10/03/12 | | |
| CHECKED | | | |
| | | SIZE C | DRAWING No. PSC-4430 REV 01 |
| | | DO NOT SCALE DRAWING | SHEET 1 OF 2 |

| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APPROVED |
| 00 | INITIAL RELEASE | 10/5/12 | KS |
| 01 | UPDATE PACKAGE DRWING | 8/12/14 | J.HUA |

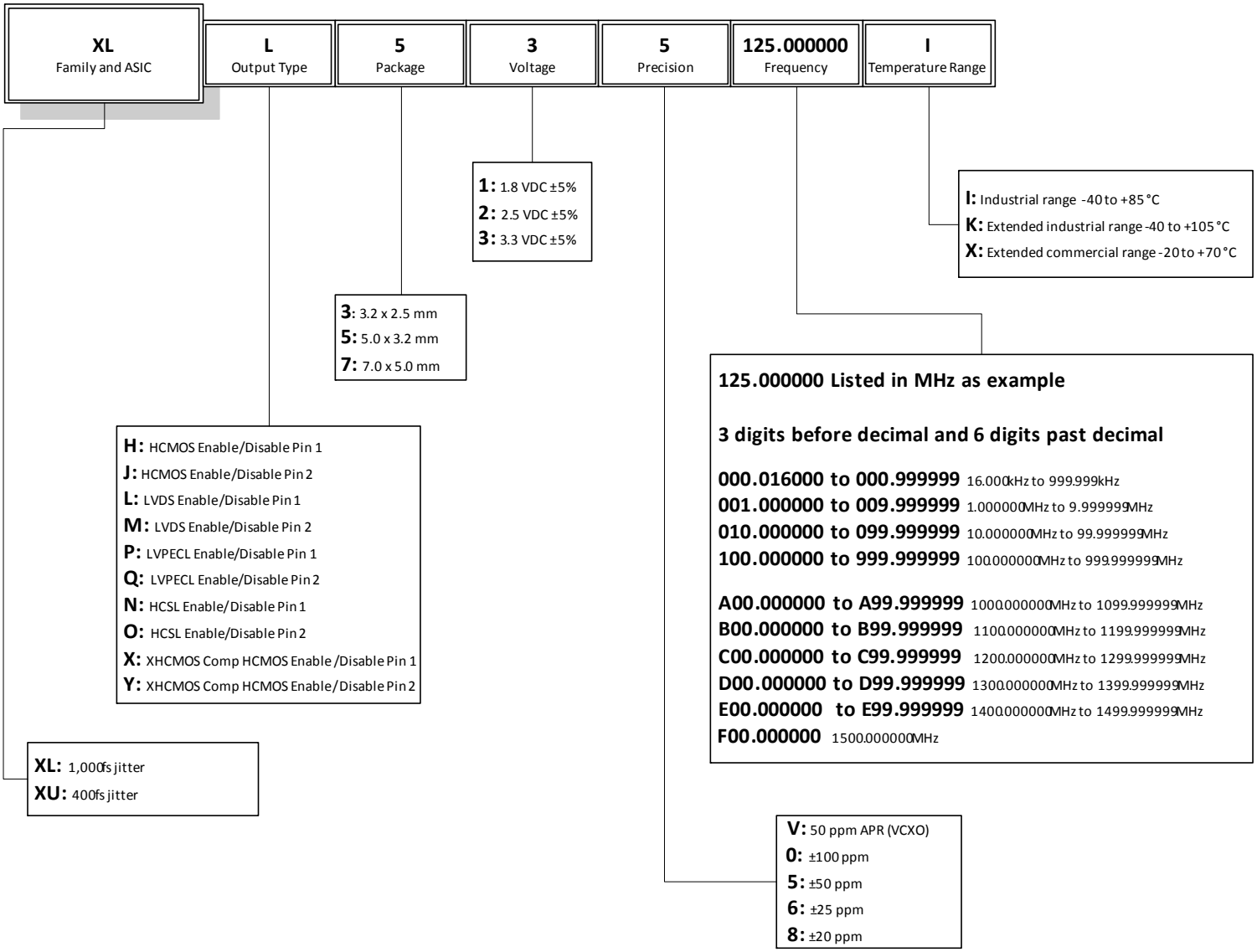



RECOMMENDED LAND PATTERN

DIMENSION ARE IN mm. ANGLES IN DEGREES.
DOWN VIEW. AS VIEWED ON PCB.
PONENT OUTLINE SHOW FOR REFERENCE IN GREEN.
PATTERN IN BLUE. NSMD PATTERN ASSUMED.
PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT
SURFACE MOUNT DESIGN AND LAND PATTERN.

| | | |
|---|---|---|
| TOLERANCES UNLESS SPECIFIED<br>DECIMAL ANGULAR<br>XX± ±<br>XXX±<br>XXXX± | IDT™ www.IDT.com | 6024 Silver Creek Valley Rd<br>San Jose, CA 95138<br>PHONE: (408) 727-6116<br>FAX: (408) 492-8674 |
| APPROVALS / DATE | TITLE | JU6 PACKAGE OUTLINE<br>7.0 x 5.0 mm BODY<br>1.3 mm Thick |
| DRAWN JCS 10/03/12 | | |
| CHECKED | | |
| | SIZE C | DRAWING No. PSC-4430 REV 01 |
| | DO NOT SCALE DRAWING | SHEET 2 OF 2 |

# IDT Ordering Information



## Revision History

| Date | Originator | Description of Change |
|---|---|---|
| 10/17/14 | B. Chandhoke | Initial release. |
| 12/10/14 | B. Chandhoke | 1. Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings.<br>2. Updated ordering information table/graphic to show JU6 package option. |
| 10/28/16 | P. Jenkins | Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables. |
| 06/13/17 | L.S. | Removed “Ordering Information Scheme #1 (for reference only)”. Replaced with a single ordering information table. |
| 06/20/17 | L.S. | Corrected frequency errors in Ordering Information table. |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