

### Description

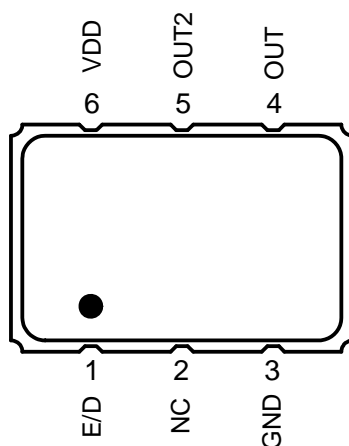
The XLP is an LVPECL crystal oscillator with 860fs typical phase jitter over 12kHz to 20MHz bandwidth. Available in a wide frequency range from 0.750MHz to 1350MHz, the IDT XLP series crystal oscillator utilizes a family of proprietary ASICs, with a key focus on noise reduction technologies.

The 3rd order Delta Sigma Modulator reduces noise to the levels that are comparable to traditional bulk Quartz and SAW oscillators. With short lead-time, low cost, low noise, wide frequency range, excellent ambient performance, the XLP is an excellent choice over the conventional technologies. The XLP has stabilities as tight as  $\pm 20\text{ppm}$  with extremely quick delivery for both standard and custom frequencies

### Features

- Frequency range: 0.750 to 1350MHz
- Output type: LVPECL
- Frequency stability:  $\pm 20\text{ppm}$ ,  $\pm 25\text{ppm}$ ,  $\pm 50\text{ppm}$ , or  $\pm 100\text{ppm}$
- Supply voltage: 2.5V or 3.3V
- Phase jitter (1.875MHz to 20MHz): 225fs typical
- Phase jitter (12kHz to 20MHz): 860fs typical
- Package options: 5.0mm x 3.2mm x 1.2mm (JS6)  
7.0mm x 5.0mm x 1.3mm (JU6)
- Operating temperatures:  $-20^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$  or  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$

### Pin Assignment



6-pin CLCC

### Pin Descriptions

Pin Number	Pin Name	Description
1	E/D	Enable/Disable <sup>1</sup> (0=Output Disabled)
2	NC	No connect
3	GND	Connect to ground
4	OUT	Output
5	OUT2	Complementary Output
6	VDD	Supply voltage

1. Pulled high internally.

## Absolute Maximum Ratings

Stresses above the ratings listed below can cause permanent damage to the XLP. These ratings, which are standard values for IDT commercially rated parts, are stress ratings only. Functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods can affect product reliability. Electrical parameters are guaranteed only over the recommended operating temperature range.

Item	Rating
VDD	-0.5 to +5.0V
E/D	-0.5V to VDD + 0.5V
OUT	-0.5V to VDD + 0.5V
Storage Temperature	-55°C to 125°C
Theta Ja (Junction to Ambient)	102°C/W – Still Air

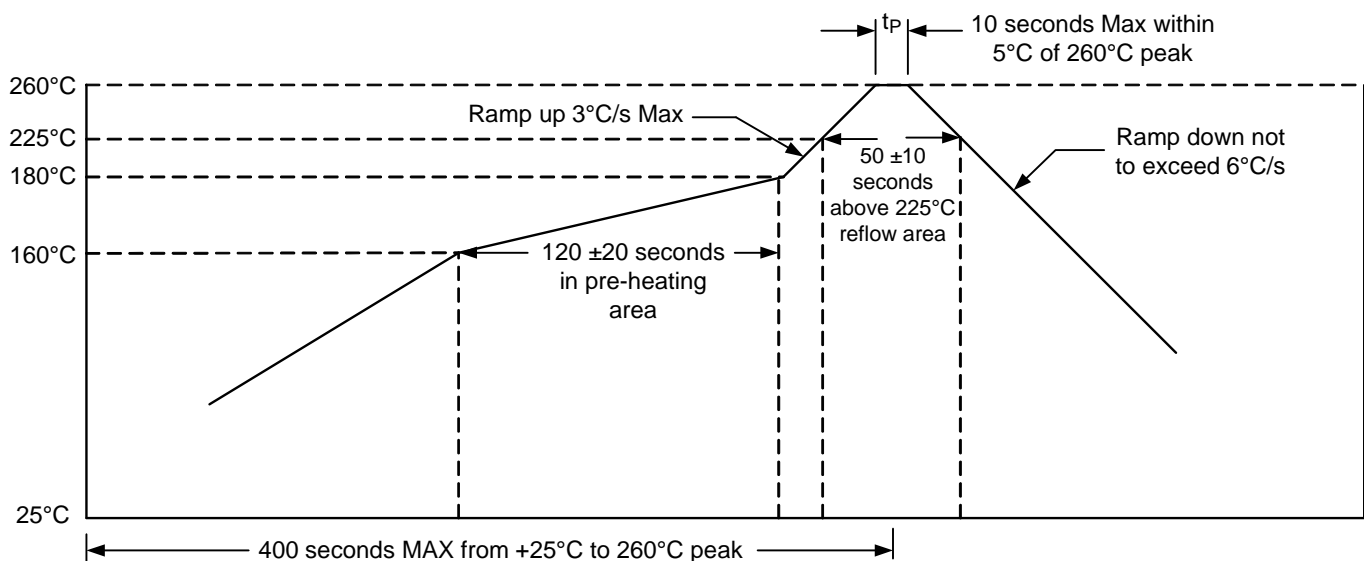
## ESD Compliance

Human Body Model (HBM)	1000V
Machine Model (MM)	150V

## Mechanical Testing

Parameter	Test Method
Mechanical Shock	Drop from 75cm to hardwood surface–3 times
Mechanical Vibration	10~55Hz, 1.5mm amplitude, 1 minute sweep 2 hours each in 3 directions (X, Y, Z)
High Temperature Burn-in	Under power at 125°C for 2000 hours
Hermetic Seal	He pressure: $4 \pm 1 \text{kgf/cm}^2$ 2 hour soak

## Solder Reflow Profile



## DC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies			120	mA
Output HIGH Voltage	$V_{OH}$	Standard LVPECL load	2.055		2.405	V
Output LOW Voltage	$V_{OL}$	Standard LVPECL load	1.305		1.650	V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

## AC Characteristics

( $V_{DD} = 3.3V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1350	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Aging (1 <sup>st</sup> year)		$T_a = 25^\circ C$			3	
Aging (10 years)		$T_a = 25^\circ C$			10	
Output Load		To $V_{DD} - 2.0V$		50		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		5.80		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.29		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		9.3		ps
Total Jitter	$T_J$			27.7		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Common Frequencies		860		fs
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-80		dBc/Hz
		1kHz of Carrier		-115		dBc/Hz
		10kHz of Carrier		-117		dBc/Hz
		100kHz of Carrier		-121		dBc/Hz
		1MHz of Carrier		-142		dBc/Hz
		10MHz of Carrier		-150		dBc/Hz
Output Frequency (Common)	$F_{OUT}$	100MHz, 106.25MHz, 125.8MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at  $25^\circ C$ . We do not recommend hand soldering the devices

## DC Characteristics

( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

Parameter	Symbol	Condition	Min	Typ	Max	Units
Power Supply Current	$I_{DD}$	Common Frequencies	33		72	mA
Output HIGH Voltage	$V_{OH}$	Standard LVPECL load		1.40		V
Output LOW Voltage	$V_{OL}$	Standard LVPECL load		0.68		V
Enable/Disable Input HIGH Voltage (Output enabled)*	$V_{IH}$		$70\%V_{DD}$			V
Enable/Disable Input LOW Voltage (Output disabled)	$V_{IL}$				$30\%V_{DD}$	V

\* A pullup resistor from pin 6 (VDD) to pin 1 (E/D) enables output when pin 1 is left open.

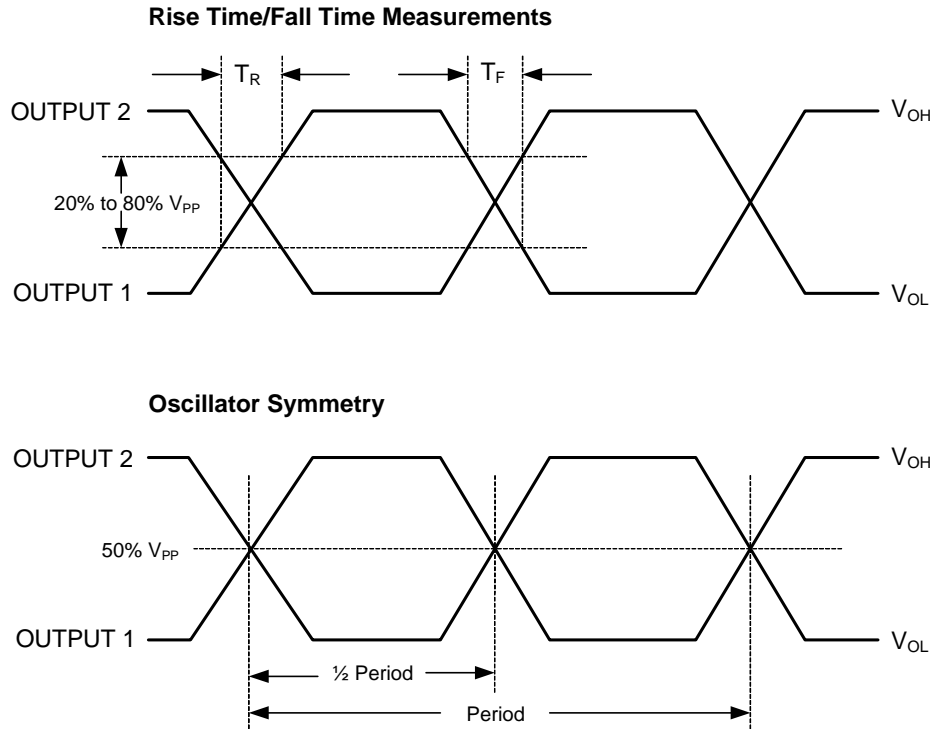
## AC Characteristics

( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = -20^\circ C$  to  $+70^\circ C$ ;  $-40^\circ$  to  $+85^\circ C$ )

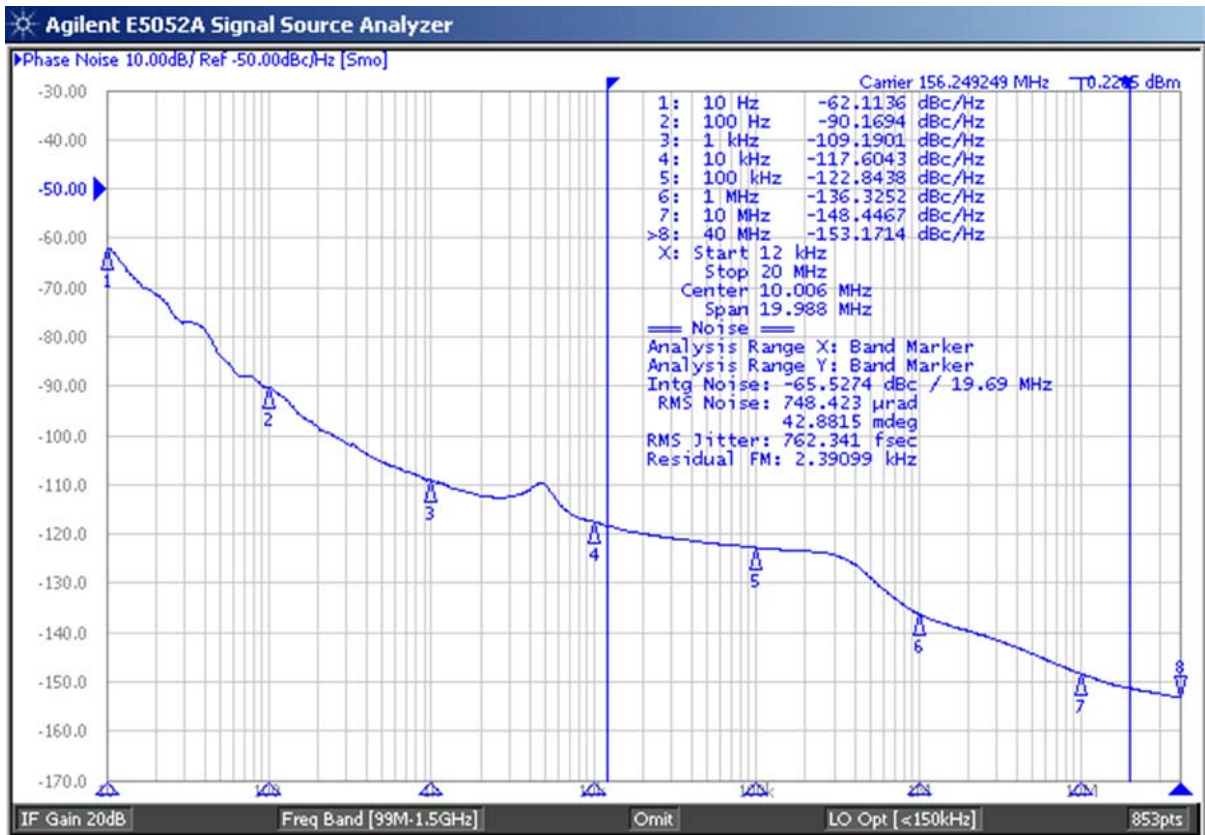
Parameter	Symbol	Condition	Min	Typ	Max	Units
Output Frequency Range	$F_{OUTR}$		0.750		1000	MHz
Frequency Stability		Temperature = $-20^\circ C$ to $+70^\circ C$	$\pm 20$		$\pm 100$	ppm
		Temperature = $-40^\circ C$ to $+85^\circ C$	$\pm 25$		$\pm 100$	ppm
Output Load		To $V_{DD} - 2.0V$		50		Ohms
Start-up Time	$T_{ST}$	Output valid time after VDD meets minimum specified level			10	ms
Output Rise Time		20% to 80% $V_{PP}$			400	ps
Output Fall Time		80% to 20% $V_{PP}$			400	ps
Output Clock Duty Cycle	$T_{DTCY}$	50% $V_{P-P}$	45		55	%
Output Enable/ Disable Time	$T_{OE}$				100	ns
Period Jitter, RMS	$J_{PER}$	Frequency = 156.25MHz		5.12		ps
Random Jitter	$R_J$	Frequency = 156.25MHz		1.36		ps
Deterministic Jitter	$D_J$	Per MJSQ spec (Methodologies for Jitter and Signal Quality specifications)		10.0		ps
Total Jitter	$T_J$			29.3		ps
Phase Jitter (12kHz – 20MHz)	$\phi_{JITTER}$	Frequency = 156.25MHz		1200		fs
Phase Noise Performance Frequency = 156.25MHz	$\phi_{NOISE}$	100Hz of Carrier		-83.2		dBc/Hz
		1kHz of Carrier		-106.5		dBc/Hz
		10kHz of Carrier		-115.6		dBc/Hz
		100kHz of Carrier		-120.2		dBc/Hz
		1MHz of Carrier		-136.1		dBc/Hz
		10MHz of Carrier		-145.9		dBc/Hz
Output Frequency (Standards)	$F_{OUT}$	100MHz, 106.25MHz, 125.8MHz, 150MHz, 155.52MHz, 156.25MHz, 200MHz, 212.5MHz, 250MHz, 300MHz, 312.5MHz, 400MHz (Contact IDT for additional frequencies)				

Note: Inclusive of initial frequency accuracy, operating temperature range, supply variation, load variation, 3 times solder reflow, shock, vibration and 1 year aging at 25°C. We do not recommend hand soldering the devices

## Output Waveform



## Typical Phase Noise (3.3V)



REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	04/2/12	DP
01	ADDED LID IN TOP VIEW	07/12/12	KS
02	UPDATED LID TOLERANCES	12/03/12	KS
03	UPDATE PACKAGE DRAWING	8/8/14	JHVA

REVISIONS	
REV	DATE
DESCRIPTION	
APPROVED	

TOLERANCES	
UNLESS SPECIFIED	
DECIMAL	±
ANGULAR	±
XXX#	
XXXX#	
APPROVALS	DATE
DRAWN <i>WAC</i>	04/2/12
CHECKED	
SIZE	C
DRAWING No.	PSC-4411
REV	03

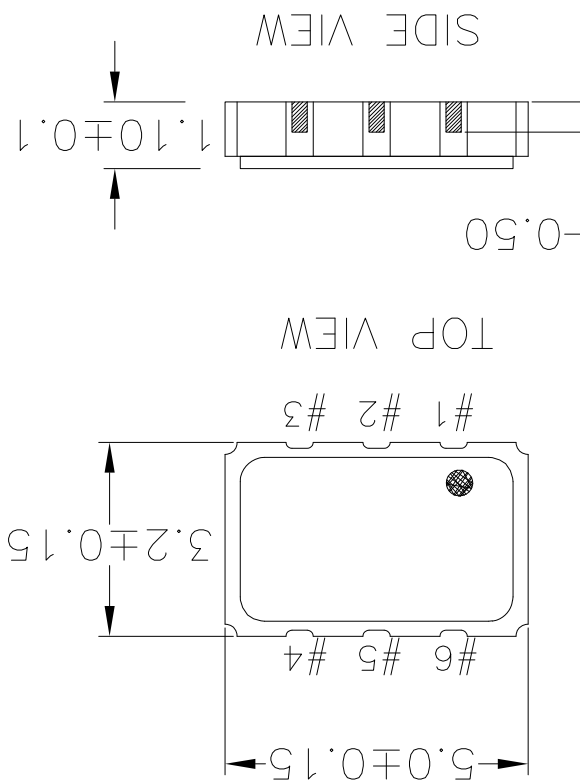
TITLE	
J56 PACKAGE OUTLINE	
5.0 x 3.2 mm BODY	
1.1 mm Thick	

DO NOT SCALE DRAWING	
SHEET 1 OF 2	

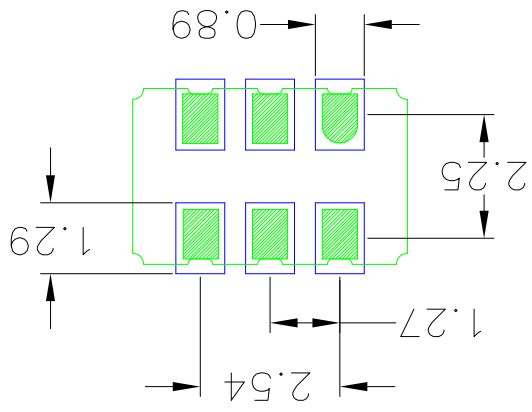
6024 Silver Creek Valley Rd  
 San Jose, CA 95138  
 PHONE: (408) 727-6116  
 FAX: (408) 492-8674  
**IDT**™  
 WWW.IDT.COM



DIMENSIONS IN MM.

DOWN VIEW, AS VIEWED ON PCB.  
 DIMENSION ARE IN mm. ANGLES IN DEGREES.  
 COMPONENT OUTLINE SHOW FOR REFERENCE IN GREEN.  
 D PATTERN IN BLUE. NSMD PATTERN ASSUMED.  
 D PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT  
 & SURFACE MOUNT DESIGN AND LAND PATTERN.

RECOMMENDED LAND PATTERN




REV	DATE	DESCRIPTION	APPROVED
00	04/2/12	INITIAL RELEASE	DP
01	07/12/12	ADDED LID IN TOP VIEW	KS
02	12/03/12	UPDATE LID TOLERANCES	KS
03	8/8/14	UPDATE PACKAGE DRAWING	JHUA

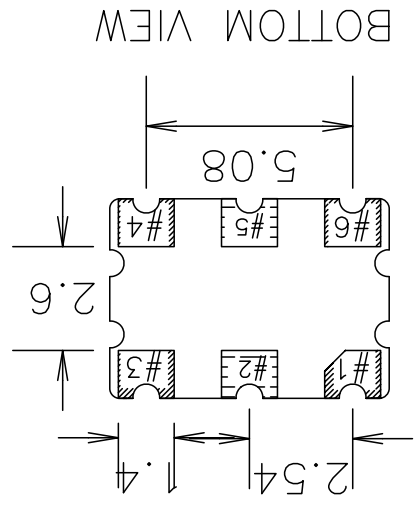
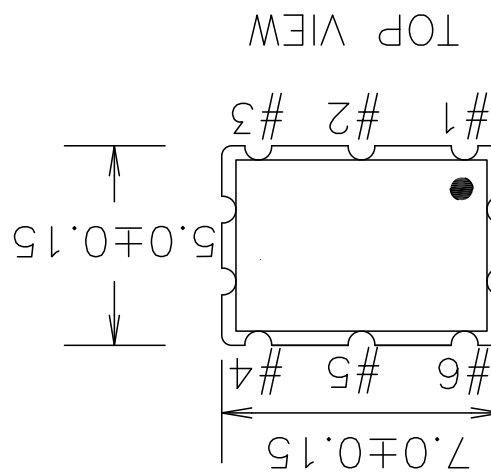
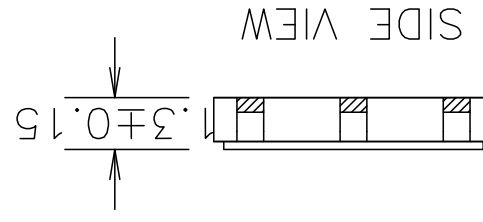
TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XXX	±
XXXX	
APPROVALS	DATE
DRM/BAG	04/2/12
CHECKED	
TITLE	5.0 x 3.2 mm BODY
	1.1 mm Thick
SIZE	PSC-4411
REV	03
DO NOT SCALE DRAWING	
SHEET 2 OF 2	

	6024 Silver Creek Valley Rd San Jose, CA 95138 Phone: (408) 727-8116 Fax: (408) 492-8874 www.idt.com
--	--

DO NOT SCALE DRAWING	SHEET 1 OF 2
SIZE C	DRAWING No. PSC-4430
REV 01	
APPROVALS	DATE
DRWN XZ	10/03/12
CHECKED	
TITLE	7.0 x 5.0 mm BODY
	1.3 mm thick
 www.idt.com Son Jose, CA 95138 PHONE: (408) 727-6116 FAX: (408) 492-8874	
TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR ± XXXX XXX XXX	

NOTES:  
1. ALL DIMENSIONS IN MM.



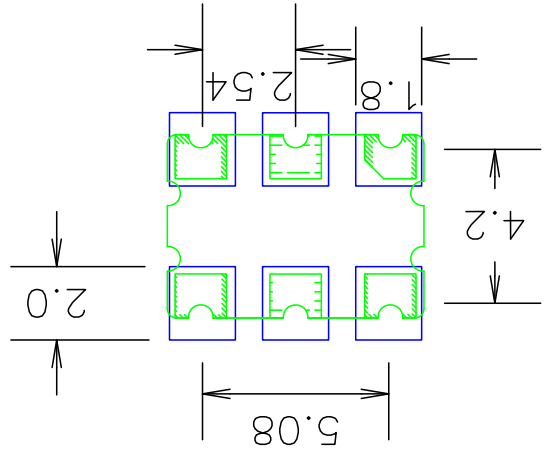
REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWNG	8/12/14	JHVA



DO NOT SCALE DRAWING		SHEET 2 OF 2	
REV	01	SIZE	C
DRAWING No. PSC-4430		TITLE J06 PACKAGE OUTLINE	
7.0 x 5.0 mm BODY		1.3 mm Thick	
APPROVALS	DATE	CHECKED	DRAWN %S
XXXXX	10/03/12		
TOLERANCES UNLESS SPECIFIED			
DECIMAL ±			
ANGULAR			
XXX°			
XXXX			
XXXXX			
WWW.IDT.COM			
IDT			
6024 Silver Creek Valley Rd			
San Jose, CA 95138			
PHONE: (408) 777-8118			
FAX: (408) 482-8874			

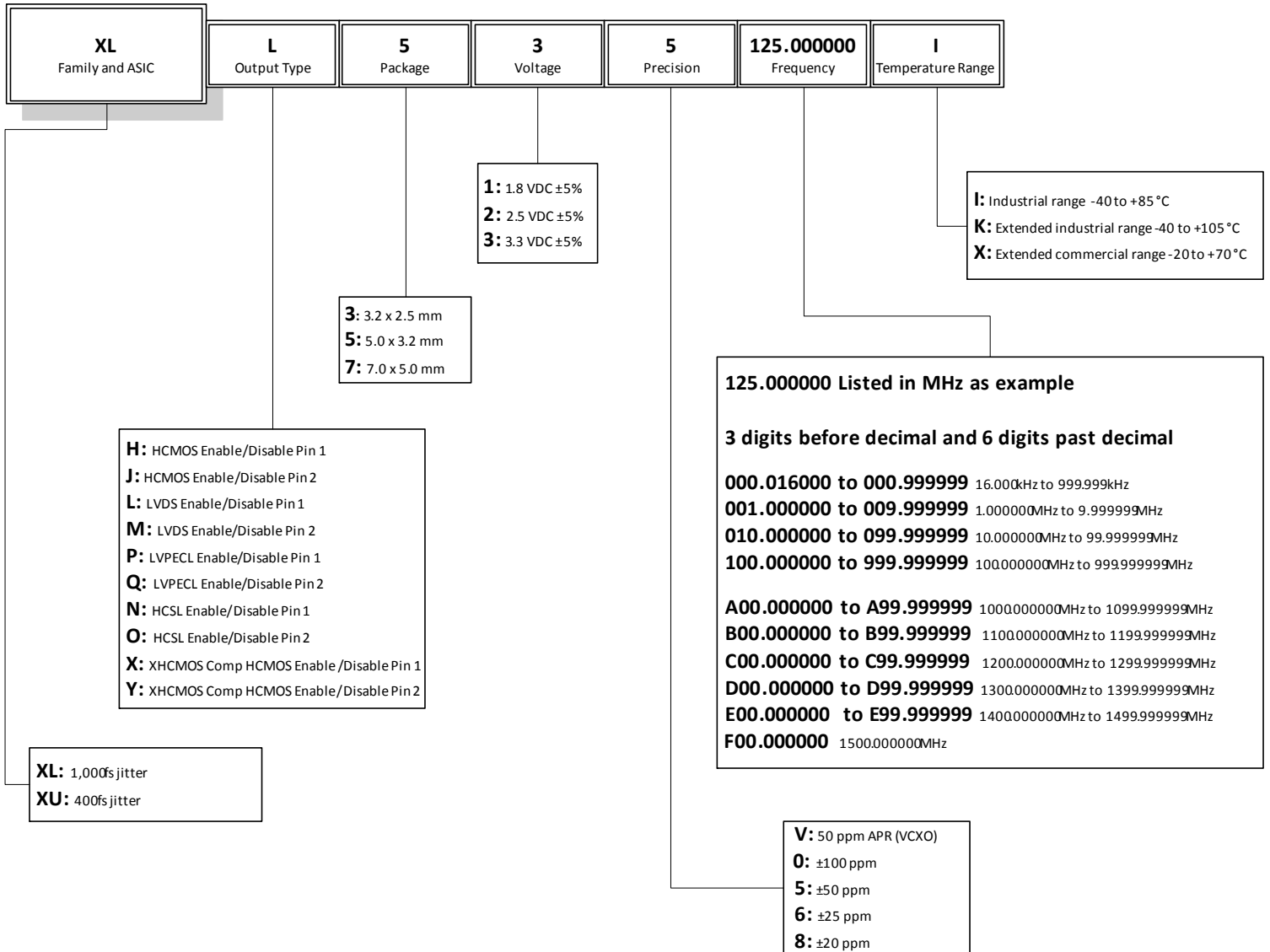
DIMENSION ARE IN mm. ANGLES IN DEGREES.  
DOWN VIEW, AS VIEWED ON PCB.  
DOWNLINE SHOW FOR REFERENCE IN GREEN.  
PATTERN IN BLUE. NSMD PATTERN ASSUMED.  
PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT  
SURFACE MOUNT DESIGN AND LAND PATTERN.

RECOMMENDED LAND PATTERN



REV	DESCRIPTION	DATE	APPROVED
00	INITIAL RELEASE	10/5/12	KS
01	UPDATE PACKAGE DRWING	8/12/14	JHUA

# IDT Ordering Information



---

## Revision History

Date	Originator	Description of Change
10/17/14	B. Chandhoke	Initial release.
12/10/14	B. Chandhoke	1. Added 7 x 5 x 1.3mm JU6 package option and package dimension/landing pattern drawings. 2. Updated ordering information table/graphic to show JU6 package option.
10/28/16	P. Jenkins	Update ordering information decoder tables by separating them into Scheme 1 and Scheme 2; add note to distinguish the two tables.
06/13/17	L.S.	Removed "Ordering Information Scheme #1 (for reference only)". Replaced with a single ordering information table.
06/20/17	L.S.	Corrected frequency errors in Ordering Information table.



**Corporate Headquarters**  
6024 Silver Creek Valley Road  
San Jose, CA 95138 USA  
[www.IDT.com](http://www.IDT.com)

**Sales**  
1-800-345-7015 or 408-284-8200  
Fax: 408-284-2775  
[www.IDT.com/go/sales](http://www.IDT.com/go/sales)

**Tech Support**  
[www.IDT.com/go/support](http://www.IDT.com/go/support)

DISCLAIMER Integrated Device Technology, Inc. (IDT) and its affiliated companies (herein referred to as "IDT") reserve the right to modify the products and/or specifications described herein at any time, without notice, at IDT's sole discretion. Performance specifications and operating parameters of the described products are determined in an independent state and are not guaranteed to perform the same way when installed in customer products. The information contained herein is provided without representation or warranty of any kind, whether express or implied, including, but not limited to, the suitability of IDT's products for any particular purpose, an implied warranty of merchantability, or non-infringement of the intellectual property rights of others. This document is presented only as a guide and does not convey any license under intellectual property rights of IDT or any third parties.

IDT's products are not intended for use in applications involving extreme environmental conditions or in life support systems or similar devices where the failure or malfunction of an IDT product can be reasonably expected to significantly affect the health or safety of users. Anyone using an IDT product in such a manner does so at their own risk, absent an express, written agreement by IDT.

Integrated Device Technology, IDT and the IDT logo are trademarks or registered trademarks of IDT and its subsidiaries in the United States and other countries. Other trademarks used herein are the property of IDT or their respective third party owners. For datasheet type definitions and a glossary of common terms, visit [www.idt.com/go/glossary](http://www.idt.com/go/glossary). Integrated Device Technology, Inc.. All rights reserved.

## X-ON Electronics

Largest Supplier of Electrical and Electronic Components

*Click to view similar products for [Standard Clock Oscillators](#) category:*

*Click to view products by [IDT](#) manufacturer:*

Other Similar products are found below :

[EP1400SJTSC-125.000M](#) [601137](#) [601252](#) [CSX750FBC-24.000M-UT](#) [CSX750FBC-33.333M-UT](#) [CSX750FCC-3.6864M-UT](#) [F335-12](#) [F335-25](#) [DSC506-03FM2](#) [ASA-20.000MHZ-L-T](#) [ASA-25.000MHZ-L-T](#) [ASA-27.000MHZ-L-T](#) [ASV-20.000MHZ-LR-T](#) [ECS-2018-160-BN-TR](#) [EL13C7-H2F-125.00M](#) [MXO45HS-2C-66.6666MHZ](#) [SiT1602BI-22-33E-50.000000E](#) [SIT8003AC-11-33S-2.04800X](#) [SiT8256AC-23-33E-156.250000X](#) [SIT8918AA-11-33S-50.000000G](#) [SM4420TEV-40.0M-T1K](#) [SMA4306-TL-H](#) [F335-24](#) [F335-40](#) [F335-50](#) [F535L-10](#) [F535L-12](#) [F535L-16](#) [F535L-27](#) [F535L-48](#) [PE7744DW-100.0M](#) [CSX750FBC-20.000M-UT](#) [CSX-750FBC33333000T](#) [CSX750FBC-4.000M-UT](#) [CSX750FBC-7.3728M-UT](#) [CSX750FBC-8.000M-UT](#) [CSX-750FCC14745600T](#) [CSX750FCC-16.000M-UT](#) [CSX-750FCC40000000T](#) [CSX750FCC-4.000M-UT](#) [ASA-22.000MHZ-L-T](#) [ASA2-26.000MHZ-L-T](#) [ASA-40.000MHZ-L-T](#) [ASA-48.000MHZ-L-T](#) [ASA-60.000MHZ-L-T](#) [ASF1-3.686MHZ-N-K-S](#) [XO37CTECNA10M](#) [XO57CRECNA16M](#) [XO57CTECNA3M6864](#) [XO57CTECNA4M9152](#)