

AOD4186
N-Channel Enhancement Mode Field Effect Transistor
General Description

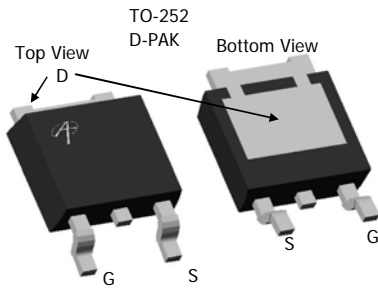
The AOD4186 combines advanced trench MOSFET technology with a low resistance package to provide extremely low $R_{DS(ON)}$. This device is ideal for low voltage inverter applications.

- RoHS Compliant
- Halogen Free

Features

V_{DS} (V) =40V
 I_D = 35A (V_{GS} = 10V)
 $R_{DS(ON)}$ < 15m Ω (V_{GS} = 10V)
 $R_{DS(ON)}$ < 19m Ω (V_{GS} = 4.5V)

100% UIS Tested!
100% R_g Tested!


Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	40	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^G	$T_C=25^\circ\text{C}$	35	A
	$T_C=100^\circ\text{C}$	27	
Pulsed Drain Current ^C	I_{DM}	70	
Continuous Drain Current	$T_A=25^\circ\text{C}$	10	A
	$T_A=70^\circ\text{C}$	8	
Avalanche Current ^C	I_{AR}	24	A
Repetitive avalanche energy $L=0.1\text{mH}$ ^C	E_{AR}	29	mJ
Power Dissipation ^B	$T_C=25^\circ\text{C}$	50	W
	$T_C=100^\circ\text{C}$	25	
Power Dissipation ^A	$T_A=25^\circ\text{C}$	2.5	W
	$T_A=70^\circ\text{C}$	1.6	
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 175	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	$t \leq 10\text{s}$	16.7	$^\circ\text{C/W}$
Maximum Junction-to-Ambient ^{A D}		Steady-State	40	$^\circ\text{C/W}$
Maximum Junction-to-Case	$R_{\theta JC}$	2.5	3	$^\circ\text{C/W}$

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	40			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =40V, V _{GS} =0V T _J =55°C			1 5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	1.7	2.2	2.7	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	100			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =20A T _J =125°C		12.4 20	15 24	mΩ
		V _{GS} =4.5V, I _D =15A		14.5	19	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =20A		60		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.75	1	V
I _S	Maximum Body-Diode Continuous Current				60	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =20V, f=1MHz	780	980	1200	pF
C _{oss}	Output Capacitance		90	130	170	pF
C _{riss}	Reverse Transfer Capacitance		48	80	110	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	1.9	3.8	5.7	Ω
SWITCHING PARAMETERS						
Q _g (10V)	Total Gate Charge	V _{GS} =10V, V _{DS} =20V, I _D =20A	13.5	17	20	nC
Q _g (4.5V)	Total Gate Charge		7	9	11	nC
Q _{gs}	Gate Source Charge		2	2.5	3	nC
Q _{gd}	Gate Drain Charge		2.7	4.5	6.3	nC
t _{D(on)}	Turn-On Delay Time	V _{GS} =10V, V _{DS} =20V, R _L =1.0Ω, R _{GEN} =3Ω		6		ns
t _r	Turn-On Rise Time			12		ns
t _{D(off)}	Turn-Off Delay Time			26		ns
t _f	Turn-Off Fall Time			7		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =20A, dI/dt=500A/μs	9	12	15	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =20A, dI/dt=500A/μs	24	31	38	nC

A. The value of R_{θJA} is measured with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The Power dissipation P_{DSM} is based on R_{θJA} and the maximum allowed junction temperature of 150°C. The value in any given application depends on the user's specific board design, and the maximum temperature of 175°C may be used if the PCB allows it.

B. The power dissipation P_D is based on T_{J(MAX)}=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=175°C. Ratings are based on low frequency and duty cycles to keep initial T_J=25°C.

D. The R_{θJA} is the sum of the thermal impedance from junction to case R_{θJC} and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <30Q_s pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of T_{J(MAX)}=175°C. The SOA curve provides a single pulse rating.

G. The maximum current rating is limited by bond-wires.

H. These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

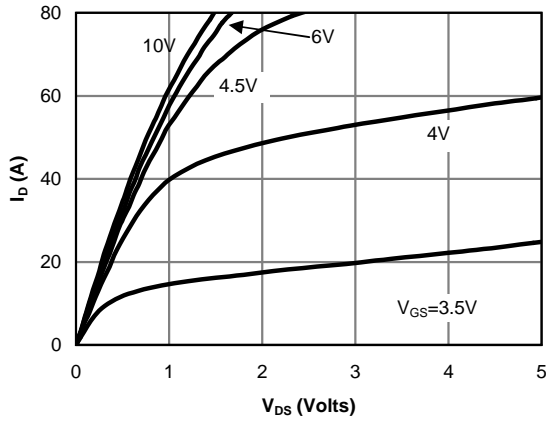


Fig 1: On-Region Characteristics (Note E)

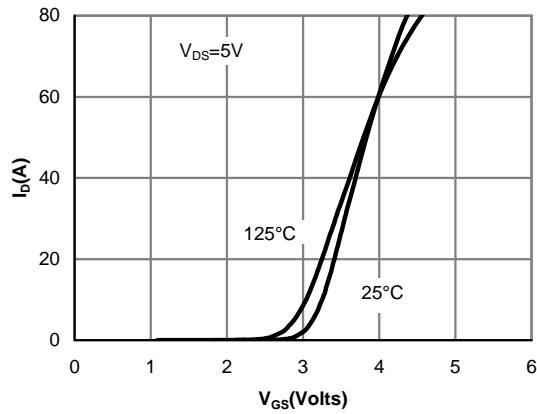


Figure 2: Transfer Characteristics (Note E)

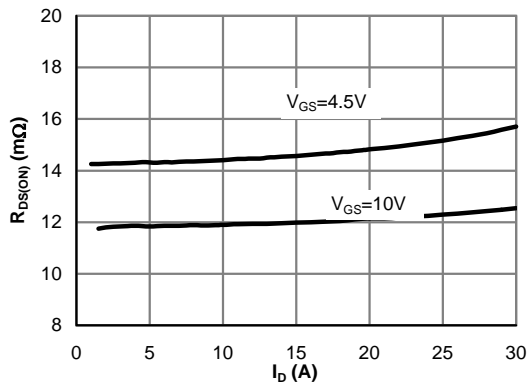


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

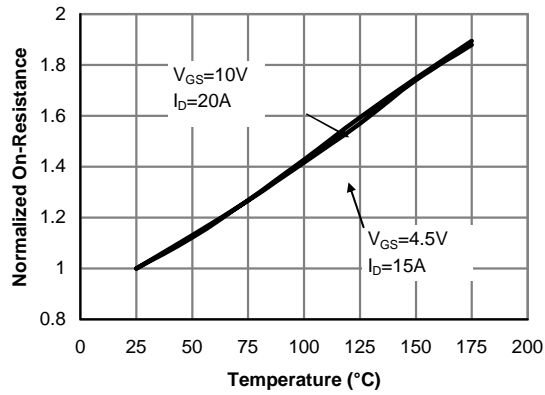


Figure 4: On-Resistance vs. Junction Temperature (Note E)

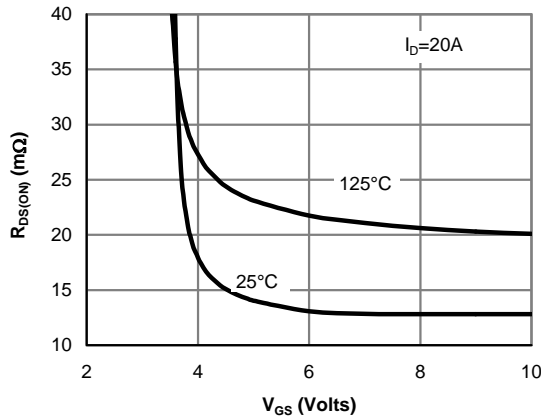


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

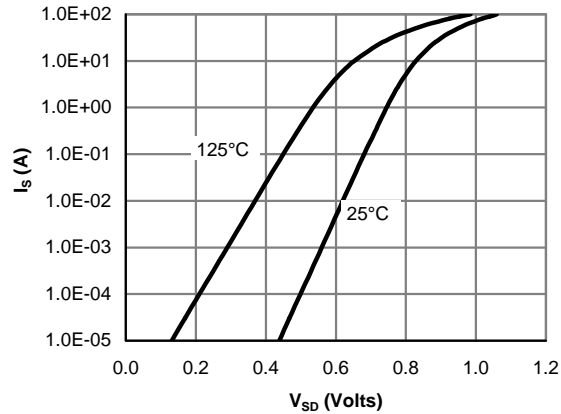


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

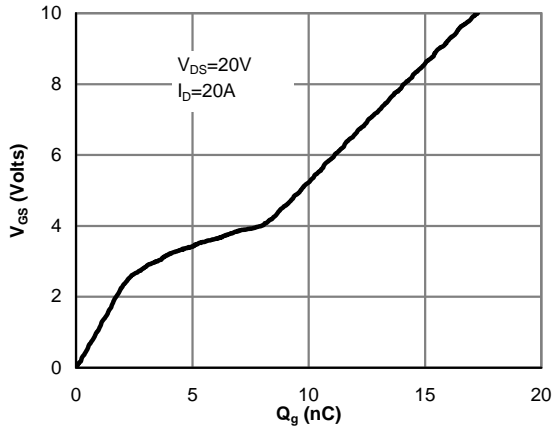


Figure 7: Gate-Charge Characteristics

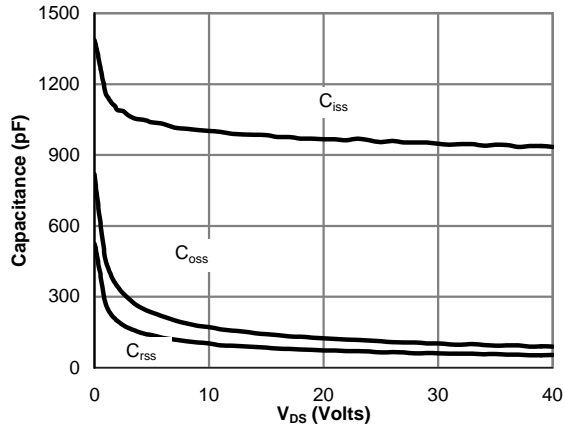


Figure 8: Capacitance Characteristics

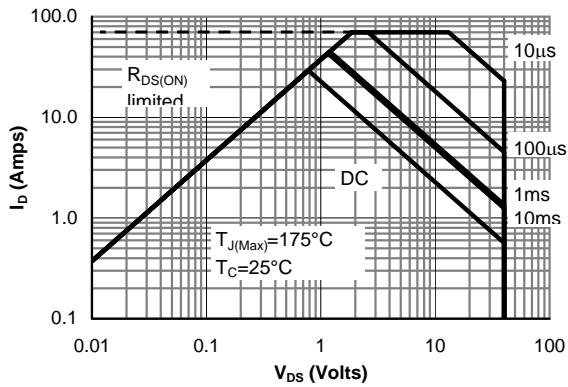


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

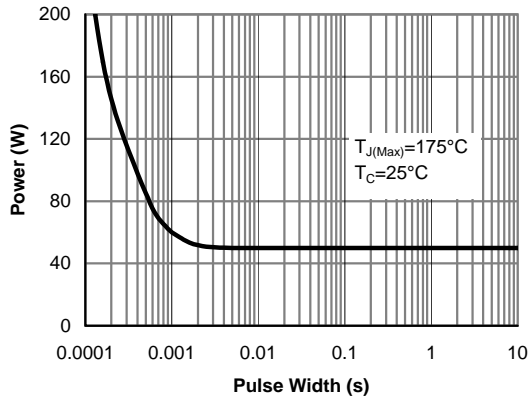


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

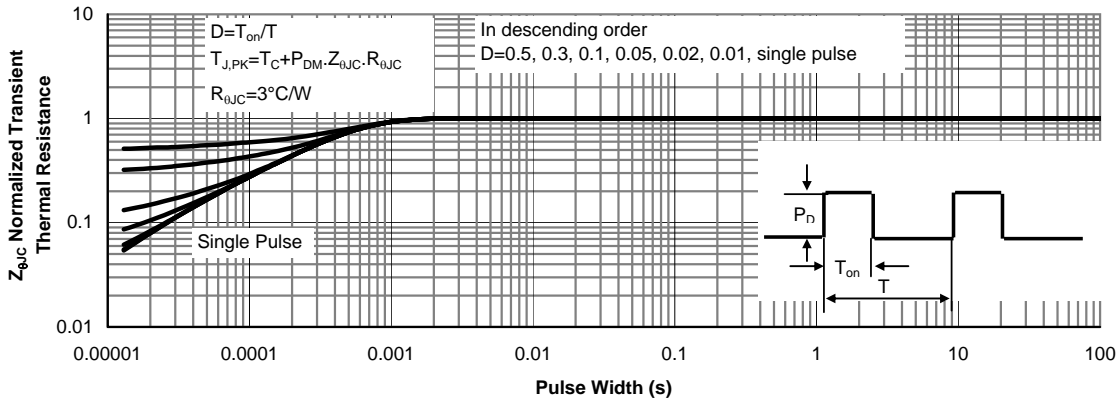


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

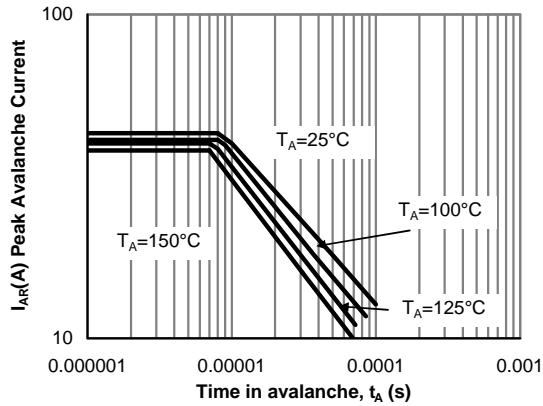


Figure 12: Single Pulse Avalanche capability (Note C)

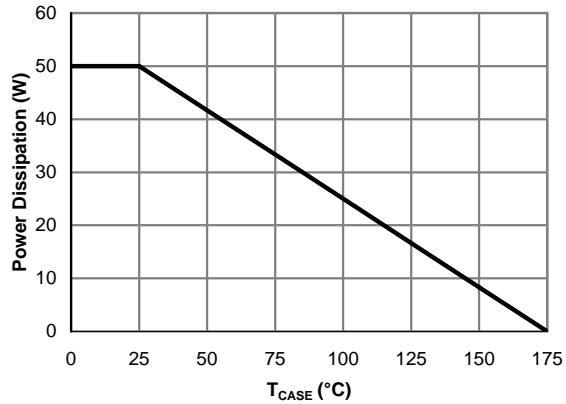


Figure 13: Power De-rating (Note F)

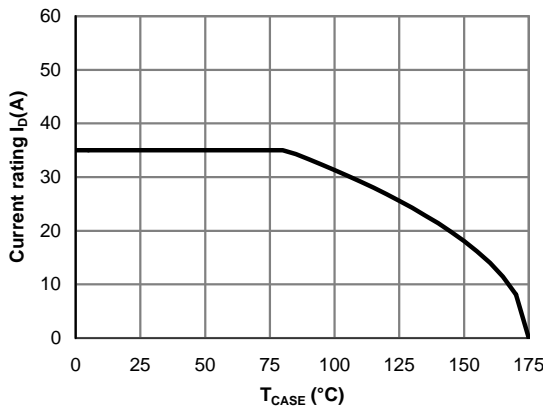


Figure 14: Current De-rating (Note F)

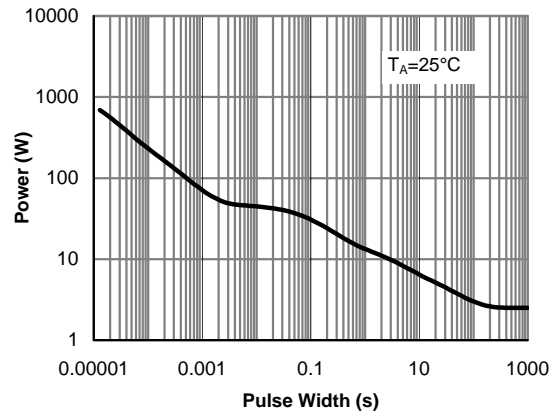


Figure 15: Single Pulse Power Rating Junction-to-Ambient (Note H)

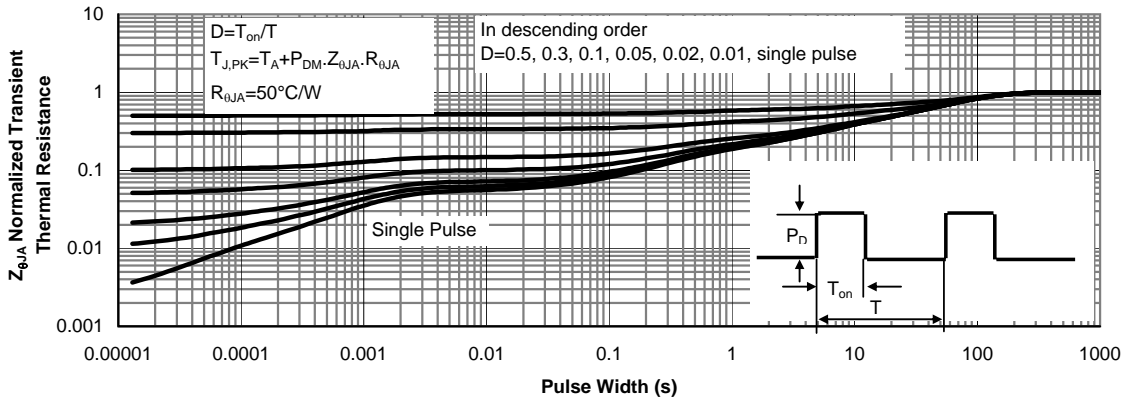
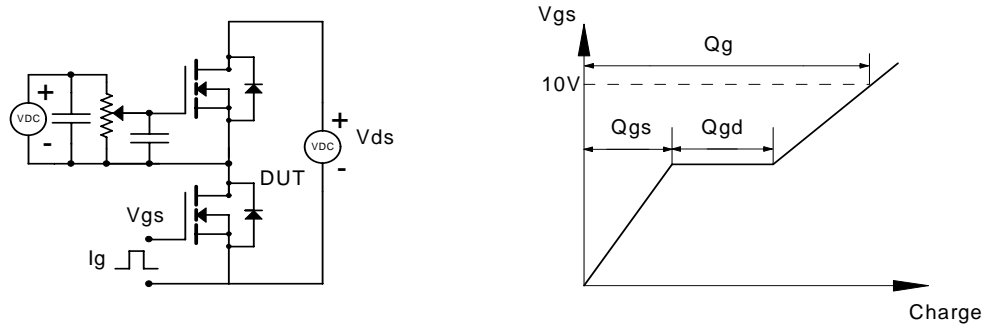
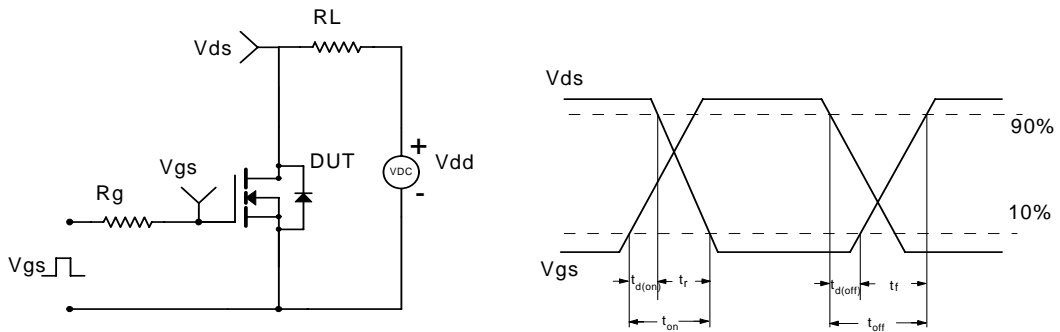


Figure 16: Normalized Maximum Transient Thermal Impedance (Note H)

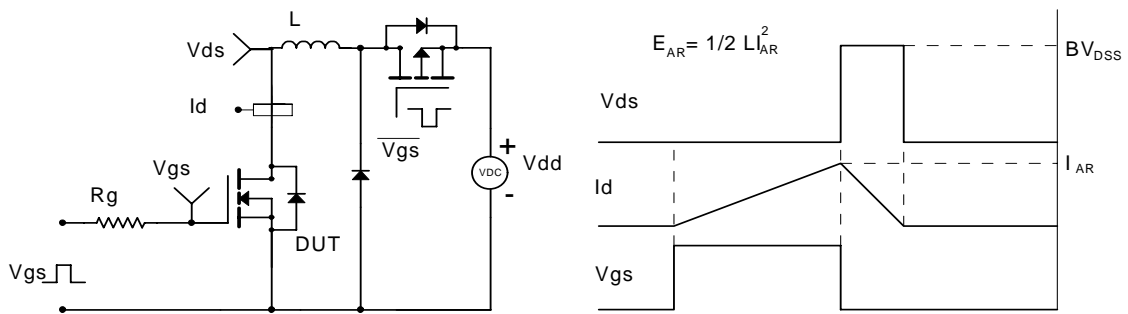
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

