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Team Nexperia



PSMN2R0-30BL

N-channel 30 V 2.1 m Ω logic level MOSFET in D2PAK

Rev. 1 — 20 March 2012

Product data sheet

1. Product profile

1.1 General description

Logic level N-channel MOSFET in D2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

1.2 Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for logic level gate drive sources

1.3 Applications

- DC-to-DC converters
- Motor control
- Load switching
- Server power supplies

1.4 Quick reference data

Table 1. Quick reference data

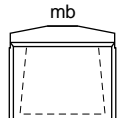
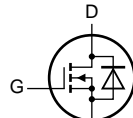
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|--|---|-----|------|-----|------------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | - | 30 | V |
| I_D | drain current | $T_{mb} = 25\text{ °C}; V_{GS} = 10\text{ V}$; see Figure 1 [1] | - | - | 100 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | - | 211 | W |
| T_j | junction temperature | | -55 | - | 175 | °C |
| Static characteristics | | | | | | |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 100\text{ °C}$; see Figure 12 ; see Figure 11 | - | 2.51 | 2.9 | m Ω |
| | | $V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 25\text{ °C}$; see Figure 11 | - | 1.79 | 2.1 | m Ω |
| Dynamic characteristics | | | | | | |
| Q_{GD} | gate-drain charge | $V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}; V_{DS} = 15\text{ V}$; see Figure 13 ; see Figure 14 | - | 16 | - | nC |
| $Q_{G(tot)}$ | total gate charge | | - | 55 | - | nC |
| Avalanche ruggedness | | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(init)} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped | - | - | 555 | mJ |

[1] Continuous current is limited by package.



2. Pinning information

Table 2. Pinning information

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|-----|--------|-----------------------------------|---|---|
| 1 | G | gate |  |  |
| 2 | D | drain ^[1] | | |
| 3 | S | source | | |
| mb | D | mounting base; connected to drain | | |

SOT404 (D2PAK)

[1] It is not possible to make connection to pin 2

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|--------------|---------|--|---------|
| | Name | Description | Version |
| PSMN2R0-30BL | D2PAK | plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped) | SOT404 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|--------------|--------------|
| PSMN2R0-30BL | PSMN2R0-30BL |

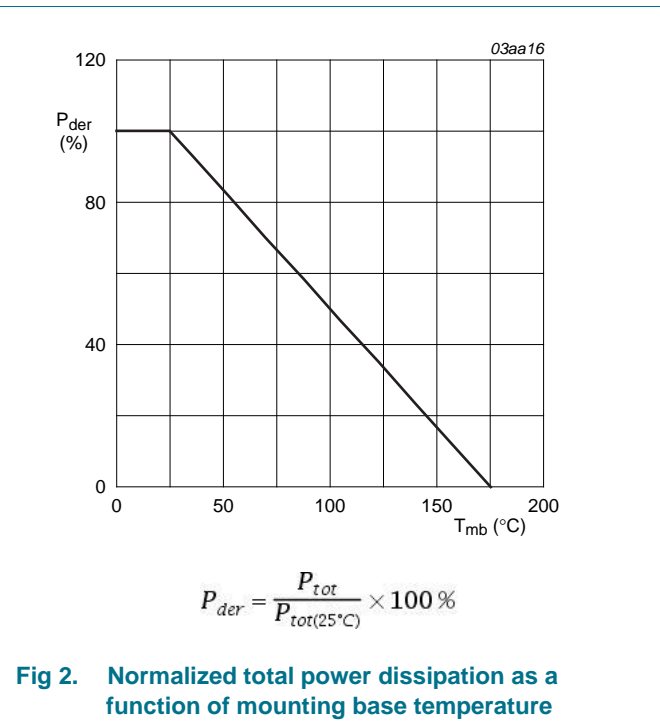
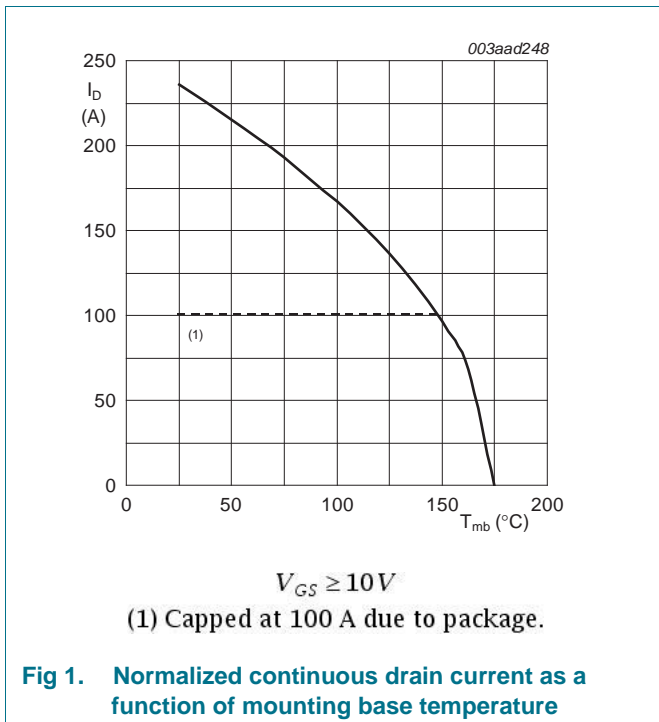
5. Limiting values

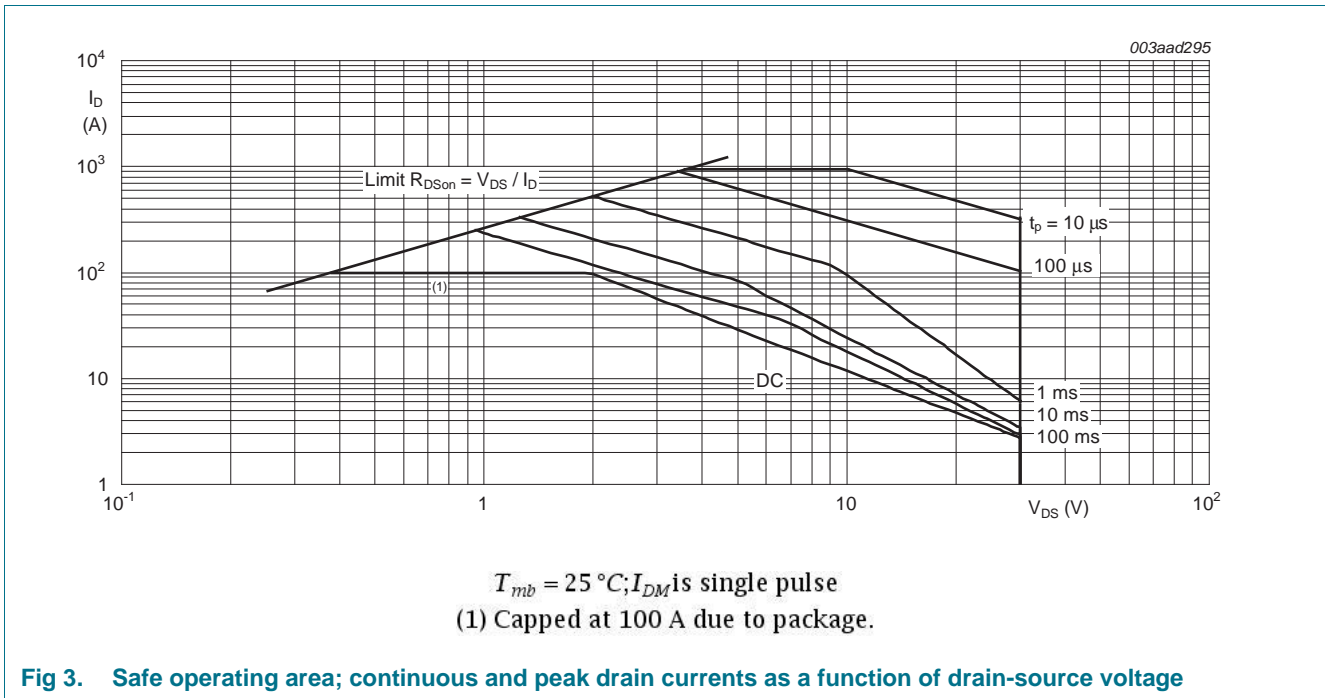
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------------------------|--|--|-----|-----|------|
| V_{DS} | drain-source voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}$ | - | 30 | V |
| V_{DGR} | drain-gate voltage | $T_j \geq 25\text{ °C}; T_j \leq 175\text{ °C}; R_{GS} = 20\text{ k}\Omega$ | - | 30 | V |
| V_{GS} | gate-source voltage | | -20 | 20 | V |
| I_D | drain current | $V_{GS} = 10\text{ V}; T_{mb} = 100\text{ °C}$; see Figure 1 | [1] | 100 | A |
| | | $V_{GS} = 10\text{ V}; T_{mb} = 25\text{ °C}$; see Figure 1 | [1] | 100 | A |
| I_{DM} | peak drain current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$; see Figure 3 | - | 943 | A |
| P_{tot} | total power dissipation | $T_{mb} = 25\text{ °C}$; see Figure 2 | - | 211 | W |
| T_{stg} | storage temperature | | -55 | 175 | °C |
| T_j | junction temperature | | -55 | 175 | °C |
| $T_{slid(M)}$ | peak soldering temperature | | - | 260 | °C |
| Source-drain diode | | | | | |
| I_S | source current | $T_{mb} = 25\text{ °C}$ | [1] | 100 | A |
| I_{SM} | peak source current | pulsed; $t_p \leq 10\text{ }\mu\text{s}$; $T_{mb} = 25\text{ °C}$ | - | 943 | A |
| Avalanche ruggedness | | | | | |
| $E_{DS(AL)S}$ | non-repetitive drain-source avalanche energy | $V_{GS} = 10\text{ V}; T_{j(\text{init})} = 25\text{ °C}; I_D = 100\text{ A}; V_{sup} \leq 30\text{ V}; R_{GS} = 50\text{ }\Omega$; unclamped | - | 555 | mJ |

[1] Continuous current is limited by package.





6. Thermal characteristics

Table 6. Thermal characteristics

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|----------------|---|--|-----|------|------|------|
| $R_{th(j-mb)}$ | thermal resistance from junction to mounting base | see Figure 4 | - | 0.41 | 0.71 | K/W |
| $R_{th(j-a)}$ | thermal resistance from junction to ambient | maximum foot print; mounted on a printed circuit board | - | 50 | - | K/W |

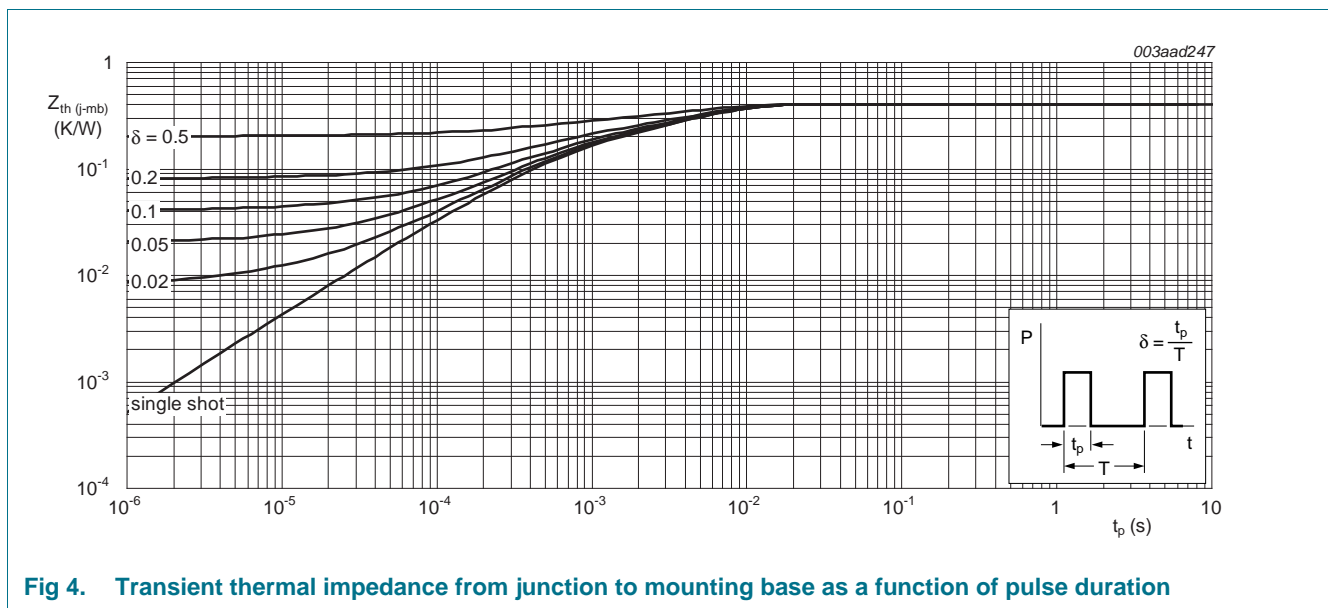


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration

7. Characteristics

Table 7. Characteristics

Tested to JEDEC standards where applicable.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--------------------------------|-----------------------------------|--|-----|------|------|---------|
| Static characteristics | | | | | | |
| $V_{(BR)DSS}$ | drain-source breakdown voltage | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | 30 | - | - | V |
| | | $I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$ | 27 | - | - | V |
| $V_{GS(th)}$ | gate-source threshold voltage | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$; see Figure 9 ; see Figure 10 | 1.3 | 1.7 | 2.15 | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$; see Figure 10 | 0.5 | - | - | V |
| | | $I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$; see Figure 10 | - | - | 2.45 | V |
| I_{DSS} | drain leakage current | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 0.02 | 3 | μA |
| | | $V_{DS} = 30 V; V_{GS} = 0 V; T_j = 125 \text{ }^\circ C$ | - | - | 70 | μA |
| I_{GSS} | gate leakage current | $V_{GS} = 16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| | | $V_{GS} = -16 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$ | - | 10 | 100 | nA |
| $R_{DS(on)}$ | drain-source on-state resistance | $V_{GS} = 4.5 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 11 | - | 2.47 | 2.9 | mΩ |
| | | $V_{GS} = 10 V; I_D = 25 A; T_j = 175 \text{ }^\circ C$; see Figure 12 ; see Figure 11 | - | 3.4 | 4 | mΩ |
| | | $V_{GS} = 10 V; I_D = 25 A; T_j = 100 \text{ }^\circ C$; see Figure 12 ; see Figure 11 | - | 2.51 | 2.9 | mΩ |
| | | $V_{GS} = 10 V; I_D = 25 A; T_j = 25 \text{ }^\circ C$; see Figure 11 | - | 1.79 | 2.1 | mΩ |
| R_G | gate resistance | $f = 1 \text{ MHz}$ | - | 0.78 | - | Ω |
| Dynamic characteristics | | | | | | |
| $Q_{G(tot)}$ | total gate charge | $I_D = 0 A; V_{DS} = 0 V; V_{GS} = 10 V$ | - | 107 | - | nC |
| | | $I_D = 25 A; V_{DS} = 15 V; V_{GS} = 10 V$; see Figure 13 ; see Figure 14 | - | 117 | - | nC |
| | | $I_D = 25 A; V_{DS} = 15 V; V_{GS} = 4.5 V$; see Figure 13 ; see Figure 14 | - | 55 | - | nC |
| Q_{GS} | gate-source charge | | - | 17 | - | nC |
| $Q_{GS(th)}$ | pre-threshold gate-source charge | | - | 11 | - | nC |
| $Q_{GS(th-pl)}$ | post-threshold gate-source charge | | - | 6 | - | nC |
| Q_{GD} | gate-drain charge | | - | 16 | - | nC |
| $V_{GS(pl)}$ | gate-source plateau voltage | $I_D = 25 A; V_{DS} = 25 V$; see Figure 13 ; see Figure 14 | - | 2.6 | - | V |
| C_{iss} | input capacitance | $V_{DS} = 15 V; V_{GS} = 0 V; f = 1 \text{ MHz}$; | - | 6810 | - | pF |
| C_{oss} | output capacitance | $T_j = 25 \text{ }^\circ C$; see Figure 15 | - | 1410 | - | pF |
| C_{riss} | reverse transfer capacitance | | - | 650 | - | pF |
| $t_{d(on)}$ | turn-on delay time | $V_{DS} = 15 V; R_L = 0.5 \text{ } \Omega; V_{GS} = 4.5 V$; | - | 63 | - | ns |
| t_r | rise time | $R_{G(ext)} = 4.7 \text{ } \Omega$ | - | 125 | - | ns |
| $t_{d(off)}$ | turn-off delay time | | - | 111 | - | ns |
| t_f | fall time | | - | 59 | - | ns |

Table 7. Characteristics ...continued
 Tested to JEDEC standards where applicable.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|-----------------------|---|-----|------|-----|------|
| Source-drain diode | | | | | | |
| V_{SD} | source-drain voltage | $I_S = 25\text{ A}$; $V_{GS} = 0\text{ V}$; $T_j = 25\text{ °C}$; see Figure 16 | - | 0.76 | 1.2 | V |
| t_{rr} | reverse recovery time | $I_S = 25\text{ A}$; $di_S/dt = -100\text{ A}/\mu\text{s}$; | - | 49 | - | ns |
| Q_r | recovered charge | $V_{GS} = 0\text{ V}$; $V_{DS} = 15\text{ V}$ | - | 66 | - | nC |

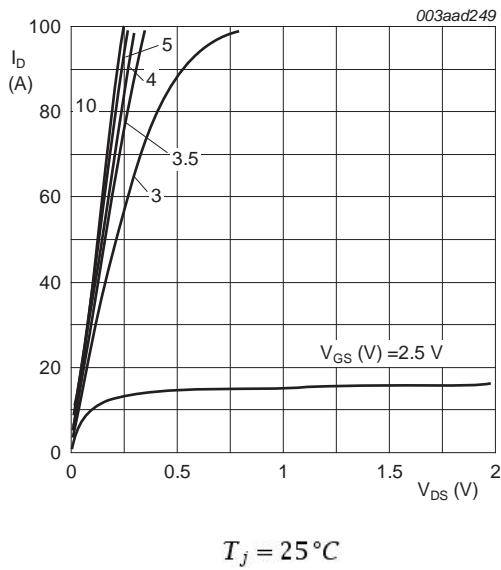


Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values

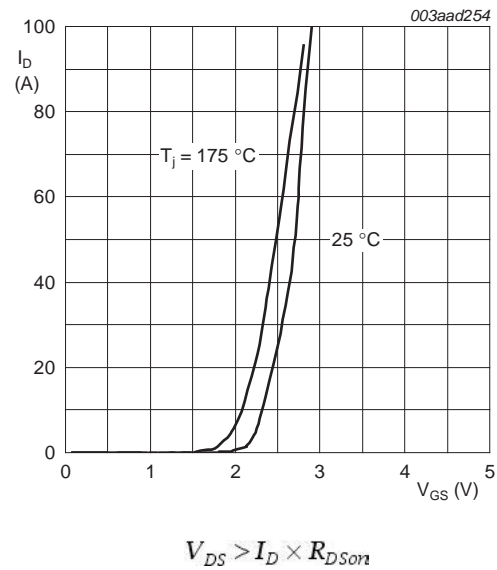


Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values

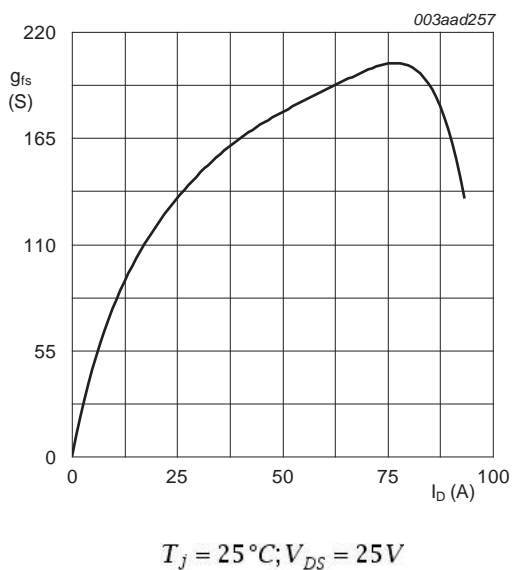


Fig 7. Forward transconductance as a function of drain current; typical values

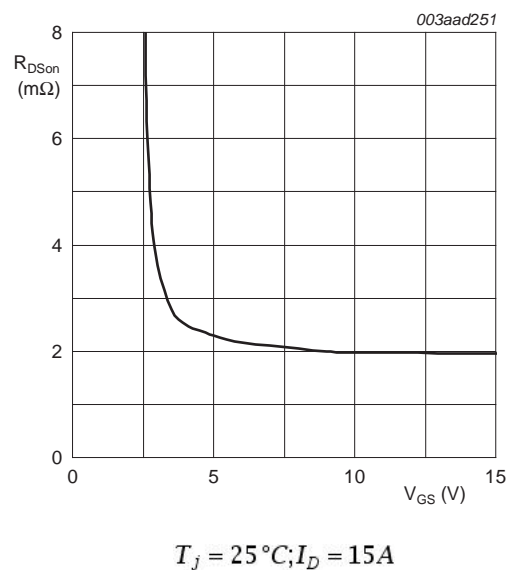
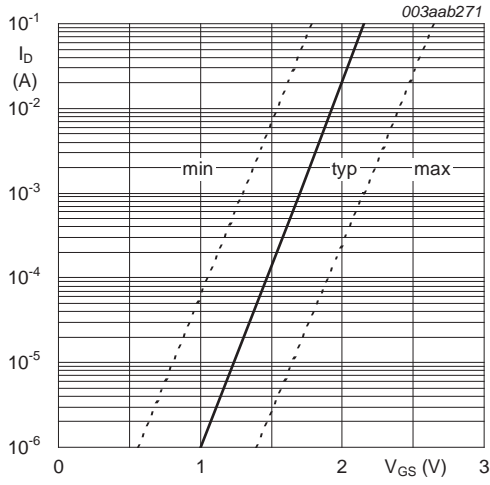
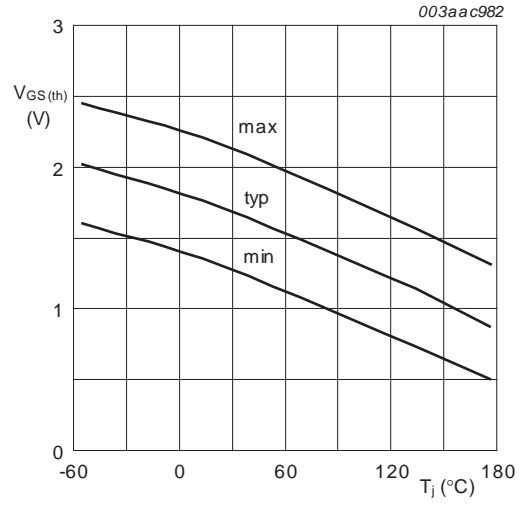


Fig 8. Drain source on-state resistance as a function of gate-source voltage; typical values



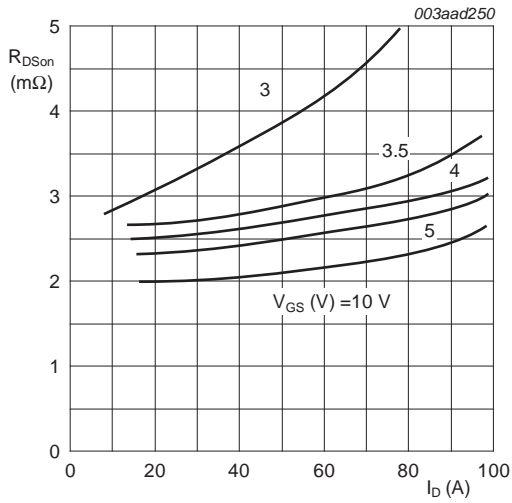
$$T_j = 25^\circ\text{C}; V_{DS} = 5\text{V}$$

Fig 9. Sub-threshold drain current as a function of gate-source voltage



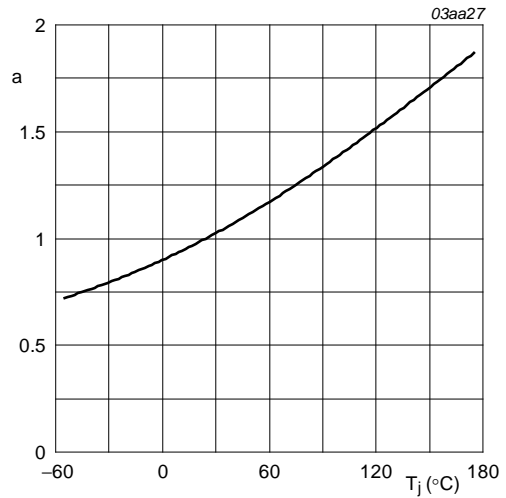
$$I_D = 1\text{mA}; V_{DS} = V_{GS}$$

Fig 10. Gate-source threshold voltage as a function of junction temperature



$$T_j = 25^\circ\text{C}$$

Fig 11. Drain-source on-state resistance as a function of drain current; typical values



$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 12. Normalized drain-source on-state resistance factor as a function of junction temperature

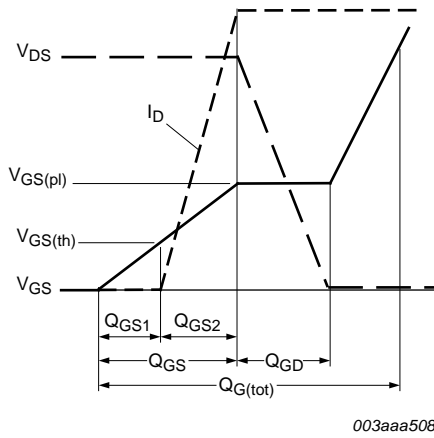
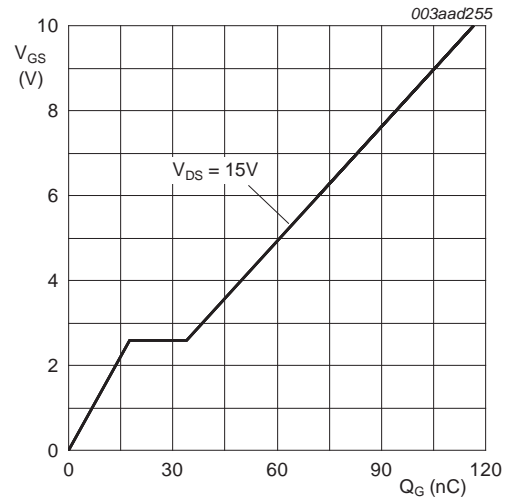
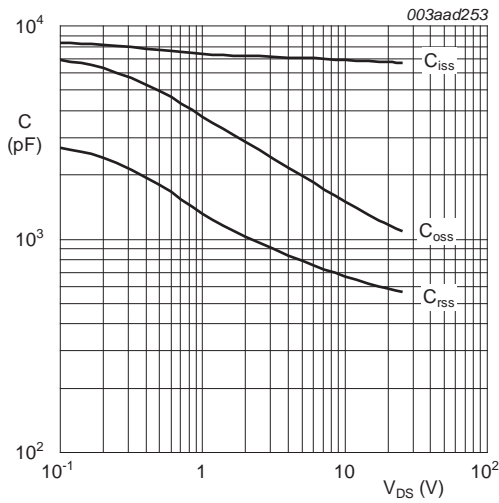


Fig 13. Gate charge waveform definitions



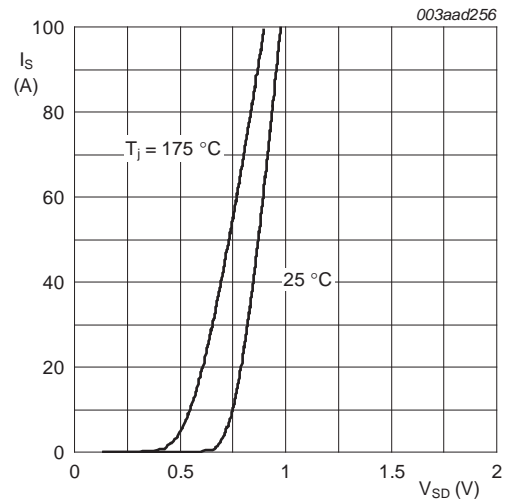
$T_j = 25^\circ C; I_D = 25A$

Fig 14. Gate-source voltage as a function of gate charge; typical values



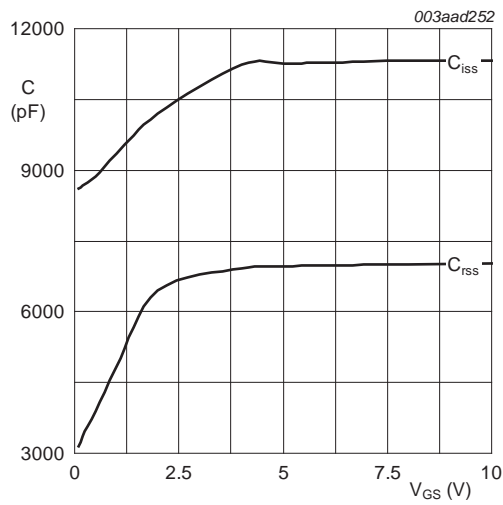
$V_{GS} = 0V; f = 1MHz$

Fig 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$V_{GS} = 0V$

Fig 16. Source current as a function of source-drain voltage; typical values



$V_{DS} = 0V; f = 1MHz$

Fig 17. Input and reverse transfer capacitances as a function of gate-source voltage; typical values

8. Package outline

Plastic single-ended surface-mounted package (D2PAK); 3 leads (one lead cropped)

SOT404

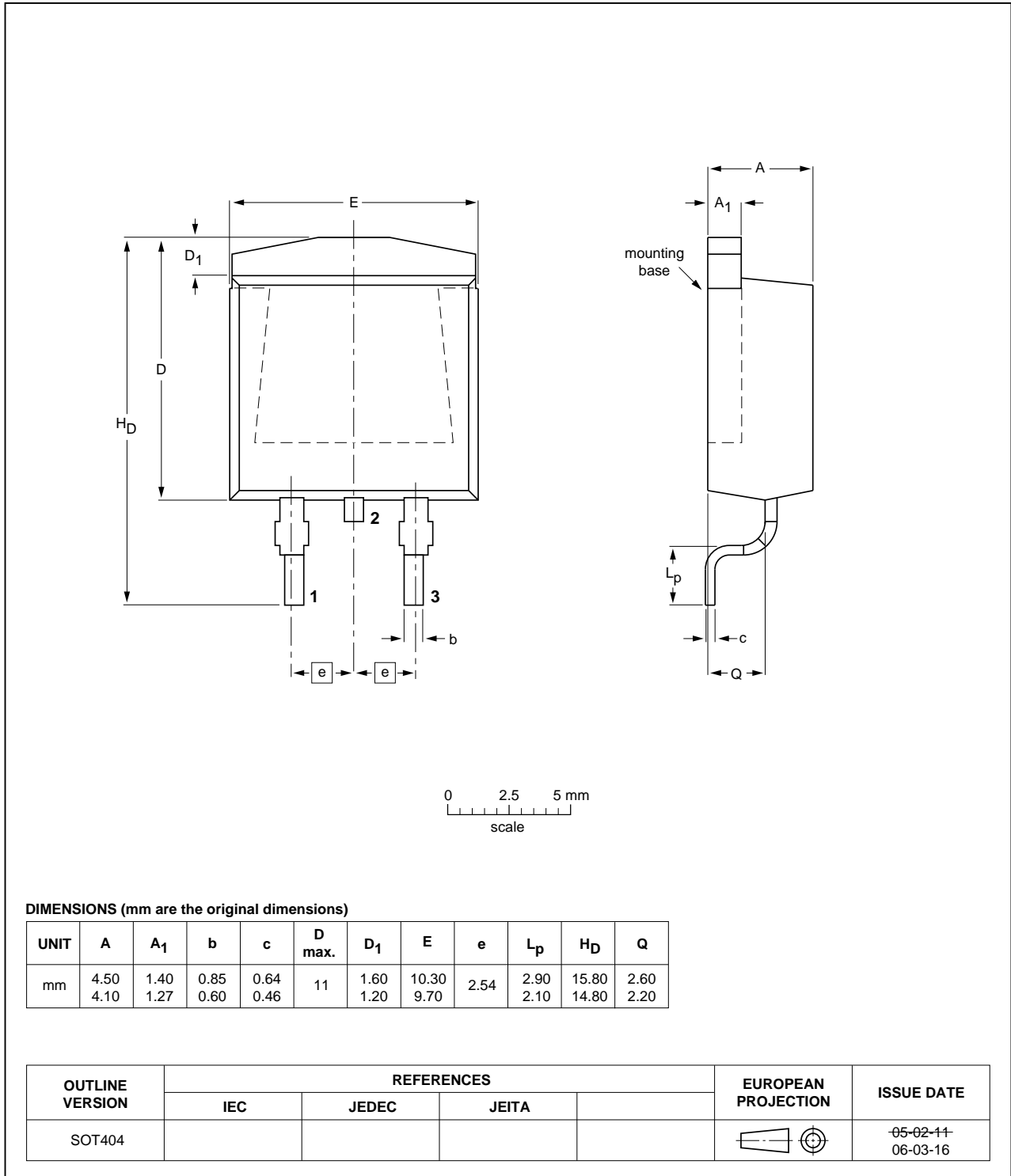


Fig 18. Package outline SOT404 (D2PAK)

9. Revision history

Table 8. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--------------|--------------------|---------------|------------|
| PSMN2R0-30BL v.1 | 20120320 | Product data sheet | - | - |

10. Legal information

10.1 Data sheet status

| Document status ^[1] [2] | Product status ^[3] | Definition |
|------------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
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12. Contents

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