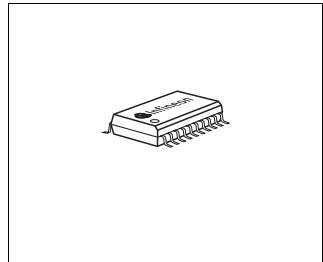
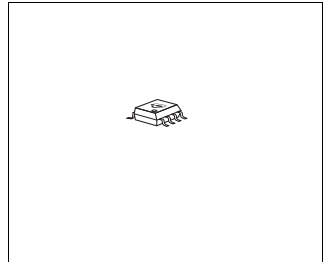




## Features

- Output voltage tolerance  $\leq \pm 2\%$
- Very low current consumption
- Low-drop voltage
- Watchdog
- Settable reset threshold
- Overtemperature protection
- Reverse polarity protection
- Short-circuit proof
- Suitable for use in automotive electronics
- Wide temperature range
- Green Product (RoHS compliant)
- AEC Qualified



## Functional Description

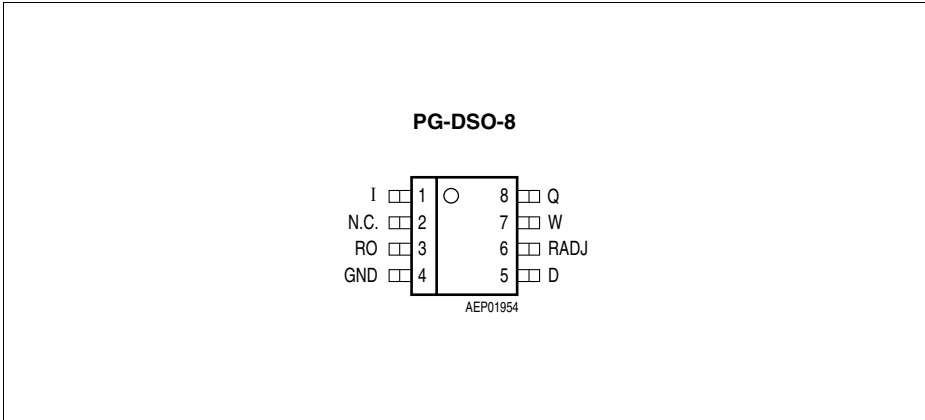
This device is a 5-V low-drop fixed-voltage regulator. The maximum input voltage is 45 V. It can deliver an output current of at least 180 mA. The IC is short-circuit proof and features temperature protection that disables the circuit in the event of impermissibly high temperatures. The watchdog function is disabled as a function of the load, so that a controller is not interrupted during sleep mode by a watchdog reset.

## Application Description

The IC regulates an input voltage  $V_I$  in the range  $5.5\text{ V} < V_I < 45\text{ V}$  to  $V_{Q,nom} = 5.0\text{ V}$ . In the event of an output voltage  $V_Q < V_{RT}$ , a reset signal is generated. The wiring of the reset switching threshold input enables the value of  $V_{RT}$  to be reduced. The reset delay time can be adjusted using an external capacitor. The integrated watchdog monitors the connected active controller. If there is no rising edge at the watchdog input, the reset

Type	Package
TLE 4268 GS	PG-DSO-8
TLE 4268 G	PG-DSO-20

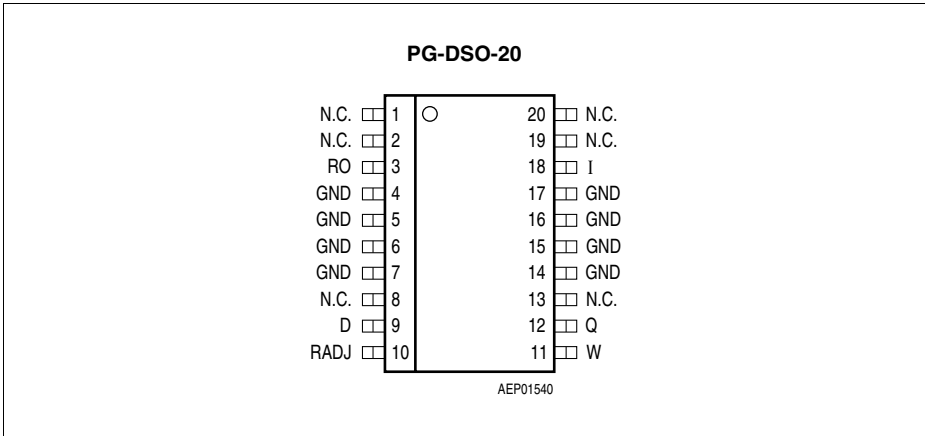
output is set to low. The reset delay capacitor provides a wide adjustment range for the pulse repetition time. The watchdog function is only activated if the load exceeds 8 mA. This ensures that a microcontroller is not activated during power-down and the current drain is not increased. The IC is protected against overload and overtemperature.



**Figure 1** Pin Configuration (top view)

**Table 1** Pin Definitions and Functions

Pin	Symbol	Function
1	I	Input voltage
2	N.C.	Not connected
3	RO	Reset output
4	GND	Ground
5	D	Reset delay
6	RADJ	Reset switching threshold
7	W	Watchdog input
8	Q	5 V output voltage



**Figure 2** Pin Configuration (top view)

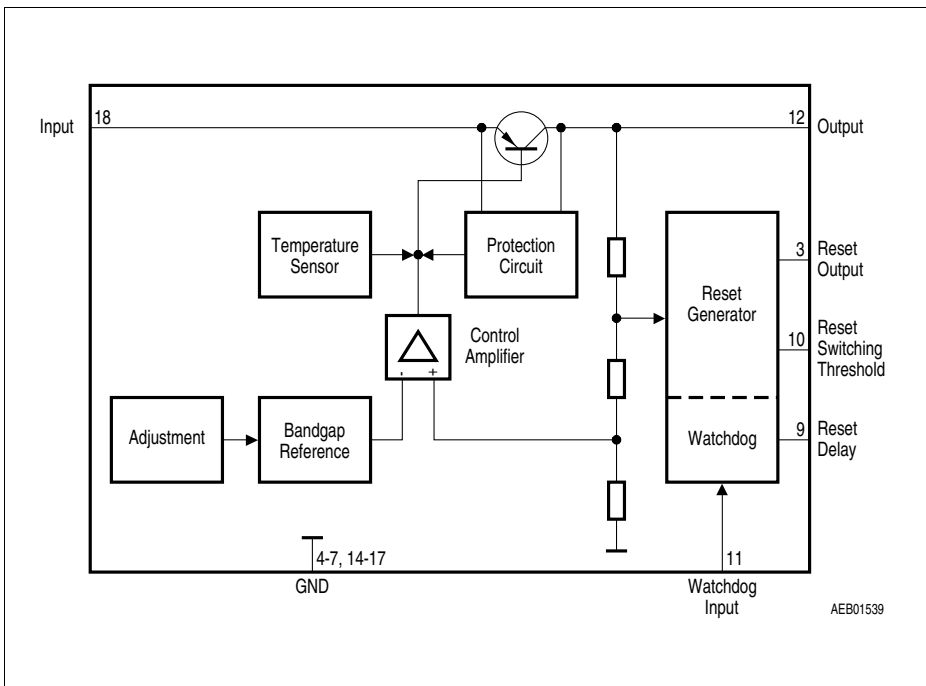
**Table 2** Pin Definitions and Functions

Pin	Symbol	Function
1, 2, 8, 13, 19, 20	N.C.	Not connected.
3	RO	<b>Reset output</b> ; the open collector output is connected to the 5-V output via an integrated resistor of 30 k $\Omega$ .
4 ... 7, 14 ... 17	GND	<b>Ground</b>
9	D	<b>Reset delay</b> ; connect a capacitor to ground for delay time adjustment.
10	RADJ	<b>Reset switching threshold</b> ; for setting the switching threshold, output to ground with voltage divider. If this input is connected to ground, the reset is triggered at an output voltage of 4.5 V.
11	W	<b>Watchdog input</b> ; positive-edge-triggered input for monitoring a microcontroller.
12	Q	<b>5-V output voltage</b> ; block to ground with 22 $\mu$ F capacitor, ESR < 3 $\Omega$ .
18	I	<b>Input voltage</b> ; block to ground directly on the IC with ceramic capacitor.

### Circuit Description

The control amplifier compares a reference voltage, which is kept highly accurate by resistance adjustment, to a voltage that is proportional to the output voltage and drives the base of the series transistor via a buffer. Saturation control as a function of the load current prevents any over-saturation of the power element. If the externally scaled down output voltage at the reset threshold input drops below 1.35 V, the external reset delay capacitor is discharged by the reset generator. If the voltage on the capacitor reaches the lower threshold  $V_{DRL}$ , a reset signal is generated on the reset output and not cancelled again until the upper threshold voltage is exceeded. If the reset threshold input is connected to GND, reset is triggered at an output voltage of 4.5 V. A connected microcontroller is monitored by the watchdog logic. If pulses are missing, the rest output is set to low. The pulse sequence time can be set within a wide range with the reset delay capacitor. The IC also incorporates internal circuits for protection against:

- Overload
- Overtemperature
- Reverse polarity



**Figure 3** Block Diagram TLE 4268 G (PG-DSO-20)

**Table 3 Absolute Maximum Ratings**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
<b>Input I</b>					
Input voltage	$V_I$	-30	45	V	–
Input current	$I_I$	–	–	–	Internally limited
<b>Reset Output RO</b>					
Voltage	$V_R$	-0.3	7	V	–
Current	$I_R$	–	–	–	Internally limited
<b>Reset Delay D</b>					
Voltage	$V_D$	-0.3	7	V	–
Current	$I_D$	–	–	–	Internally limited
<b>Watchdog W</b>					
Watchdog input	$V_W$	-0.3	7	V	–
<b>Reset Switching Threshold RADJ</b>					
Reset threshold	$V_{RADJ}$	-0.3	7	V	–
<b>Output Q</b>					
Output voltage	$V_Q$	-0.3	7	V	–
Output current	$I_Q$	–	–	–	Internally limited
<b>Ground GND</b>					
Current	$I_{GND}$	-100	50	mA	–
<b>Temperatures</b>					
Junction temperature	$T_j$	-40	150	°C	–
Storage temperature	$T_S$	-50	150	°C	–

**Table 4 Operating Range**

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	Max.		
Input voltage	$V_I$	–	45	V	–
Junction temperature	$T_j$	-40	150	°C	–

**Thermal Resistance**

Junction ambient (soldered)	$R_{thj-a}$	–	185	K/W	PG-DSO-8 <sup>1)</sup>
	$R_{thj-a}$	–	100	K/W	PG-DSO-20 <sup>1)</sup>
Junction pin	$R_{thj-pin}$	–	72	K/W	PG-DSO-8 <sup>2)</sup>
	$R_{thj-pin}$	–	23	K/W	PG-DSO-20 <sup>3)</sup>

1) Package mounted on PCB 80 × 80 × 1.5 mm<sup>3</sup>; 35μ Cu; 5μ Sn; Footprint only; zero airflow.

2) Measured to pin 2.

3) Measured to pin 5.

Optimum reliability and life time are guaranteed if the junction temperature does not exceed 125 °C in operating mode. Operation at up to the maximum junction temperature of 150 °C is possible in principle. Note, however, operation at the maximum permitted ratings could affect the reliability of the device.

**Table 5 Characteristics**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
Output voltage	$V_Q$	4.90	5.00	5.10	V	$5 \text{ mA} \leq I_Q \leq 150 \text{ mA};$ $6 \text{ V} \leq V_I \leq 28 \text{ V}$
Output current limiting	$I_Q$	180	250	–	mA	–
Current consumption $I_q = I_I - I_Q$	$I_q$	–	300	450	$\mu\text{A}$	$I_Q = 0 \text{ mA}$
Current consumption $I_q = I_I - I_Q$	$I_q$	–	13	20	mA	$I_Q = 150 \text{ mA}$
Drop voltage	$V_{DR}$	–	0.25	0.50	V	$I_Q = 150 \text{ mA}^{(1)}$
Load regulation	$\Delta V_{Q,Lo}$	–	10	30	mV	$I_Q = 5 \text{ to } 150 \text{ mA}$
Line regulation	$\Delta V_{Q,Li}$	–	10	30	mV	$V_I = 6 \text{ to } 28 \text{ V}$ $I_Q = 150 \text{ mA}$

**Reset Generator**

Reset threshold	$V_{Q,rt}$	4.2	4.5	4.8	V	–
Reset adjust threshold	$V_{RADJ}$	1.28	1.35	1.45	V	–
Reset low voltage	$V_{RO,l}$	–	0.2	0.5	V	1 mA external
Saturation voltage	$V_D$	–	30	100	mV	$V_Q < V_{RT}$
Charging current	$I_{D,c}$	5	12	18	$\mu\text{A}$	$V_D = 1.0 \text{ V}$
Upper reset timing threshold	$V_{DU}$	1.4	1.8	2.2	V	–
Reset delay time	$t_{rd}$	10	15	25	ms	$C_D = 100 \text{ nF}$
Reset reaction time	$t_{rr}$	–	2	–	$\mu\text{s}$	$C_D = 100 \text{ nF}$
Pull-up	$R_{RO}$	18	30	46	k $\Omega$	with resp. to $V_Q$
Lower reset timing threshold	$V_{DRL}$	0.2	0.4	0.55	V	–

**Table 5 Characteristics (cont'd)**
 $V_I = 13.5 \text{ V}; -40 \text{ }^\circ\text{C} \leq T_j \leq 125 \text{ }^\circ\text{C}$  (unless otherwise specified)

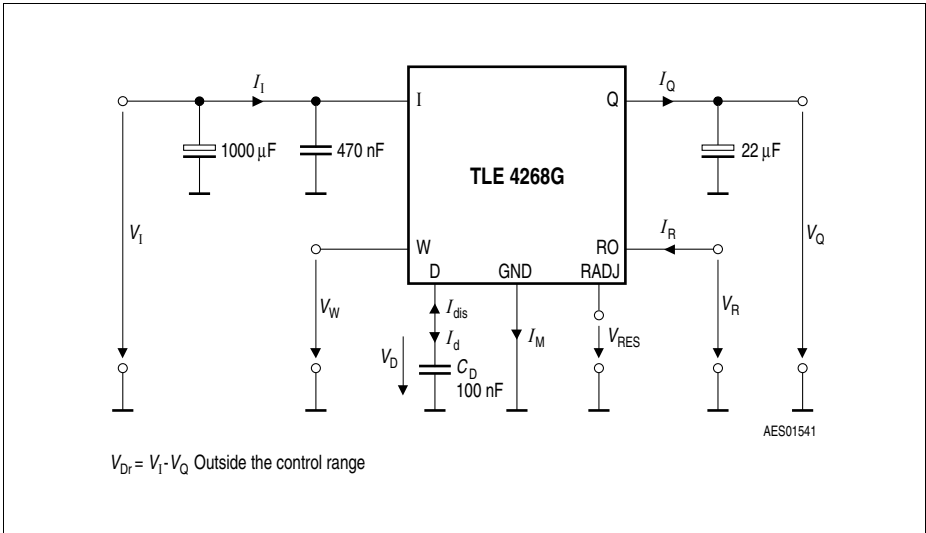
Parameter	Symbol	Limit Values			Unit	Test Condition
		Min.	Typ.	Max.		
<b>Watchdog</b>						
Discharge current	$I_{D,d}$	1.5	3.5	5.2	$\mu\text{A}$	$V_D = 1.0 \text{ V}$
Charging current	$I_{D,c}$	5	12	18	$\mu\text{A}$	$V_D = 1.0 \text{ V}$
Upper timing threshold	$V_{DU}$	1.4	1.8	2.2	V	–
Lower timing threshold	$V_{DWL}$	0.2	0.4	0.55	V	–
Watchdog period	$T_{WP}$	30	55	75	ms	$C_D = 100 \text{ nF}$
Watchdog trigger time	$T_{WT}$	25	40	60	ms	$C_D = 100 \text{ nF}$
Activating current	$I_Q$	2	8	15	mA	Activates watchdog
Slew rate	$dV_W/dt$	5	–	–	V/ $\mu\text{s}$	from 20% up to 80% $V_Q$ <sup>2)</sup>

1) Drop voltage =  $V_I - V_Q$  (measured when the output voltage has dropped 100 mV from the nominal value obtained at 13.5 V input)

2) Watchdog pulse recognition tested with 10 kHz max. pulse frequency

*Note: The reset output is low in range from  $V_Q = 1 \text{ V}$  to  $V_{Q,rt}$ .*





**Figure 4 Test Circuit**

### Reset Timing

The power-on reset delay time is defined by the charging time of an external capacitor  $C_D$  which can be calculated as follows:

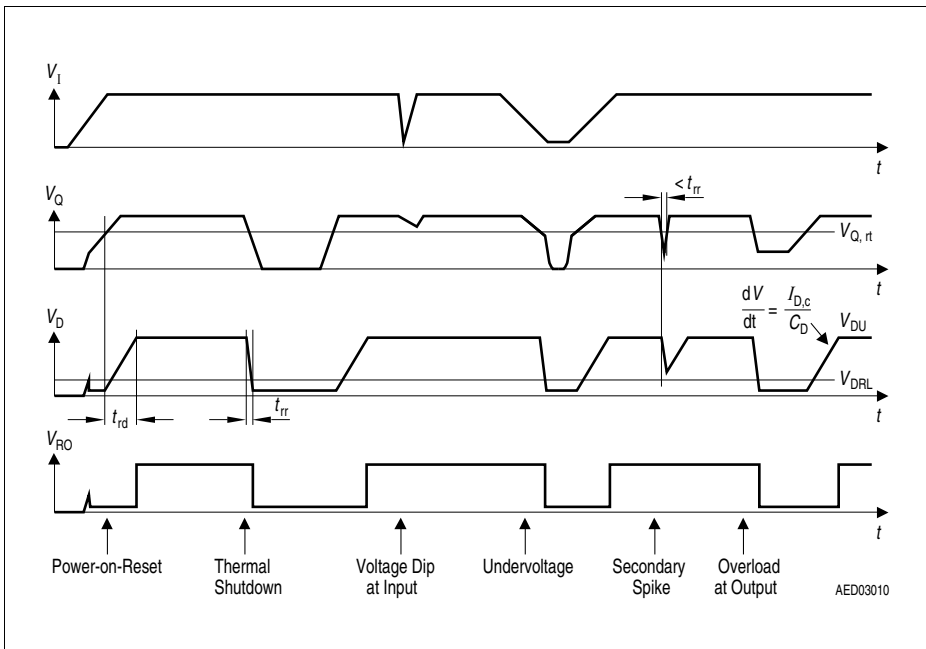
$$C_D = (\Delta t_{rd} \times I_{D,c}) / \Delta V \tag{1}$$

Definitions:

- $C_D$  = delay capacitor
- $\Delta t_{rd}$  = delay time
- $I_{D,c}$  = charge current, typical 12  $\mu$ A
- $\Delta V = V_{DU}$ , typical 1.8 V
- $V_{DU}$  = upper delay switching threshold at  $C_D$  for reset delay time

The reset reaction time  $t_{rr}$  is the time it takes the voltage regulator to set the reset out LOW after the output voltage has dropped below the reset threshold. It is typically 1  $\mu$ s for delay capacitor of 47 nF. For other values for  $C_D$  the reaction time can be estimated using the following equation:

$$t_{rr} \approx 20 \text{ s/F} \times C_D \tag{2}$$



**Figure 5 Timing (Watchdog disabled)**

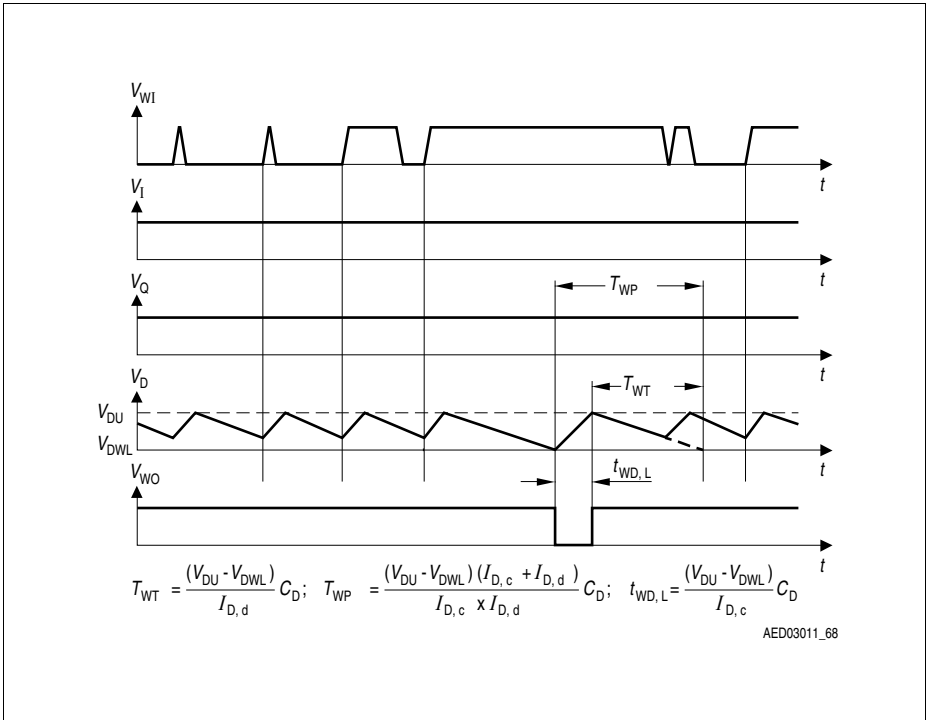
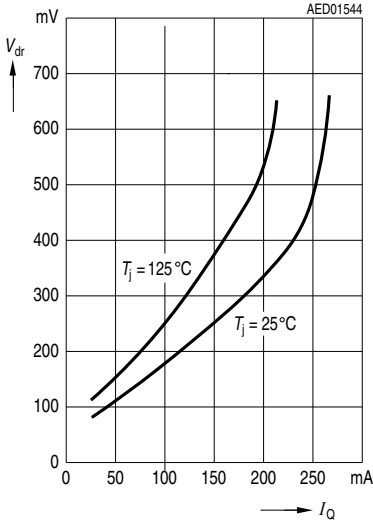
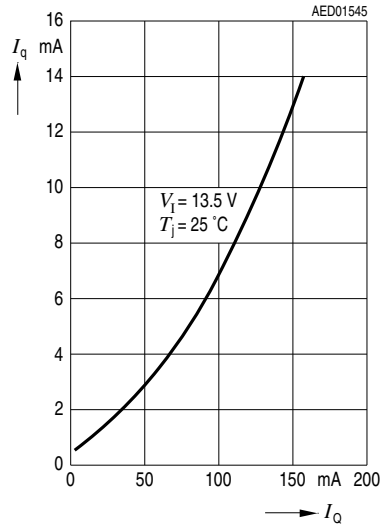


Figure 6 Timing of the Watchdog Function

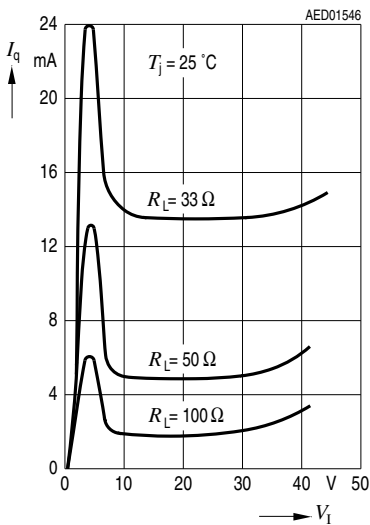
**Drop Voltage  $V_{DR}$  versus Output Current  $I_Q$**



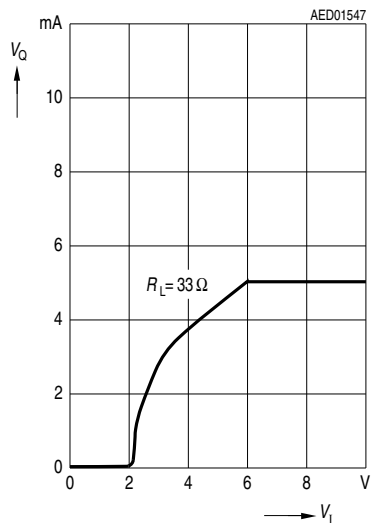
**Current Consumption  $I_q$  versus Output Current  $I_Q$**



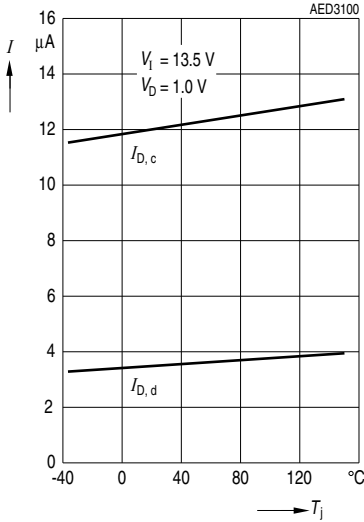
**Current Consumption  $I_q$  versus Input Voltage  $V_I$**



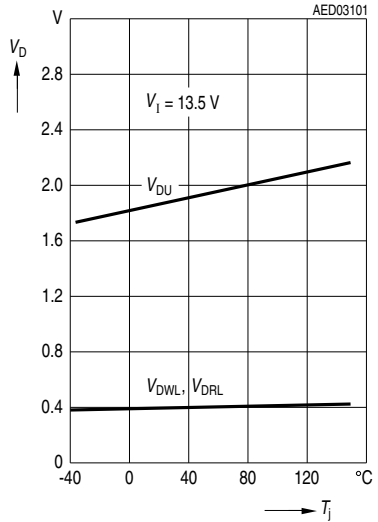
**Output Voltage versus Input Voltage  $V_I$**



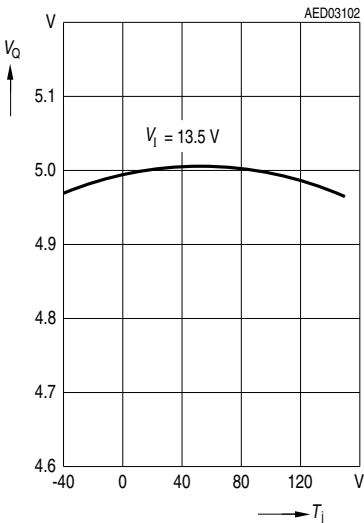
**Charge Current  $I_{D,c}$  and Discharge Current  $I_{D,d}$  versus Temperature  $T_j$**



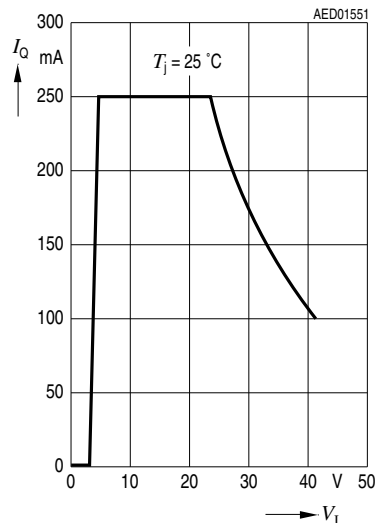
**Timing Threshold  $V_{DU}$ ,  $V_{DWL}$ ,  $V_{DRL}$  versus Temperature  $T_j$**



**Output Voltage  $V_Q$  versus Temperature  $T_j$**



**Output Current  $I_Q$  versus Input Voltage  $V_i$**



Package Outlines

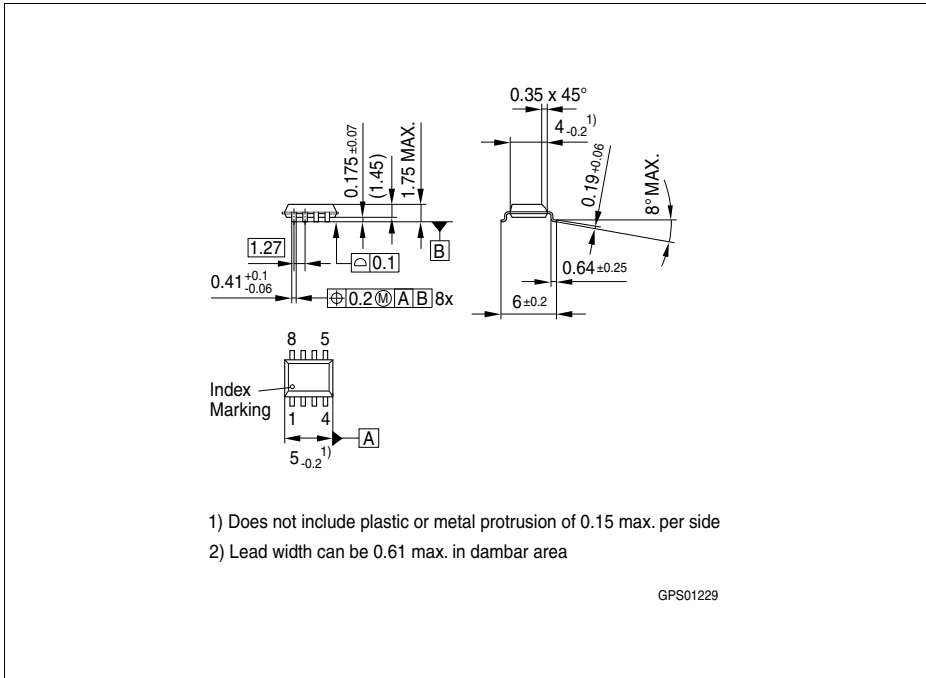


Figure 7 PG-DSO-8 (Plastic Dual Small Outline)

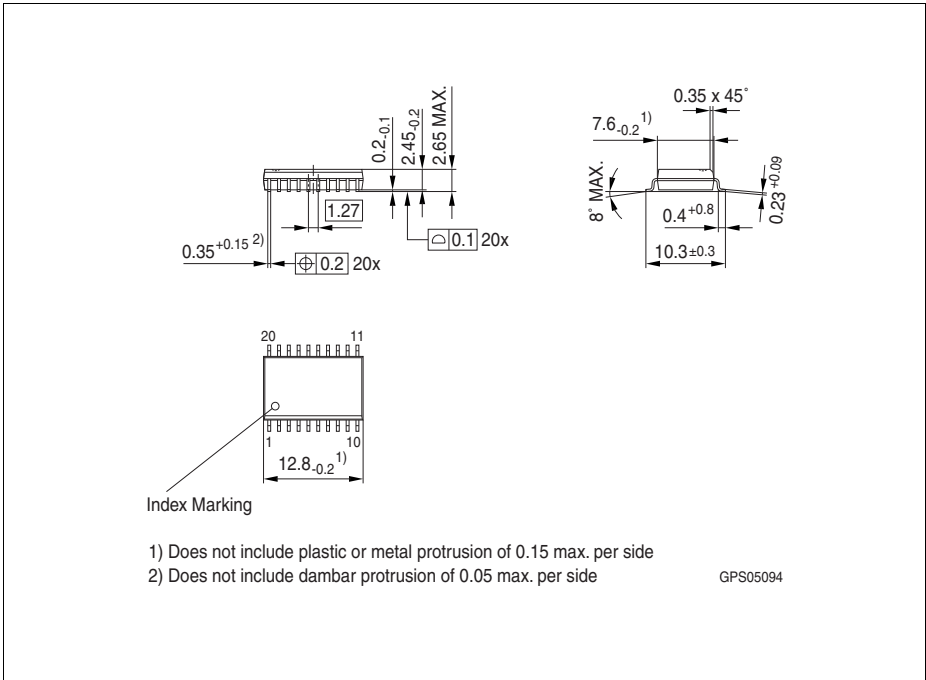
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To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

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SMD = Surface Mounted Device

Dimensions in mm



**Figure 8 PG-DSO-20 (Plastic Dual Small Outline)**

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SMD = Surface Mounted Device

Dimensions in mm

Version	Date	Changes
Rev. 1.6	2013-11-25	Package version changed: - PG-DSO-20-35 to PG-DSO-20 Package naming harmonized according to Infineon standards: - PG-DSO-8-16 to PG-DSO-8
Rev. 1.5	2007-03-20	Initial version of RoHS-compliant derivate of TLE 4268 <b>Page 1</b> : AEC certified statement added <b>Page 1</b> and <b>Page 14</b> ff: RoHS compliance statement and Green product feature added <b>Page 1</b> and <b>Page 14</b> ff: Package changed to RoHS compliant version Legal Disclaimer updated



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