PI6LC48P0101

HiFlex 10GbE Clock Generator

Features

- One Differential LVPECL output
- Crystal oscillator interface, 18pF parallel resonant crystal (23.2MHz - 30MHz)
- Output frequency range: 290MHz - 750MHz
- RMS phase jitter @ 312.5MHz, using a 25MHz crystal (12kHz - 20MHz): 0.3ps (typical), 0.5ps (max)
- 3.3V or 2.5V operating supply
- -40°C to 85°C operating temperature
- Available in 8pin TSSOP

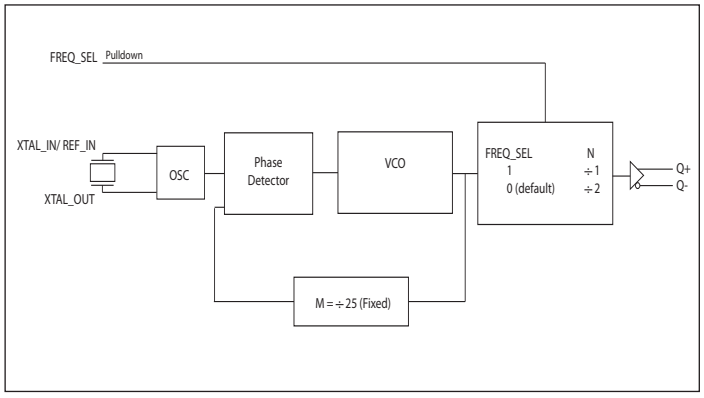
Description

The PI6LC48P0101 is a 10Gb Ethernet Clock Generator. The PI6LC48P0101 uses an 18pF parallel resonant crystal over the range of 23.2MHz - 30MHz. For Ethernet applications, a 25MHz crystal is used. The PI6LC48P0101 can achieve <0.5ps RMS phase jitter performance over the 12kHz - 20MHz integration range. The PI6LC48P0101 is packaged in a small 8-pin TSSOP, making it ideal for use in systems with limited board space.

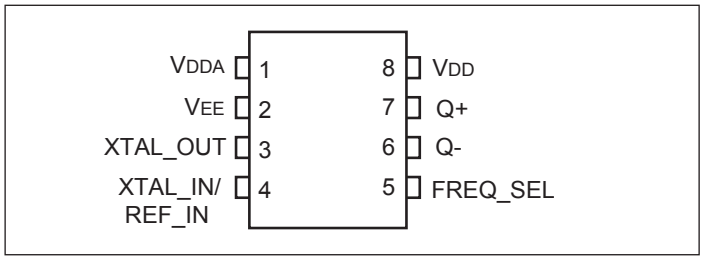
Common Configuration Table

Inputs					Output Frequency (MHz)
Crystal Frequency (MHz)	FREQ_SEL	M	N	Multiplication Value M/N	
25	1	25	1	25	625
25	0	25	2	12.5	312.5

Block Diagram



Pin Configuration



Pin Description

Pin #	Pin Name	Type		Description
1	V_{DDA}	Power		Analog supply pin.
2	V_{EE}	Power		Negative supply pin.
3	XTAL_OUT	Output		XTAL_OUT is the output.
4	XTAL_IN/ REF_IN	Input		XTAL_IN, can also be driven by a single ended reference clock
5	FREQ_SEL	Input	Pulldown	Frequency select pin. LVCMOS/LVTTL interface levels.
6, 7	Q-, Q+	Output		Differential clock outputs. LVPECL interface levels.
8	V_{DD}	Power		Core supply pin.

NOTE: Pulldown refers to internal input resistors. See Pin Characteristics for typical values.

Pin Characteristics

Symbol	Parameter	Test Condition	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

Maximum Ratings

Storage Temperature..... -65°C to+155°C
Temperature with Power Applied .....-40°C to+85°C
3.3V Supply Voltage.....-0.5 to +3.6V
ESD Protection (HBM) 2000V

Note:

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the DC Characteristics or AC Characteristics is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

DC Electrical Characteristics

Power Supply DC Characteristics (V_{DD} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.25	3.3	V_{DD}	V
I_{EE}	Power Supply Current				83	mA
I_{DDA}	Analog Supply Current				28	mA

Power Supply DC Characteristics (V_{DD} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{DD}	Core Supply Voltage		2.375	2.5	2.625	V
V_{DDA}	Analog Supply Voltage		V_{DD} – 0.25	2.5	V_{DD}	V
I_{EE}	Power Supply Current				78	mA
I_{DDA}	Analog Supply Current				28	mA

LVCMOS/LVTTL DC Characteristics (V_{DD} = 3.3V±5% or 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{IH}	Input High Voltage	V_{DD} = 3.3V	2		V_{DD} + 0.3	V
		V_{DD} = 2.5V	1.7		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage	V_{DD} = 3.3V	-0.3		0.8	V
		V_{DD} = 2.5V	-0.3		0.7	V
I_{IH}	Input High Current	V_{DD} = V_{IN} = 2.625V or 3.465V			150	µA
I_{IL}	Input Low Current	V_{DD} = 2.625V or 3.465V, V_{IN} = 0V	-5			µA

LVPECL DC Characteristics (V_{DD} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Units
V_{OH}	Output High Voltage*	V_{DD} = 3.3V	1.9		2.4	V
		V_{DD} = 2.5V	1.1		1.6	
V_{OL}	Output Low Voltage*	V_{DD} = 3.3V	1.2		1.6	V
		V_{DD} = 2.5V	0.4		0.8	
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

Note: LVPECL Termination: Source 150ohm to GND and 100ohm across CLK+ and CLK-

Crystal Characteristics

Parameter	Test Condition	Min.	Typ.	Max.	Units
Mode of Oscillation		Fundamental			
Frequency		23.2		30	MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance				7	pF

NOTE: It is not recommended to overdrive the crystal input with an external clock.

AC Electrical Characteristics

(V_{DD} = 3.3V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency	FREQ_SEL = 0		312.5		MHz
		FREQ_SEL = 1		625		MHz
tjit	RMS Phase Jitter (Random)*	312.5MHz @ Integration Range: 12kHz - 20MHz		0.3	0.5	ps
		312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.1		
		625MHz @ Integration Range: 12kHz - 20MHz		0.3	0.5	ps
		625MHz @ Integration Range: 1.875MHz - 20MHz		0.07		
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		400	ps
odc	Output Duty Cycle		47		53	%

NOTE: Refer to the Phase Noise Plots following this section.

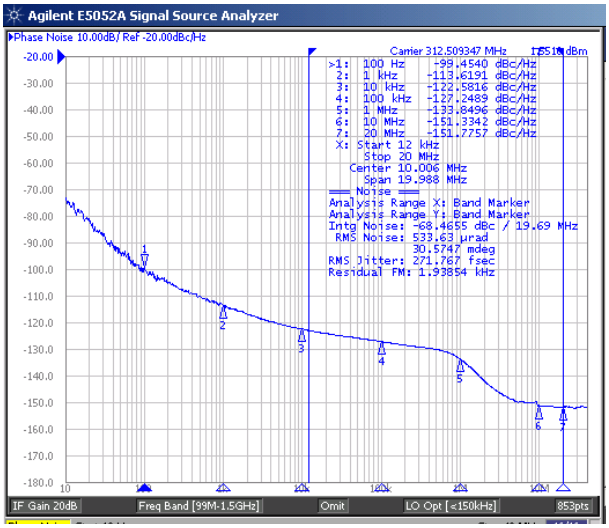
AC Electrical Characteristics (V_{DD} = 2.5V±5%, V_{EE} = 0V, T_A = -40°C to 85°C)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
f_{OUT}	Output Frequency	FREQ_SEL = 0		312.5		MHz
		FREQ_SEL = 1		625		MHz
tjit	RMS Phase Jitter (Random)*	312.5MHz @ Integration Range: 12kHz - 20MHz		0.3	0.5	ps
		312.5MHz @ Integration Range: 1.875MHz - 20MHz		0.1		
		625MHz @ Integration Range: 12kHz - 20MHz		0.3	0.5	ps
		625MHz @ Integration Range: 1.875MHz - 20MHz		0.07		
t_R / t_F	Output Rise/Fall Time	20% to 80%	100		400	ps
odc	Output Duty Cycle		47		53	%

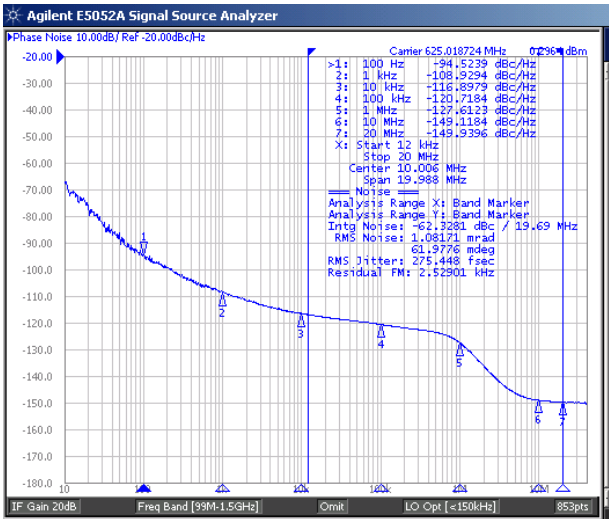
NOTE: Refer to the Phase Noise Plots following this section.

Phase Noise Plots

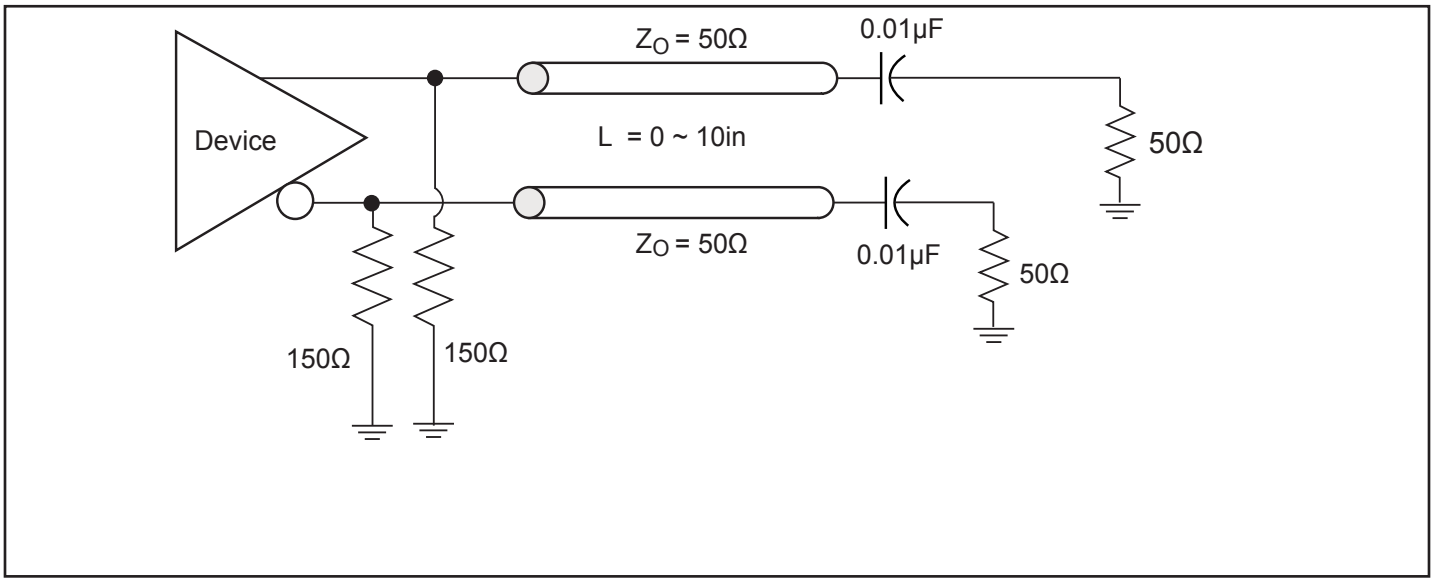
312.5MHz



625MHz

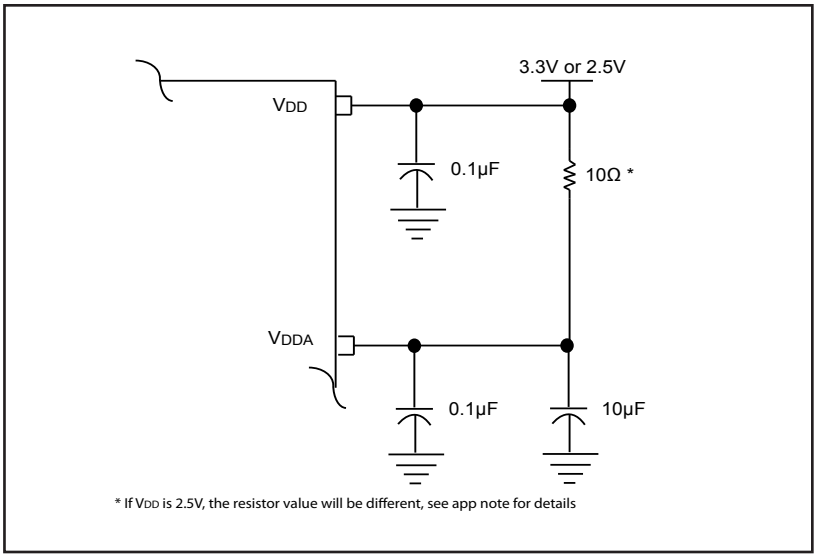


LVPECL Test Circuit



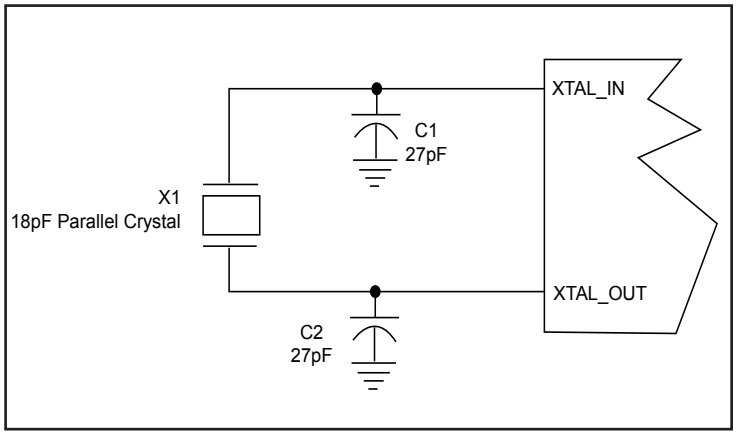
Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The PI6LC48P0101 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{DD} and V_{DDA} should be individually connected to the power supply plane through vias, and 0.1µF bypass capacitors should be used for each pin. Figure below illustrates this for a generic V_{DD} pin and also shows that V_{DDA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{DDA} pin.



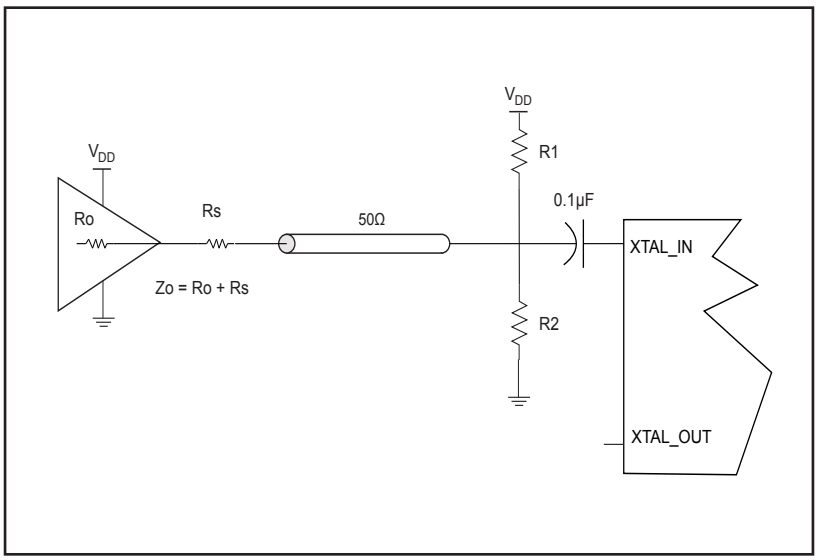
Crystal Input Interface

The clock generator has been characterized with 18pF parallel resonant crystals. The capacitor values shown in the figure below were determined using a 25MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.



LVCMOS to XTAL Interface

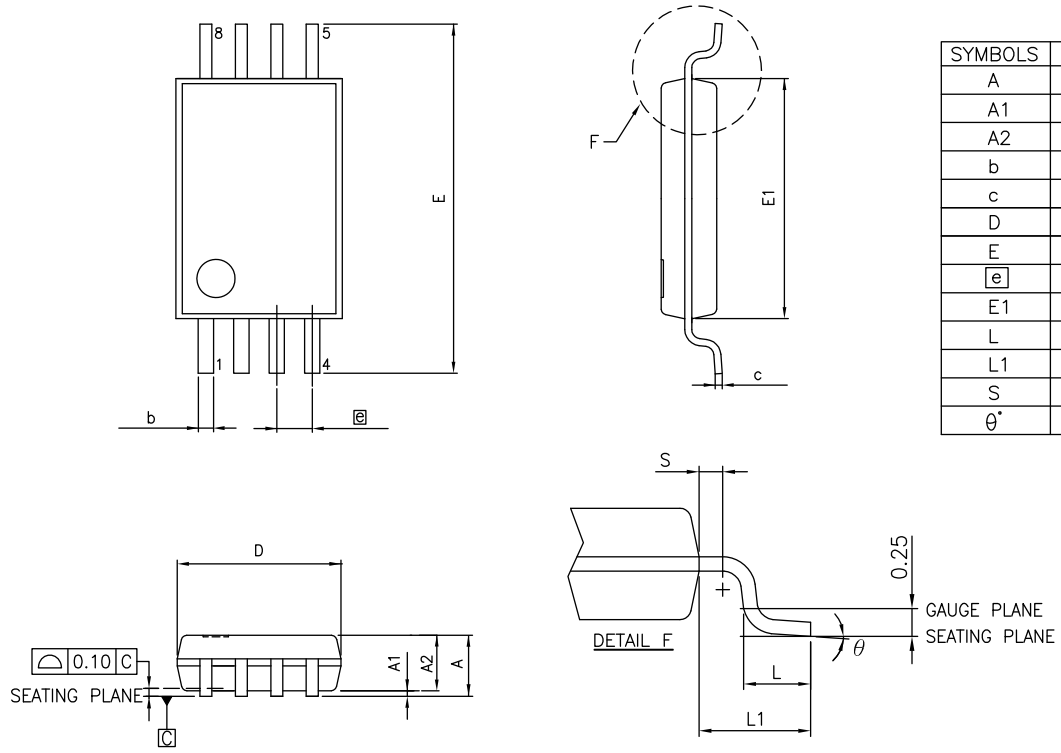
The XTAL_IN input can accept a single-ended LVCMOS signal through an AC coupling capacitor. A general interface diagram is shown in the figure below. The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS signals, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of the two ways. First, R1 and R2 in parallel should equal the transmission line empedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω. By overdriving the crystal oscillator, the device will be functional, but note, the device performance is quaranteed by using a quartz crystal.



Thermal Information

Symbol	Description	
Θ_{JA}	Junction-to-ambient thermal resistance	124 ^{O}C/W
Θ_{JC}	Junction-to-case thermal resistance	37^{O}C/W

Packaging Mechanical:



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	–	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	2.90	3.00	3.10
E		6.40 BSC	
e		0.65 BSC	
E1	4.30	4.40	4.50
L	0.45	0.60	0.75
L1		1.00 REF	
S	0.20	–	–
θ°	0	–	8

UNIT : MM

Notes:
1. Refer JEDEC MO-153F/AA
2. Controlling dimensions in millimeters
3. Package outline exclusive of mold flash and metal burr

PERICOM Enabling Serial Connectivity

DATE: 05/03/12

DESCRIPTION: 8 pin, 173mil wide TSSOP

PACKAGE CODE: L

DOCUMENT CONTROL #: PD-1308 **REVISION: F**

12-0370

Ordering Information

Ordering Code	Package Code	Package Type
PI6LC48P0101LIE	L	Pb-free & Green, 8-pin TSSOP
PI6LC48P0101LIEX	L	Pb-free & Green, 8-pin TSSOP, Tape & Reel

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
2. "E" denotes Pb-free and Green
3. Adding an "X" at the end of the ordering code denotes tape and Reel packaging

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