

1. General description

Planar passivated Silicon Controlled Rectifier with sensitive gate in a SOT54 (TO-92) plastic package. This SCR is designed to be interfaced directly to microcontrollers, logic ICs and other low power gate trigger circuits.

2. Features and benefits

- Enhanced voltage capability
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Direct triggering from low power drivers and logic ICs
- A-G-K reverse pin-out

3. Applications

- General purpose switching and phase control

4. Quick reference data

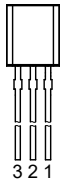

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; Fig. 1	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ °C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	9	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ °C}$; Fig. 7	-	50	200	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ °C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 12	500	800	-	V/ μs

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{DM} = 402 \text{ V}$; $T_j = 125 \text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	-	2	-	V/ μs

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>TO-92 (SOT54)</p>	
2	G	gate		
3	A	anode		

6. Ordering information

Table 3. Ordering information

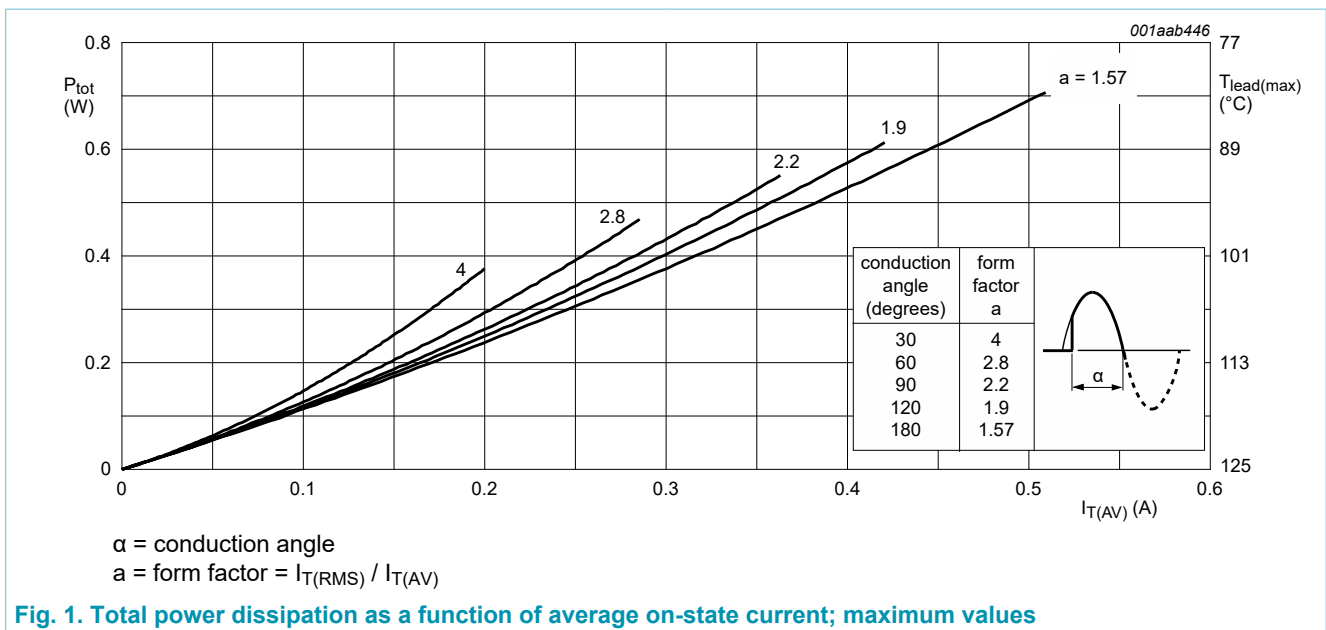
Type number	Package		
	Name	Description	Version
BT149G	TO-92	plastic single-ended leaded (through hole) package; 3 leads	SOT54

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	600	V
V_{RRM}	repetitive peak reverse voltage		-	600	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{lead} \leq 83\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; SIN	-	0.32	A^2s
dl_T/dt	rate of rise of on-state current	$I_T = 2\text{ A}$; $I_G = 10\text{ mA}$; $dl_G/dt = 100\text{ mA}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$



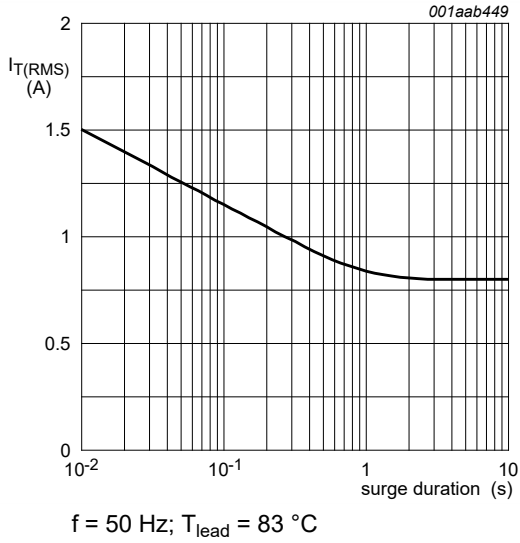


Fig. 2. RMS on-state current as a function of surge duration for sinusoidal currents

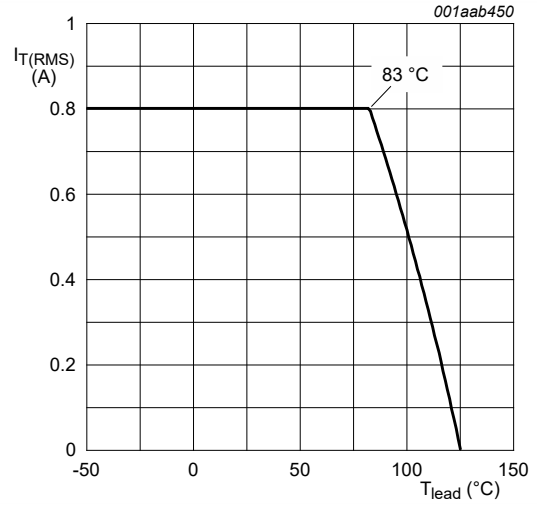


Fig. 3. RMS on-state current as a function of lead temperature; maximum values

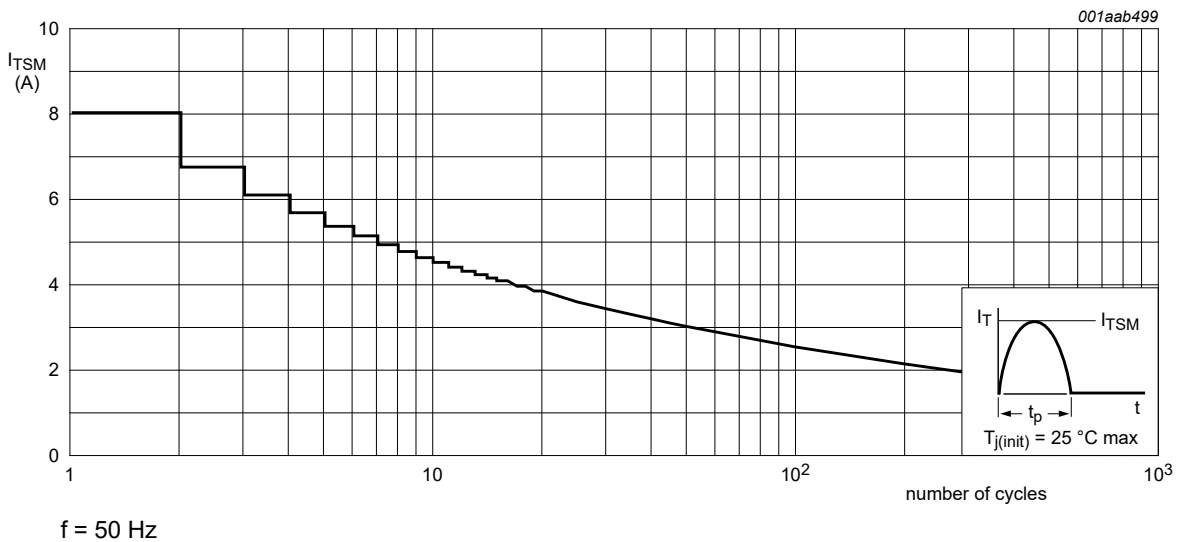
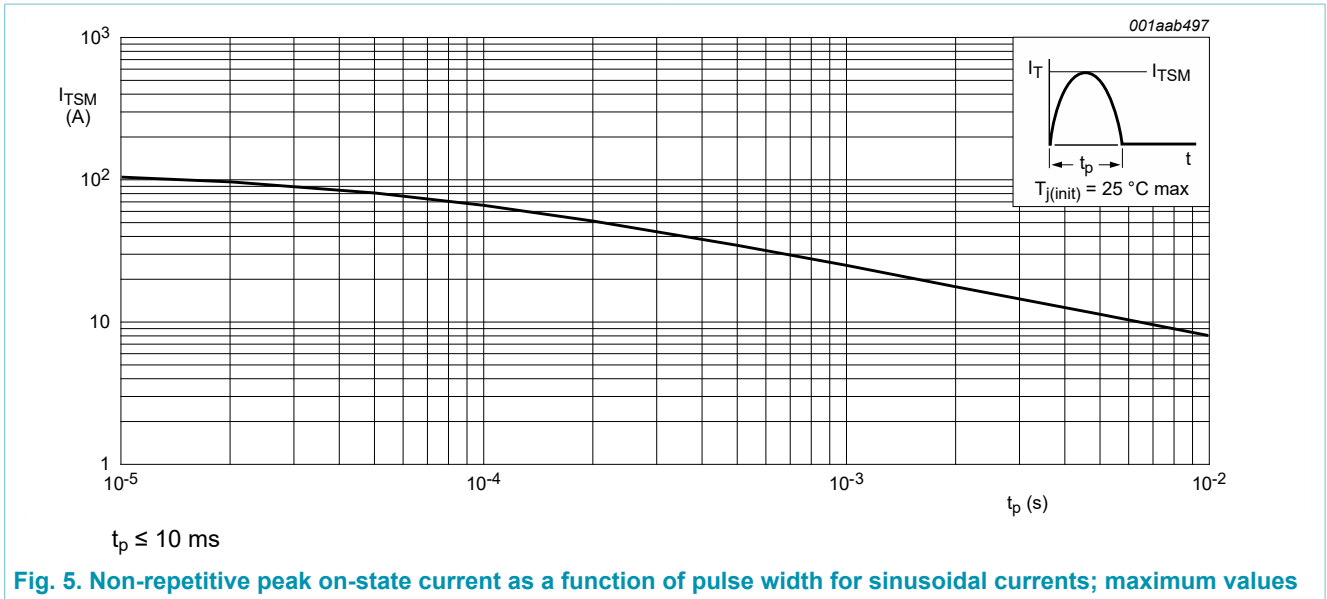


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-lead)}$	thermal resistance from junction to lead	Fig. 6	-	-	60	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted: lead length = 4 mm	-	150	-	K/W

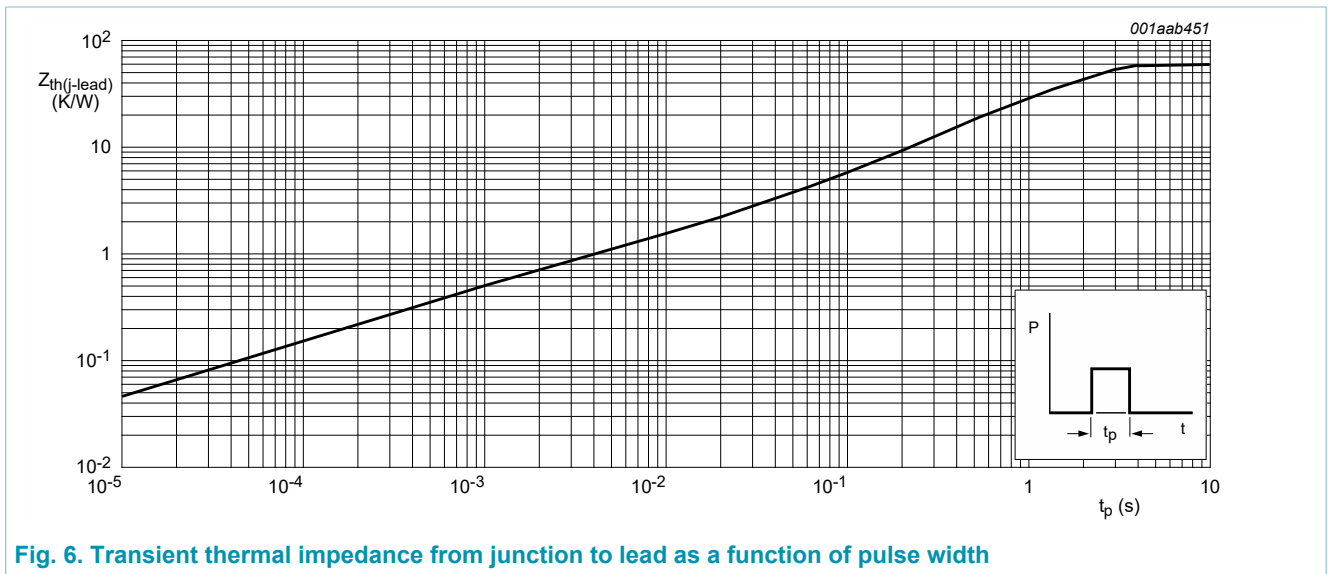


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 7	-	50	200	μA
I_L	latching current	$V_D = 12\text{ V}$; $I_G = 0.5\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$; Fig. 8	-	2	6	mA
I_H	holding current	$V_D = 12\text{ V}$; $T_j = 25\text{ }^\circ\text{C}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$; Fig. 9	-	2	5	mA
V_T	on-state voltage	$I_T = 1.2\text{ A}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 10	-	1.25	1.7	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 25\text{ }^\circ\text{C}$; Fig. 11	-	0.5	0.8	V
		$V_D = 600\text{ V}$; $I_T = 10\text{ mA}$; $T_j = 125\text{ }^\circ\text{C}$; Fig. 11	0.2	0.3	-	V
I_D	off-state current	$V_D = 600\text{ V}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$; $T_j = 125\text{ }^\circ\text{C}$	-	0.05	0.1	mA
I_R	reverse current	$V_R = 600\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$	-	0.05	0.1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $R_{GK} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; Fig. 12	500	800	-	V/ μs
		$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit; Fig. 12	-	2	-	V/ μs
t_{gt}	gate-controlled turn-on time	$I_{TM} = 2\text{ A}$; $V_D = 600\text{ V}$; $I_G = 10\text{ mA}$; $dI_G/dt = 0.1\text{ A}/\mu\text{s}$; $T_j = 25\text{ }^\circ\text{C}$	-	2	-	μs
t_q	commutated turn-off time	$V_{DM} = 402\text{ V}$; $T_j = 125\text{ }^\circ\text{C}$; $I_{TM} = 1.6\text{ A}$; $V_R = 35\text{ V}$; $(dI_T/dt)_M = 30\text{ A}/\mu\text{s}$; $dV_D/dt = 2\text{ V}/\mu\text{s}$; $R_{GK(\text{ext})} = 1\text{ k}\Omega$; ($V_{DM} = 67\%$ of V_{DRM})	-	100	-	μs

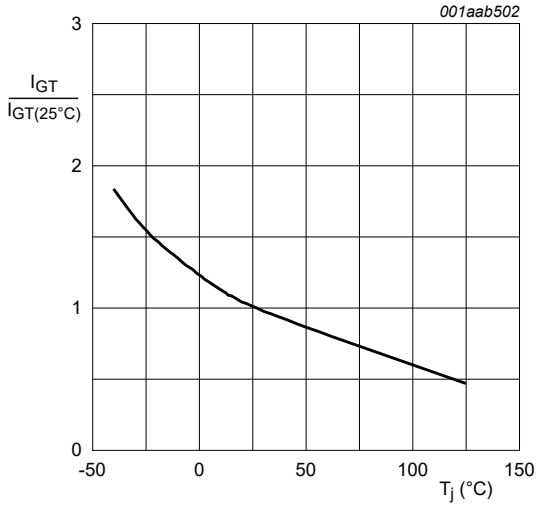


Fig. 7. Normalized gate trigger current as a function of junction temperature

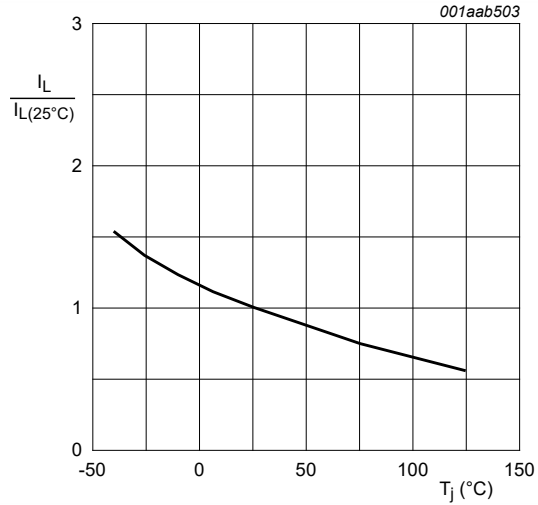


Fig. 8. Normalized latching current as a function of junction temperature
 $R_{GK} = 1 \text{ k}\Omega$

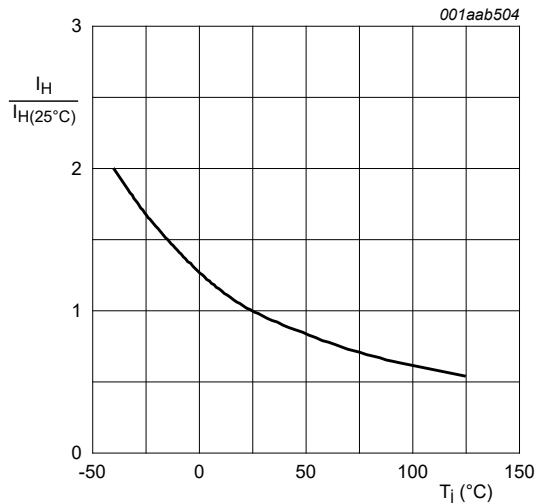


Fig. 9. Normalized holding current as a function of junction temperature
 $R_{GK} = 1 \text{ k}\Omega$

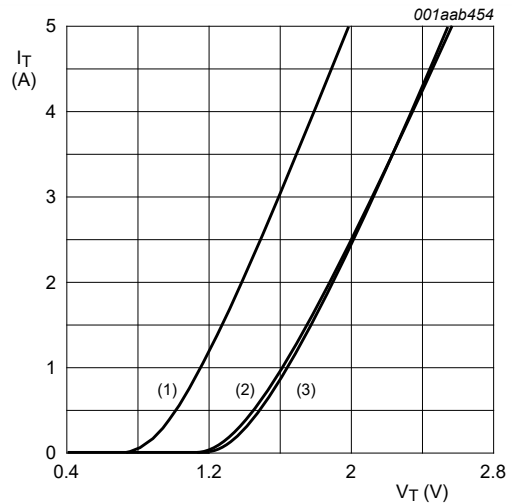


Fig. 10. On-state current as a function of on-state voltage
 $V_o = 1.067 \text{ V}; R_s = 0.187 \Omega$
 (1) $T_j = 125 \text{ }^\circ\text{C}$; typical values
 (2) $T_j = 125 \text{ }^\circ\text{C}$; maximum values
 (3) $T_j = 25 \text{ }^\circ\text{C}$; maximum values

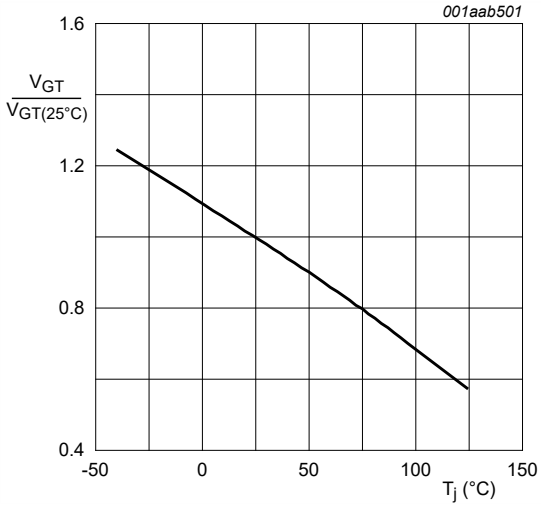
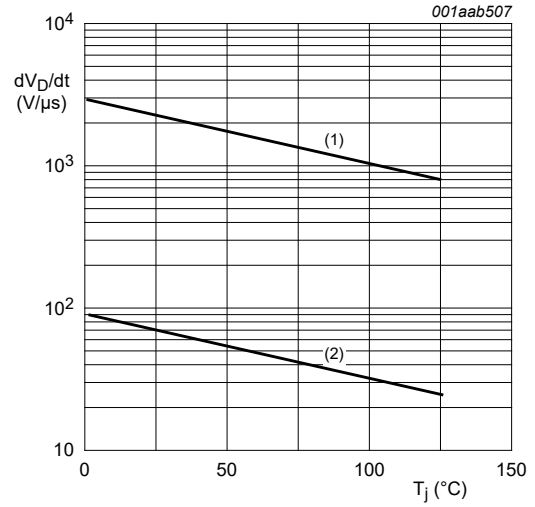


Fig. 11. Normalized gate trigger voltage as a function of junction temperature



- (1) $R_{GK} = 1 \text{ k}\Omega$
- (2) gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

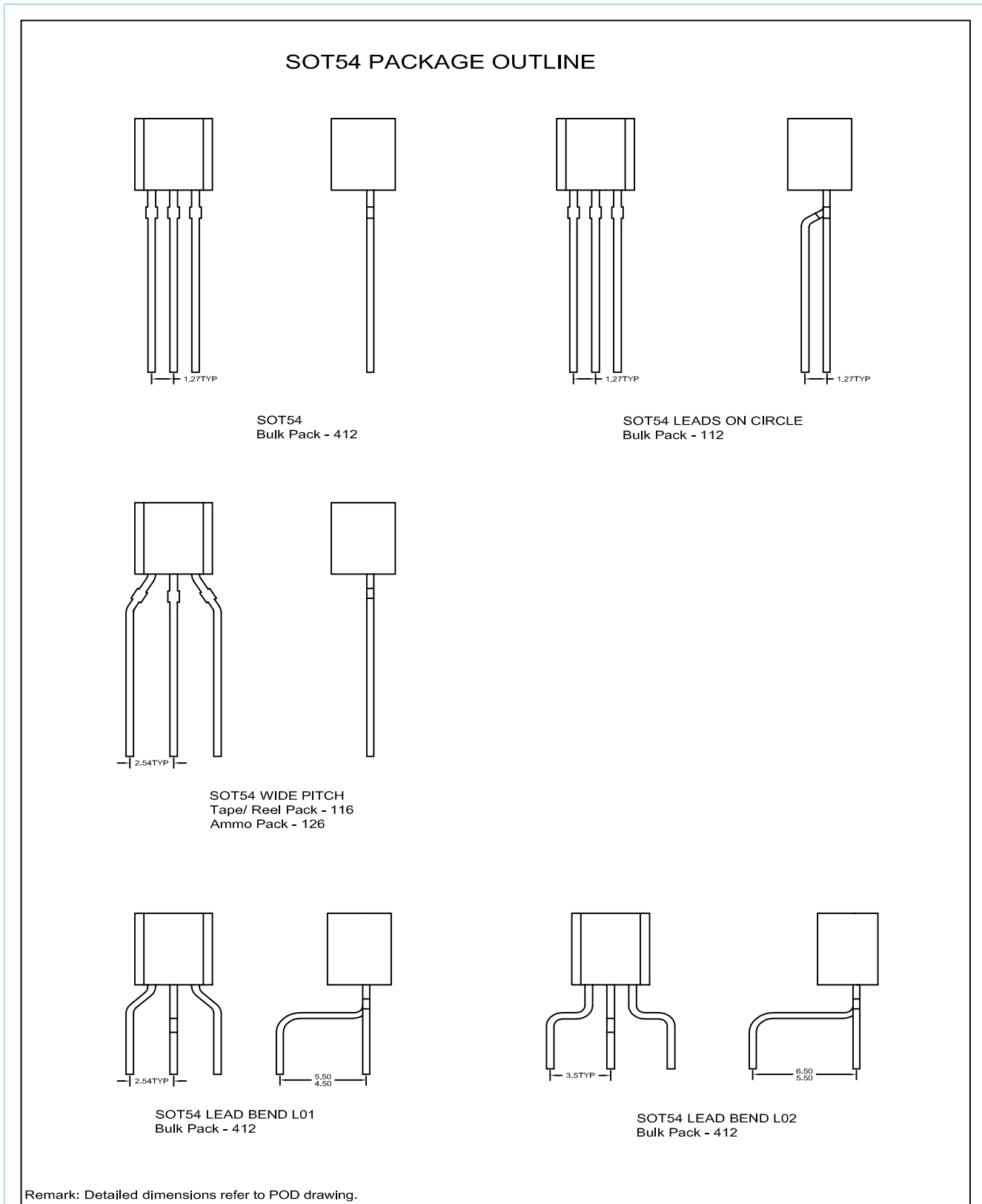


Fig. 13. Package outline TO-92 (SOT54)

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