This is a short form datasheet and is intended to provide an overview only. Additional details are available from IDT. Contact information may be found on the last page.

HIGHLIGHTS

- Synchronization Management Unit (SMU) provides tools to manage physical layer and packet based synchronous clocks for IEEE 1588 / PTP Telecom Profile applications
- Supports independent IEEE 1588 and Synchronous Ethernet (SyncE) timing paths
- Combo mode provides SyncE physical layer frequency support for IEEE 1588 Telecom Boundary Clocks (T-BC) and Telecom Time Slave Clocks (T-TSC) per G.8273.2
- Digital PLL 1 (DPLL1) and DPLL 2 can be configured as Digitally Controlled Oscillators (DCOs) for PTP clock synthesis
- DCO frequency resolution is [(77760 / 1638400) * 2^-48] or ~1.686305041e-10 ppm
- DPLL1 and DPLL2 generate G.8262 compliant SyncE clocks
- Two independent Time of Day (ToD) counters/time accumulators, one associated with each of DPLL1 and DPLL2, can be used to track differences between the two time domains and to time-stamp external events
- DPLL3 performs rate conversions to frequency synchronization interfaces or for other general purpose timing applications
- APLL1 and APLL2 generate clocks with jitter < 1 ps RMS (12 kHz to 20 MHz) for: 1000BASE-T and 1000BASE-X
- Fractional-N input dividers support a wide range of reference frequencies
- Locks to 1 Pulse Per Second (PPS) references
- It can be configured from an external EEPROM after reset

FEATURES

- Composite clock inputs (IN1 and IN2) accept 64 kHz synchronization interface signals per ITU-T G.703
- Differential reference inputs (IN3 to IN8) accept clock frequencies between 1 PPS and 650 MHz
- Single ended inputs (IN9 to IN14) accept reference clock frequencies between 1 PPS and 162.5 MHz
- Loss of Signal (LOS) pins (LOS0 to LOS3) can be assigned to any clock reference input
- Reference monitors qualify/disqualify references depending on activity, frequency and LOS pins
- Automatic reference selection state machines select the active reference for each DPLL based on the reference monitors, priority tables, revertive and non-revertive settings and other programmable settings
- Fractional-N input dividers enable the DPLLs to lock to a wide range of reference clock frequencies including: 10/100/1000 Ethernet, 10G Ethernet, OTN, SONET/SDH, PDH, TDM, GSM, CPRI and GNSS frequencies
- Any reference input (IN3 to IN14) can be designated as external sync pulse inputs (1 PPS, 2 kHz, 4 kHz or 8 kHz) associated with a selectable reference clock input
- FRSYNC_8K_1PPS and MFRSYNC_2K_1PPS output sync pulses that are aligned with the selected external input sync pulse input and frequency locked to the associated reference clock input
- DPLL1 and DPLL2 can be configured with bandwidths between 0.09 mHz and 567 Hz
- DPLL1 and DPLL2 lock to input references with frequencies between 1 PPS and 650 MHz
- DPLL3 locks to input references with frequencies between 8 kHz and 650 MHz
- DPLL1 and DPLL2 comply with ITU-T G.8262 for Synchronous Ethernet Equipment Clock (EEC), and G.813 for Synchronous Equipment Clock (SEC); and Telcordia GR-253-CORE for Stratum 3 and SONET Minimum Clock (SMC)
- DPLL1 and DPLL2 generate clocks with PDH, TDM, GSM, CPRI/OBSAI, 10/100/1000 Ethernet and GNSS frequencies; these clocks are directly available on OUT1 and OUT8
- DPLL1 and DPLL2 can be configured as DCOs to synthesize IEEE 1588 clocks
- DPLL3 generates N x 8 kHz clocks up to 100 MHz that are output on OUT10 and OUT11
- APLL1 and APLL2 can be connected to DPLL1 or DPLL2
- APLL1 and APLL2 generate 10/100/1000 Ethernet, 10G Ethernet, or SONET/SDH frequencies
- Any of eight common TCXO/OCXO frequencies can be used for the System Clock: 10 MHz, 12.8 MHz, 13 MHz, 19.44 MHz, 20 MHz, 24.576 MHz, 25 MHz or 30.72 MHz
- The I2C slave, SPI or the UART interface can be used by a host processor to access the control and status registers
- The I2C master interface can automatically load a device configuration from an external EEPROM after reset
- DPLL1 or DPLL3 can be connected to an internal composite clock generator that outputs its 64 kHz synchronization signal on OUT8
- Differential outputs OUT3 to OUT6 output clocks with frequencies between 1 PPS and 650 MHz
- Single ended outputs OUT1, OUT2, OUT7 and OUT8 output clocks with frequencies between 1 PPS and 125 MHz
- Single ended outputs OUT10 and OUT11 output clocks N*8kHz multiples up to 100 MHz
- DPLL1 and DPLL2 support independent programmable delays for each of IN3 to IN14; the delay for each input is programmable in steps of 0.61 ns with a range of ~±78 ns
- The input to output phase delay of DPLL1 and DPLL2 is programmable in steps of 0.0745 ps with a total range of ±20 µs
- The clock phase of each of the output dividers for OUT1 (from APLL1) to OUT8 is individually programmable in steps of ~200 ps with a total range of +/-180°
- 1149.1 JTAG Boundary Scan
- 144-pin CABGA green package

APPLICATIONS

- Access routers, edge routers, core routers
- Carrier Ethernet switches
- Multiservice access platforms
- PON OLT
- LTE eNodeB
- IEEE 1588 / PTP Telecom Profile clock synthesizer
- ITU-T G.8273.2 Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC)
- ITU-T G.8264 Synchronous Equipment Timing Source (SETS)
- ITU-T G.8263 Packet-based Equipment Clock (PEC)
- ITU-T G.8262 Synchronous Ethernet Equipment Clock (EEC)
- ITU-T G.813 Synchronous Equipment Clock (SEC)
- Telcordia GR-253-CORE Stratum 3 Clock (S3) and SONET Minimum Clock (SMC)

DESCRIPTION

The 82P33810 Synchronization Management Unit (SMU) provides tools to manage timing references, clock sources and timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks. The device supports up to three independent timing paths that control: PTP clock synthesis; SyncE clock generation; and general purpose frequency translation. The device supports physical layer timing with Digital PLLs (DPLLs) and it supports packet based timing with Digitally Controlled Oscillators (DCOs). Input-to- input, input-to-output and output-to-output phase skew can all be precisely managed. The device outputs low-jitter clocks that can directly synchronize Ethernet interfaces; as well as SONET/SDH and PDH interfaces and IEEE 1588 Time Stamp Units (TSUs).

The 82P33810 accepts six differential reference inputs and six single ended reference inputs that can operate at common GNSS, Ethernet, SONET/SDH and PDH frequencies that range in frequency from 1 Pulse Per Second (PPS) to 650 MHz. The device also provides two Alternate Mark Inversion (AMI) inputs for Composite Clock (CC) signals bearing 64 kHz, 8 kHz and 0.4 kHz synchronization information. The references are continually monitored for loss of signal and for frequency offset per user programmed thresholds. All of the references are available to all three DPLLs. The active reference for each DPLL is determined by forced selection or by automatic selection based on user programmed priorities and locking allowances and based on the reference monitors and LOS inputs.

The 82P33810 can accept a clock reference and an associated phase locked sync signal as a pair. DPLL1 or DPLL2 can lock to the clock reference and align the frame sync and multi-frame sync outputs with the paired sync input. The device allows any of the differential or single ended reference inputs to be configured as sync inputs that can be associated with any of the other differential or single ended reference inputs. The input sync signals can have a frequency of 1 PPS, 2 kHz, 4 kHz or 8 kHz. This feature enables DPLL1 or DPLL2 to phase align its frame sync and multi-frame sync outputs with a sync input without the need use a low bandwidth setting to lock directly to the sync input.

DPLL1 and DPLL2 support four primary operating modes: Free-Run, Locked, Holdover and DCO. In Free-Run mode the DPLLs synthesize clocks based on the system clock alone. In Locked mode the DPLLs filter reference clock jitter with the selected bandwidth. In Locked mode, the long-term output frequency accuracy is the same as the long term frequency accuracy of the selected input reference. In Holdover mode, the DPLL uses frequency data acquired while in Locked mode to generate accurate frequencies when input references are not available. In DCO mode the DPLL control loop is opened and the DCO can be controlled by a PTP clock recovery servo running on an external processor to synthesize PTP clocks.

The 82P33810 requires a system clock for its reference monitors and other digital circuitry. The frequency accuracy of the system clock determines the frequency accuracy of the DPLLs in Free-Run mode. The frequency stability of the system clock determines the frequency stability of the DPLLs in Free-Run mode and in Holdover mode; and it affects the wander generation of the DPLLs in Locked and DCO modes.

When used with a suitable system clock, DPLL1 and DPLL2 meet the frequency accuracy, pull-in, hold-in, pull-out, noise generation, noise tolerance, transient response, and holdover performance requirements of the following applications: ITU-T G.8262/G.813 EEC/SEC options 1 and 2, ITU-T G.8263, ITU-T G.8273.2, Telcordia GR-1244 Stratum 3 (S3), Telcordia GR-253-CORE Stratum 3 (S3) and SONET Minimum Clock (SMC).

DPLL1 and DPLL2 can be configured with a range of selectable filtering bandwidths from 0.09 mHz to 567 Hz. The 17 mHz bandwidth can be used to lock the DPLL directly to a 1 PPS reference. The 69 mHz and the 92 mHz bandwidths can be used for G.8273.2. The 92 mHz bandwidth can be used for G.8262/G.813 Option 2 or Telcordia GR-253-CORE S3 or SMC applications. The bandwidths in the range 1.1 Hz to 8.9 Hz can be used for G.8262/G.813 Option 1 applications. Bandwidths above 10 Hz can be used in jitter attenuation and rate conversion applications.

DPLL1 and DPLL2 are each connected to Time of Day (ToD) counters or time accumulators; these ToD counters/time accumulators can be used to track differences between the two time domains and to time-stamp external events by using reference inputs as triggers.

DPLL3 supports three primary operation modes: Free-Run, Locked and Holdover. DPLL3 is a wideband (BW > 25Hz) frequency translator that can be used, for example, to convert a recovered line clock to a 1.544 MHz or 2.048 MHz synchronization interface clock.

In Telecom Boundary Clock (T-BC) and Telecom Time Slave Clock (T-TSC) applications per ITU-T G.8275.2, DPLL1 and DPLL2 are both used; one DPLL is configured as a DCO to synthesize PTP clocks and the other DPLL is configured as an EEC/SEC to generate physical layer clocks. Combo mode provides physical layer frequency support from the EEC/SEC to the PTP clock.

In Synchronous Equipment Timing Source (SETS) applications per ITU-T G.8264, DPLL1 or DPLL2 can be configured as an EEC/SEC to output clocks for the T0 reference point and DPLL3 can be used to output clocks for the T4 reference point.

Clocks generated by DPLL1 or DPLL2 can be passed through APLL1 or APLL2 which are LC based jitter attenuating Analog PLLs (APLLs). The output clocks generated by APLL1 and APLL2 are suitable for serial GbE and lower rate interfaces.

The device provides an AMI output for a CC signal bearing 64 kHz, 8 kHz and 0.4 kHz synchronization information. The CC output can be connected to either DPLL1 or DPLL3.

All 82P33810 control and status registers are accessed through an I2C slave, SPI or the UART microprocessor interface. For configuring the DPLLs, APLL1 and APLL2, the I2C master interface can automatically load a configuration from an external EEPROM after reset.

FUNCTIONAL BLOCK DIAGRAM

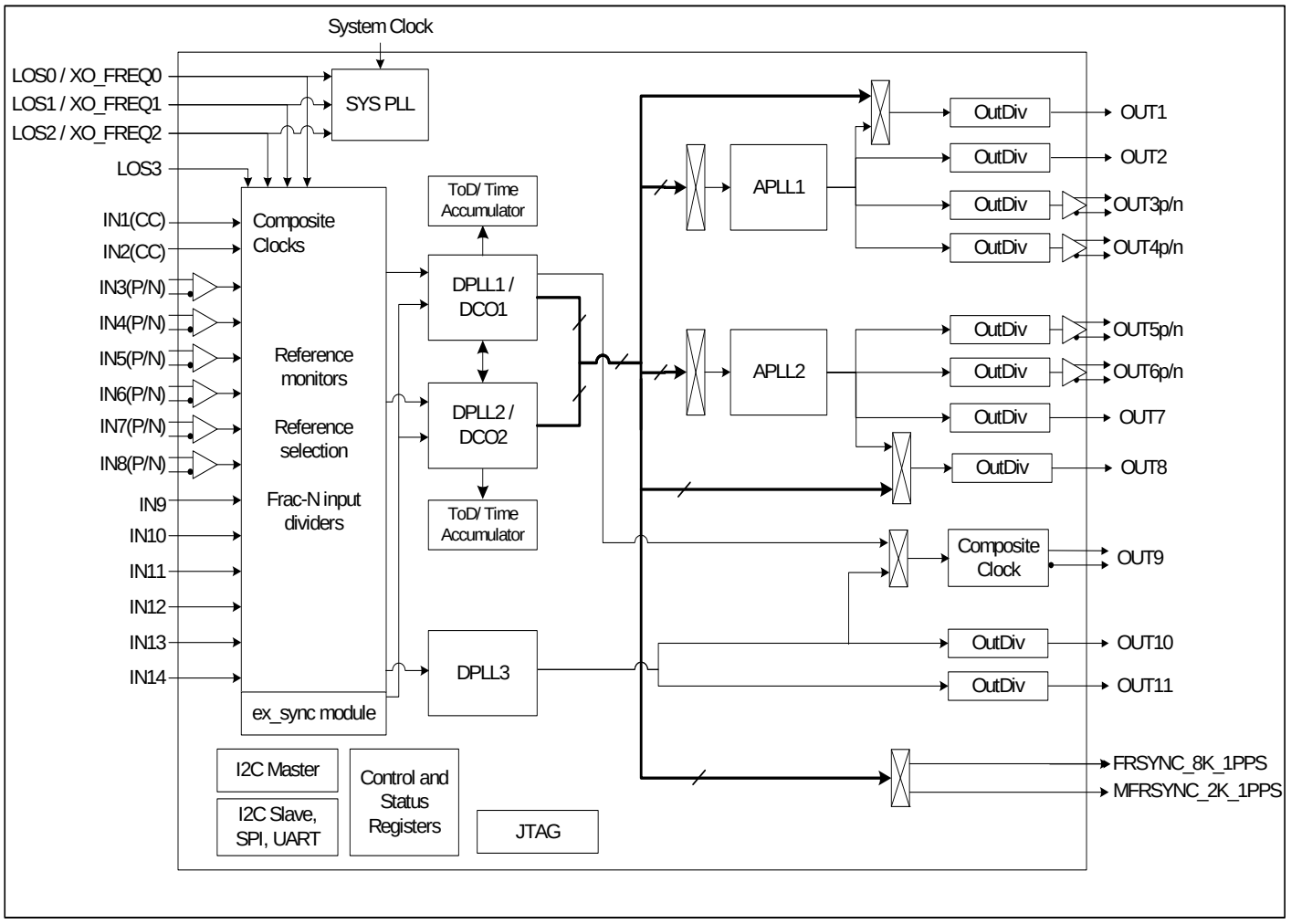

Figure 1. Functional Block Diagram

1 PIN ASSIGNMENT

	1	2	3	4	5	6	7	8	9	10	11	12	
A	IC	IC	IC	IC	VDDAO	OUT5_POS	VDDAO	OUT6_POS	CAP2	IC	SONET/SDH/LOS3	IC	A
B	VSSAO	VDDAO	VDDAO	VSSAO	VSSAO	OUT5_NEG	VSSAO	OUT6_NEG	VSSA	IC	MPU_MODE1/I2CM_SCL	IC	B
C	VDDA	VSSA	VSS	OUT7	SDO/I2C_SDA/UART_TX	VDDA	VDDA	CS/I2C_AD0	CAP1	OUT8	MPU_MODE0/I2CM_SDA	Mfrsync_2K_1PPS	C
D	VSSA	VDDA	VSSCOM	VSSD	VDDD	VSSA	VSSA	CAP3	SDI/I2C_AD2/UART_RX	SCLK/I2C_SCL	OUT11	OUT10	D
E	OSCI	VSSA	IC	VDDDO	CLKE/I2C_AD1	VDDDO	VSSDO	VSSA	DPLL3_LOCK	IN14	IN13	Frsync_8K_1PPS	E
F	TMS	VDDA	VSSA	VSSDO	VSS	VSSD	VDDD	VSSA	VDDA	IN12	IN8_NEG	IN8_POS	F
G	TCK	VDDA	IC	VSS	VSS	VSS	IC	VSS	DPLL2_LOCK	IN11	IN7_NEG	IN7_POS	G
H	xo_freq0/LOS0	VDDA	VSSA	VSS	VSS	VSS	VSS	VSS	DPLL1_LOCK	IN10	VSSD	VDDD_1_8	H
J	xo_freq1/LOS1	xo_freq2/LOS2	VSS	VSS	VSS	VSS	VSS	VSS	INT_REQ	IN9	IN6_NEG	IN6_POS	J
K	VDDA	VDDA	TRSTB	VSSAO	OUT2	RSTB	VSSDO	MS_SL	IN2	IN1	IN5_NEG	IN5_POS	K
L	VSSA	VSSA	TDI	VDDAO	TDO	IC	VDDDO	OUT1	VSSD	VDDD_1_8	IN4_NEG	IN4_POS	L
M	OUT4_POS	OUT4_NEG	VSSAO	VDDAO	OUT3_POS	OUT3_NEG	VSSDO	VDDDO	OUT9_POS	OUT9_NEG	IN3_NEG	IN3_POS	M
	1	2	3	4	5	6	7	8	9	10	11	12	

Figure 2. Pin Assignment (Top View)

2 PIN DESCRIPTION

Table 1: Pin Description

Pin No.	Name	I/O	Type	Description
Global Control Signal				
E1	OSCI	I	CMOS	OSCI: Crystal Oscillator System Clock A clock provided by a crystal oscillator is input on this pin. It is the system clock for the device. The oscillator frequency is selected via pins XO_FREQ0 ~ XO_FREQ2
K8	MS/SL	I pull-up	CMOS	MS/SL: Master / Slave Selection This pin, together with the MS_SL_CTRL bit, controls whether the device is configured as the Master or as the Slave. The signal level on this pin is reflected by the MASTER_SLAVE bit.
A11	SONET/SDH/ LOS3	I pull-down	CMOS	SONET/SDH: SONET / SDH Frequency Selection During reset, this pin determines the default value of the IN_SONET_SDH bit (b2, 09H): High: The default value of the IN_SONET_SDH bit is '1' (SONET); Low: The default value of the IN_SONET_SDH bit is '0' (SDH). After reset, this pin takes on the operation of LOS3 LOS3- This pin is used to disqualify input clocks. See input clocks section for more details.
K6	RSTB	I pull-up	CMOS	RSTB: Reset Refer to section 2.2 reset operation for detail.
H1 J1 J2	XO_FREQ0/ LOS0 XO_FREQ1/ LOS1 XO_FREQ2/ LOS2	I pull-down	CMOS	XO_FREQ0 ~ XO_FREQ2: These pins set the oscillator frequency. XO_FREQ[2:0] Oscillator Frequency (MHz) 000 10.000 001 12.800 010 13.000 011 19.440 100 20.000 101 24.576 110 25.000 111 30.720 LOS0 ~ LOS2 - These pins are used to disqualify input clocks. See input clocks section for more details. After reset, this pin takes on the operation of LOS0-LOS2
Input Clock and Frame Synchronization Input Signal				
K10	IN1	I	AMI	IN1: Input Clock 1 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin. AMI input has internal 1k ohm to 1.5V termination.
K9	IN2	I	AMI	IN2: Input Clock 2 A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is input on this pin. AMI input has internal 1k ohm to 1.5V termination.
M12 M11	IN3_POS IN3_NEG	I	PECL/LVDS	IN3_POS / IN3_NEG: Positive / Negative Input Clock 3 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
L12 L11	IN4_POS IN4_NEG	I	PECL/LVDS	IN4_POS / IN4_NEG: Positive / Negative Input Clock 4 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
K12 K11	IN5_POS IN5_NEG	I	PECL/LVDS	IN5_POS / IN5_NEG: Positive / Negative Input Clock 5 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
J12 J11	IN6_POS IN6_NEG	I	PECL/LVDS	IN6_POS / IN6_NEG: Positive / Negative Input Clock 6 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
G12 G11	IN7_POS IN7_NEG	I	PECL/LVDS	IN7_POS / IN7_NEG: Positive / Negative Input Clock 7 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
F12 F11	IN8_POS IN8_NEG	I	PECL/LVDS	IN8_POS / IN8_NEG: Positive / Negative Input Clock 8 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
J10	IN9	I pull-down	CMOS	IN9: Input Clock 9 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
H10	IN10	I pull-down	CMOS	IN10: Input Clock 10 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
G10	IN11	I pull-down	CMOS	IN11: Input Clock 11 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
F10	IN12	I pull-down	CMOS	IN12: Input Clock 12 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
E11	IN13	I pull-down	CMOS	IN13: Input Clock 13 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
E10	IN14	I pull-down	CMOS	IN14: Input Clock 14 A reference clock is input on this pin.This pin can also be used as a sync input, and in this case a 2 kHz, 4 kHz, 8 kHz, or 1PPS signal can be input on this pin.
Output Frame Synchronization Signal				
E12	FRSYNC _8K_1PPS	O	CMOS	FRSYNC_8K_1PPS: 8 kHz Frame Sync Output An 8 kHz signal or a 1PPS sync signal is output on this pin.
C12	MFRSYNC _2K_1PPS	O	CMOS	MFRSYNC_2K_1PPS: 2 kHz Multiframe Sync Output A 2 kHz signal or a 1PPS sync signal is output on this pin.
Output Clock				
L8 K5	OUT1 OUT2	O	CMOS	OUT1 ~ OUT2: Output Clock 1 ~ 2
M5 M6	OUT3_POS OUT3_NEG	O	PECL/LVDS	OUT3_POS / OUT3_NEG: Positive / Negative Output Clock 3 This output is set to LVDS by default.The LVDS output has internal 100 ohm termination.
M1 M2	OUT4_POS OUT4_NEG	O	PECL/LVDS	OUT4_POS / OUT4_NEG: Positive / Negative Output Clock 4 This output is set to LVDS by default.The LVDS output has internal 100 ohm termination.
A6 B6	OUT5_POS OUT5_NEG	O	PECL/LVDS	OUT5_POS / OUT5_NEG: Positive / Negative Output Clock 5 This output is set to LVDS by default.The LVDS output has internal 100 ohm termination.
A8 B8	OUT6_POS OUT6_NEG	O	PECL/LVDS	OUT6_POS / OUT6_NEG: Positive / Negative Output Clock 6 This output is set to LVDS by default.The LVDS output has internal 100 ohm termination.
C4 C10	OUT7 OUT8	O	CMOS	OUT7 ~ OUT8: Output Clock 7 ~ 8
M9 M10	OUT9_POS OUT9_NEG	O	AMI	OUT9_POS / OUT9_NEG: Positive / Negative Output Composite Clock A 64 kHz + 8 kHz or 64 kHz + 8 kHz + 0.4 kHz composite clock is differentially output on this pair of pins.
D12 D11	OUT10 OUT11	O	CMOS	OUT10 ~ OUT11: Output Clock 10 ~ 11
Miscellaneous				
C9, A9, D8	CAP1, CAP2, CAP3			CAP1, CAP2 and CAP3: Analog Power Filter Capacitor connection 1 to 3. These capacitors are be part of the power filtering.
Lock Signal				
E9	DPLL3_LOCK	O	CMOS	DPLL3_LOCK This pin goes high when DPLL3 is locked
G9	DPLL2_LOCK	O	CMOS	DPLL2_LOCK This pin goes high when DPLL2 is locked

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
H9	DPLL1_LOCK	O	CMOS	DPLL1_LOCK This pin goes high when DPLL1 is locked
Microprocessor Interface				
J9	INT_REQ	O Tri-state	CMOS	INT_REQ: Interrupt Request This pin is used as an interrupt request.
B11 C11	MPU_MODE1/ I2CM_SCL MPU_MODE0/ I2CM_SDA	I/O pull-up	CMOS/ Open Drain	MPU_MODE[1:0]: Microprocessor Interface Mode Selection During reset, these pins determine the default value of the MPU_SEL_CNFG[1:0] bits as follows: 00: I2C mode 01: SPI mode 10: UART mode 11: I2C master (EEPROM) mode I2CM_SCL: Serial Clock Line In I2C master mode, the serial clock is output on this pin. I2CM_SDA: Serial Data Input for I2C Master Mode In I2C master mode, this pin is used as the for the serial data.
D9	SDI/I2C_AD2/ UART_RX	I pull-down	CMOS	SDI: Serial Data Input In Serial mode, this pin is used as the serial data input. Address and data on this pin are serially clocked into the device on the rising edge of SCLK. I2C_AD2: Device Address Bit 2 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface. UART_RX In UART mode, this pin is used as the receive data (UART Receive)
E5	CLKE/I2C_AD1	I pull-down	CMOS	CLKE: SCLK Active Edge Selection In Serial mode, this pin is an input, it selects the active edge of SCLK to update the SDO: High - The falling edge; Low - The rising edge. I2C_AD1: Device Address Bit 1 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
C8	CS/I2C_AD0	I pull-up	CMOS	CS: Chip Selection In Serial modes, this pin is an input.A transition from high to low must occur on this pin for each read or write operation and this pin should remain low until the operation is over. I2C_AD0: Device Address Bit 0 In I2C mode, I2C_AD[2:0] pins are the address bus of the microprocessor interface.
D10	SCLK/I2C_SCL	I	CMOS	SCLK: Shift Clock In Serial mode, a shift clock is input on this pin. Data on SDI is sampled by the device on the rising edge of SCLK. Data on SDO is updated on the active edge of SCLK. The active edge is determined by the CLKE. I2C_SCL: Serial Clock Line In I2C mode, the serial clock is input on this pin.
C5	SDO/I2C_SDA/ UART_TX	I/O	CMOS/ Open Drain	SDO: Serial Data Output In Serial mode, this pin is used as the serial data output. Data on this pin is serially clocked out of the device on the active edge of SCLK. I2C_SDA: Serial Data Input/Output In I2C mode, this pin is used as the input/output for the serial data. UART_TX: In UART mode, this pin is used as the transmit data (UART Transmit)

Table 1: Pin Description (Continued)

Pin No.	Name	I/O	Type	Description
JTAG (per IEEE 1149.1)				
F1	TMS	I pull-up	CMOS	TMS: JTAG Test Mode Select The signal on this pin controls the JTAG test performance and is sampled on the rising edge of TCK.
K3	TRSTB	I pull-up	CMOS	TRSTB: JTAG Test Reset (Active Low) A low signal on this pin resets the JTAG test port. This pin should be connected to ground when JTAG is not used.
G1	TCK	I pull-down	CMOS	TCK: JTAG Test Clock The clock for the JTAG test is input on this pin. TDI and TMS are sampled on the rising edge of TCK and TDO is updated on the falling edge of TCK. If TCK is idle at a low level, all stored-state devices contained in the test logic will indefinitely retain their state.
L3	TDI	I pull-up	CMOS	TDI: JTAG Test Data Input The test data are input on this pin. They are clocked into the device on the rising edge of TCK.
L5	TDO	O tri-state	CMOS	TDO: JTAG Test Data Output The test data are output on this pin. They are clocked out of the device on the falling edge of TCK. TDO pin outputs a high impedance signal except during the process of data scanning.
Power & Ground				
C1, C6, C7, D2, F2, F9, G2, H2, K1, K2	VDDA	Power	-	VDDA: Analog Core Power - +3.3V DC nominal
A5, A7, B2, B3, L4, M4	VDDAO	Power		VDDAO: Analog Output Power - +3.3V DC nominal
E4, E6, L7, M8	VDDDO	Power		VDDDO: Digital Output Power - +3.3V DC nominal
D5,F7	VDDD	Power		VDDD: Digital Core Power - +3.3V DC nominal
L10, H12	VDDD_1_8	Power		VDDD_1_8: Digital Core Power - +1.8V DC nominal
B9, C2, D1, D6, D7, E2, E8, F3, F8, H3, L1, L2	VSSA	Ground	-	VSSA: Ground
B1, B4, B5, B7, K4, M3	VSSAO	Ground		VSSAO: Ground
E7, F4, K7, M7	VSSDO	Ground		VSSDO: Ground
D4, F6, H11, L9	VSSD	Ground		VSSD: Ground
D3	VSSCOM	Ground	-	VSSCOM: Ground
C3, F5, G4, G5, G6, G8, H4, H5, H6, H7, H8, J3, J4, J5, J6, J7, J8	VSS	Ground	-	VSS: Ground
Other				
A1, A2, A3, A4, A10, A12, B10, B12, E3, G3, G7, L6	IC	-	-	IC: Internal Connection Internal Use. This pin must be left open for normal operation.

2.1 RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

2.1.1 INPUTS

Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Single-Ended Clock Inputs

For protection, unused single-ended clock inputs should be tied to ground.

Differential Clock Inputs

For applications not requiring the use of a differential input, both *_POS and *_NEG can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from _POS to ground.

PACKAGE DIMENSIONS

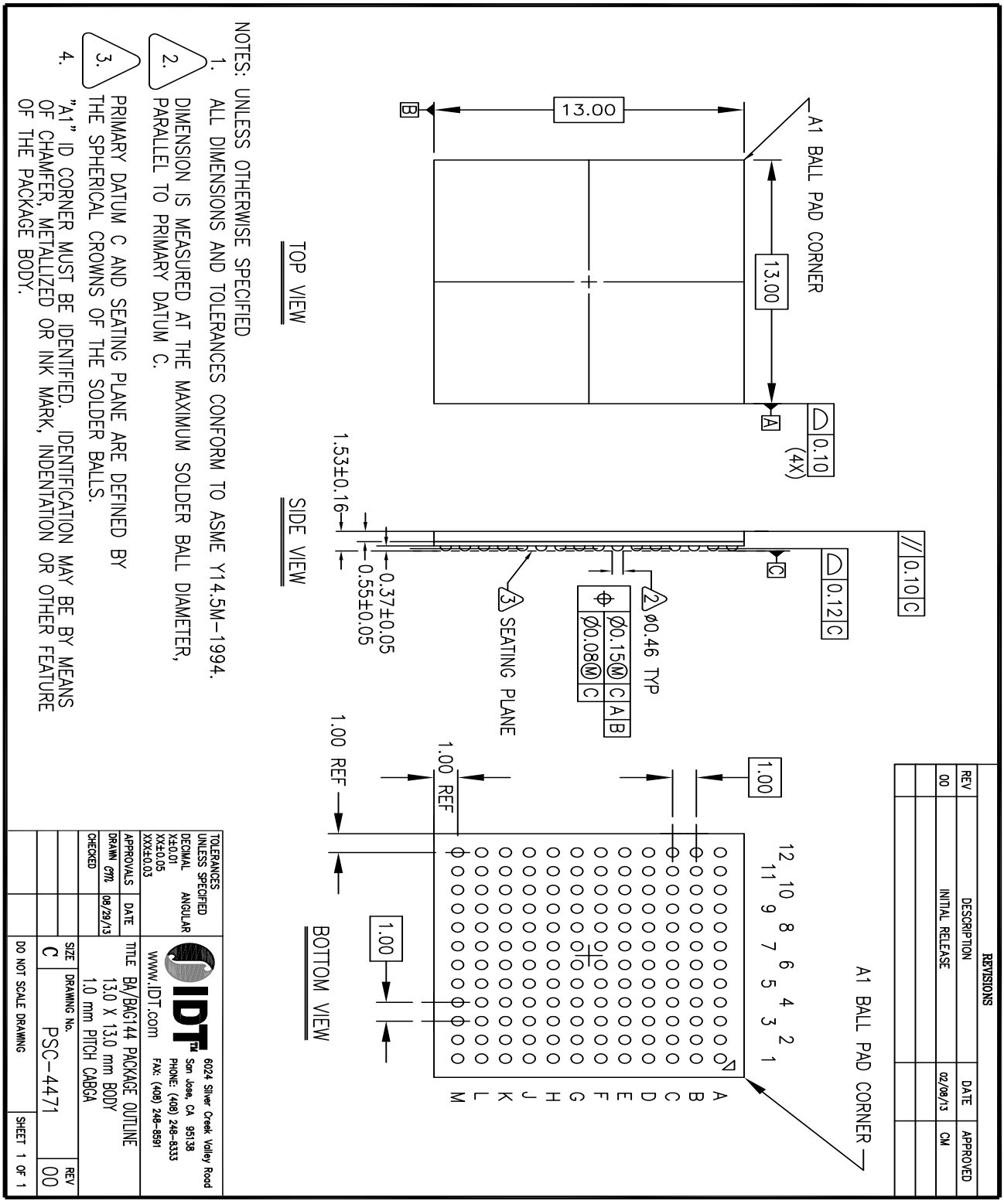

Figure 3. 144-Pin BAG Package Dimensions

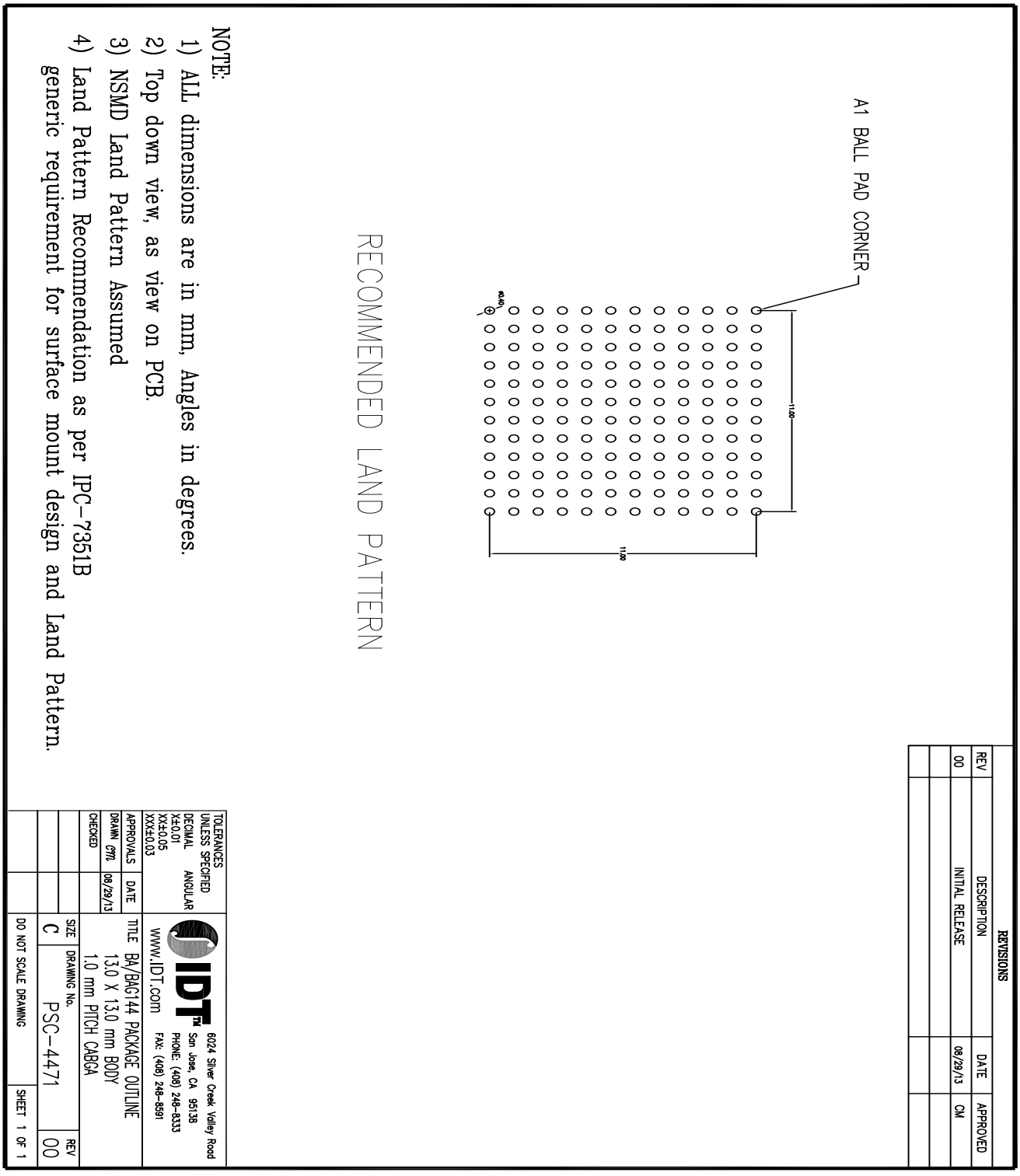

Figure 4. 144-Pin BAG Package Recommended Land Pattern

ORDERING INFORMATION

Table 2: Ordering Information

Part/Order Number	Package	Shipping Packaging	Temperature
82P33810ABAG	144-pin CABGA green package	Tray	-40° to +85°C
82P33810ABAG8	144-pin CABGA green package	Tape & Reel	-40° to +85°C

"G" after the two-letter package code denotes Pb-Free configuration, RoHS compliant.

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