

## Product Summary

Device	BV <sub>DSS</sub>	R <sub>DS(ON)</sub> Max	I <sub>D</sub> Max T <sub>C</sub> = +25°C (Note 10)
Q1 & Q2	30V	11.1mΩ @ V <sub>GS</sub> = 10V	30A
		13.8mΩ @ V <sub>GS</sub> = 4.5V	28A
		22.0mΩ @ V <sub>GS</sub> = 3.8V	22A

## Description

This new generation MOSFET is designed to minimize the on-state resistance (R<sub>DS(ON)</sub>), yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

## Applications

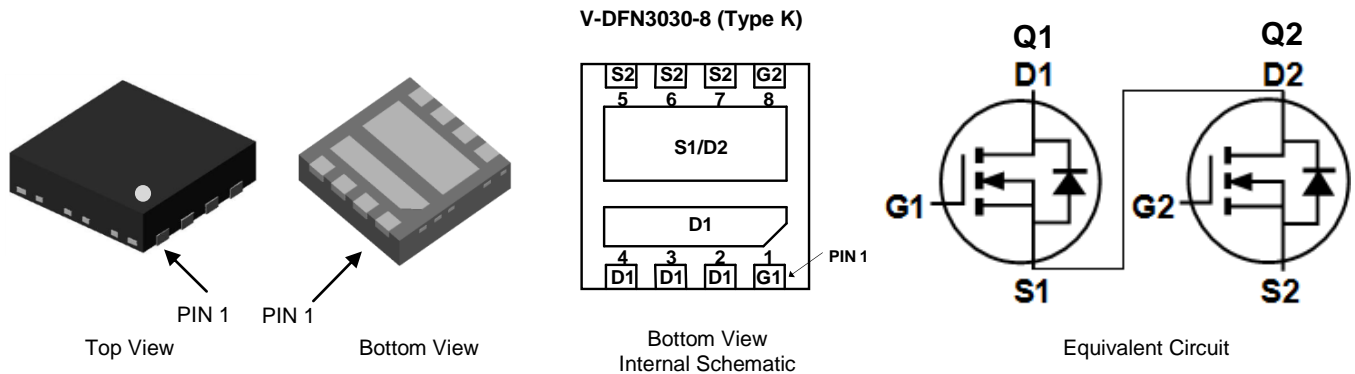
- General Purpose Interfacing Switch
- Power Management Functions

## Features and Benefits

- Low Gate Threshold Voltage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**

## Mechanical Data

- Case: V-DFN3030-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound.  
UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe.  
Solderable per MIL-STD-202, Method 208 <sup>(e4)</sup>
- Weight: 0.02 grams (Approximate)



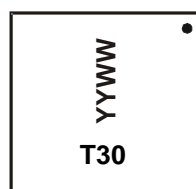
## Ordering Information (Note 4)

Part Number	Case	Tape Width	Tape Pitch	Packaging
DMT3009LDT-7	V-DFN3030-8 (Type K)	8mm	4mm	3,000/Tape & Reel
DMT3009LDT-7A	V-DFN3030-8 (Type K)	12mm	8mm	1,500/Tape & Reel

- Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
  2. See [http://www.diodes.com/quality/lead\\_free/](http://www.diodes.com/quality/lead_free/) for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
  3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
  4. For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

## Marking Information

### V-DFN3030-8 (Type K)



T30= Product Type Marking Code  
 YYWW = Date Code Marking  
 YY = Last Two Digits of Year (ex: 18 = 2018)  
 WW = Week Code (01 to 53)

**Maximum Ratings** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic			Symbol	Q1&Q2	Unit
Drain-Source Voltage			V <sub>DSS</sub>	30	V
Gate-Source Voltage			V <sub>GSS</sub>	+20, -16	V
Continuous Drain Current (Note 6) V <sub>GS</sub> = 10V	Steady State (Note 10)	T <sub>C</sub> = +25°C T <sub>C</sub> = +70°C	I <sub>D</sub>	30 25	A
	t < 10s	T <sub>A</sub> = +25°C T <sub>A</sub> = +70°C	I <sub>D</sub>	14 11	A
Maximum Body Diode Forward Current (Note 6)			I <sub>S</sub>	2.1	A
Pulsed Drain Current (100µs Pulse, Duty Cycle = 1%)			I <sub>DM</sub>	80	A
Pulsed Body Diode Forward Current (370µs Pulse, Duty Cycle = 1%)			I <sub>SM</sub>	80	A
Avalanche Current (Note 7) L = 0.1mH			I <sub>AS</sub>	19.3	A
Avalanche Energy (Note 7) L = 0.1mH			E <sub>AS</sub>	18.6	mJ

**Thermal Characteristics**

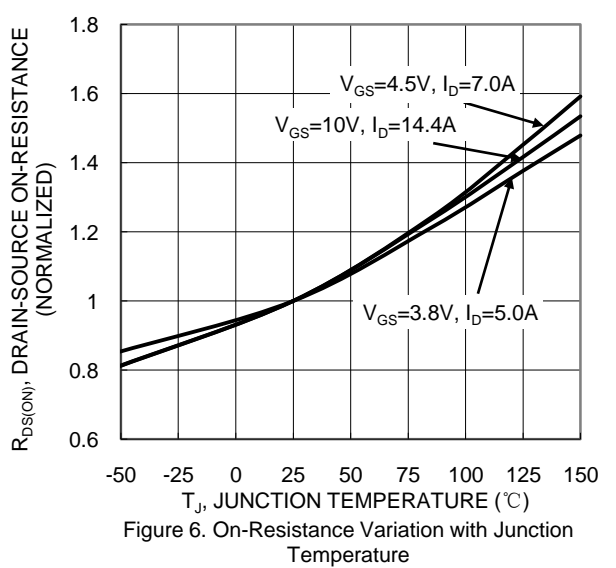
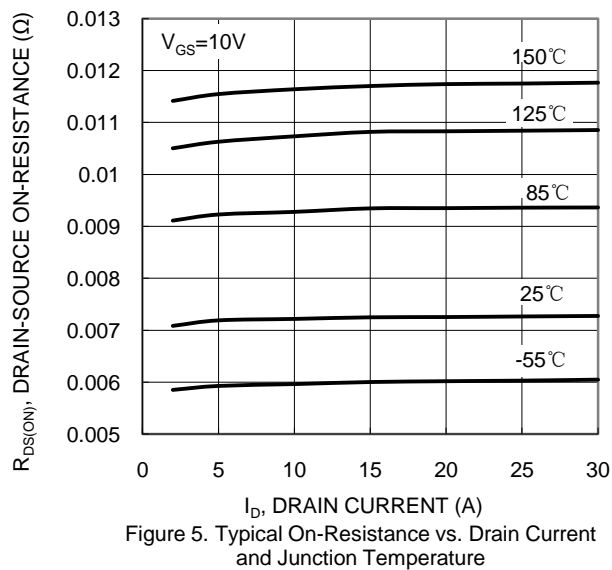
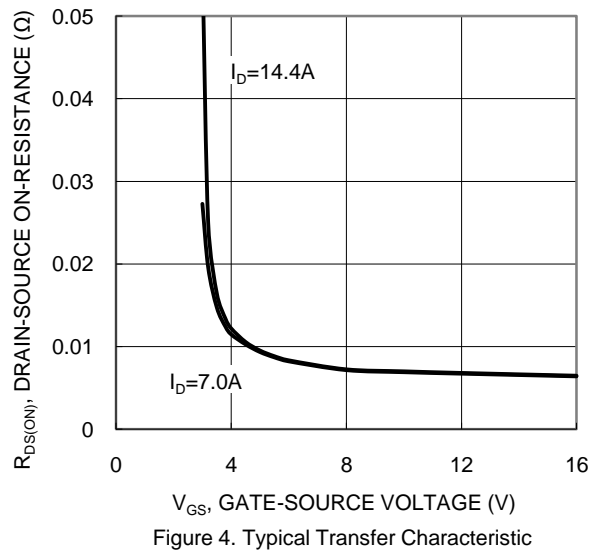
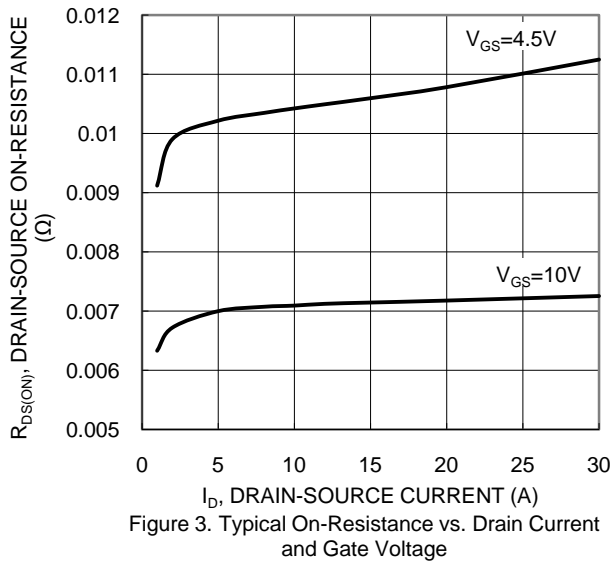
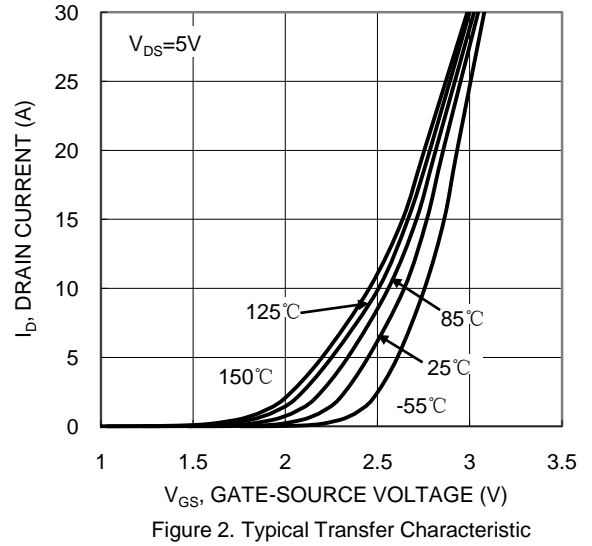
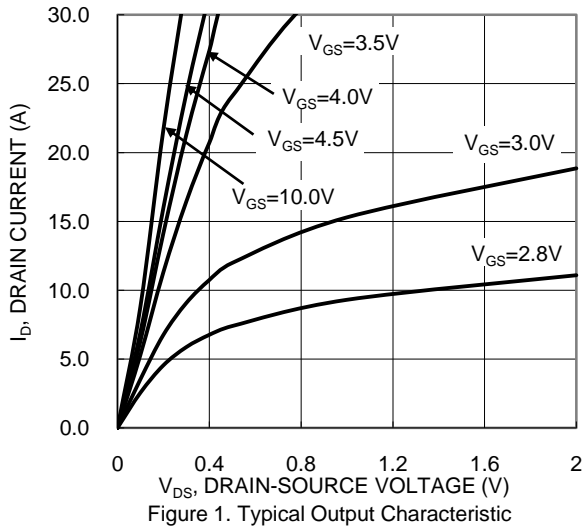
Characteristic		Symbol	Value	Unit
Total Power Dissipation (Note 5)	T <sub>A</sub> = +25°C	P <sub>D</sub>	1.2	W
	T <sub>A</sub> = +70°C		0.8	
Thermal Resistance, Junction to Ambient (Note 5)	Steady State	R <sub>θJA</sub>	107	°C/W
	t < 10s		63	
Total Power Dissipation (Note 6)	T <sub>A</sub> = +25°C	P <sub>D</sub>	2.0	W
	T <sub>A</sub> = +70°C		1.2	
Thermal Resistance, Junction to Ambient (Note 6)	Steady State	R <sub>θJA</sub>	64	°C/W
	t < 10s		39	
Thermal Resistance, Junction to Case (Note 6)		R <sub>θJC</sub>	7.6	
Operating and Storage Temperature Range		T <sub>J</sub> , T <sub>STG</sub>	-55 to +150	°C

- Notes:
5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
  6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1-inch square copper plate.
  7. UIS in production with L = 0.1mH, starting T<sub>A</sub> = +25°C.

**Electrical Characteristics** (@T<sub>A</sub> = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
<b>OFF CHARACTERISTICS</b> (Note 8)						
Drain-Source Breakdown Voltage	BV <sub>DSS</sub>	30	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	—	—	1	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
Zero Gate Voltage Drain Current T <sub>J</sub> = +150°C (Note 9)	I <sub>DSS</sub>	—	—	100	μA	V <sub>DS</sub> = 24V, V <sub>GS</sub> = 0V
Gate-Source Leakage	I <sub>GSS</sub>	—	—	±100	nA	V <sub>GS</sub> = 20V, V <sub>DS</sub> = 0V V <sub>GS</sub> = -16V, V <sub>DS</sub> = 0V
<b>ON CHARACTERISTICS</b> (Note 8)						
Gate Threshold Voltage	V <sub>GS(TH)</sub>	1	—	3	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
Static Drain-Source On-Resistance	R <sub>DS(ON)</sub>	—	7.2	11.1	mΩ	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14.4A
		—	10.5	13.8		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 7A
		—	13	22.0		V <sub>GS</sub> = 3.8V, I <sub>D</sub> = 5A
Diode Forward Voltage	V <sub>SD</sub>	—	—	1.2	V	V <sub>GS</sub> = 0V, I <sub>S</sub> = 10A
<b>DYNAMIC CHARACTERISTICS</b> (Note 9)						
Input Capacitance	C <sub>iSS</sub>	—	748	1,500	pF	V <sub>DS</sub> = 15V, V <sub>GS</sub> = 0V, f = 1.0MHz
Output Capacitance	C <sub>oSS</sub>	—	447	895		
Reverse Transfer Capacitance	C <sub>rSS</sub>	—	43	90		
Gate Resistance	R <sub>g</sub>	—	1.0	2.0	Ω	V <sub>DS</sub> = 0V, V <sub>GS</sub> = 0V, f = 1.0MHz
Total Gate Charge (V <sub>GS</sub> = 10V)	Q <sub>g</sub>	—	13.8	20	nC	V <sub>DS</sub> = 15V, I <sub>D</sub> = 14.4A
Total Gate Charge (V <sub>GS</sub> = 4.5V)	Q <sub>g</sub>	—	6.4	9		
Gate-Source Charge	Q <sub>gs</sub>	—	2.2	5		
Gate-Drain Charge	Q <sub>gd</sub>	—	2.2	5		
Turn-On Delay Time	t <sub>D(ON)</sub>	—	3.5	7	ns	V <sub>GS</sub> = 10V, V <sub>DD</sub> = 15V, R <sub>g</sub> = 1Ω, I <sub>D</sub> = 10A
Turn-On Rise Time	t <sub>r</sub>	—	5.0	10		
Turn-Off Delay Time	t <sub>D(OFF)</sub>	—	8.6	17		
Turn-Off Fall Time	t <sub>f</sub>	—	1.4	3		
Body Diode Reverse Recovery Time	t <sub>RR</sub>	—	18	33	ns	I <sub>F</sub> = 10A, di/dt = 100A/μs
Body Diode Reverse Recovery Charge	Q <sub>RR</sub>	—	7.7	15	nC	I <sub>F</sub> = 10A, di/dt = 100A/μs

- Notes: 8. Short duration pulse test used to minimize self-heating effect.  
9. Guaranteed by design. Not subject to product testing.  
10. Package limited.



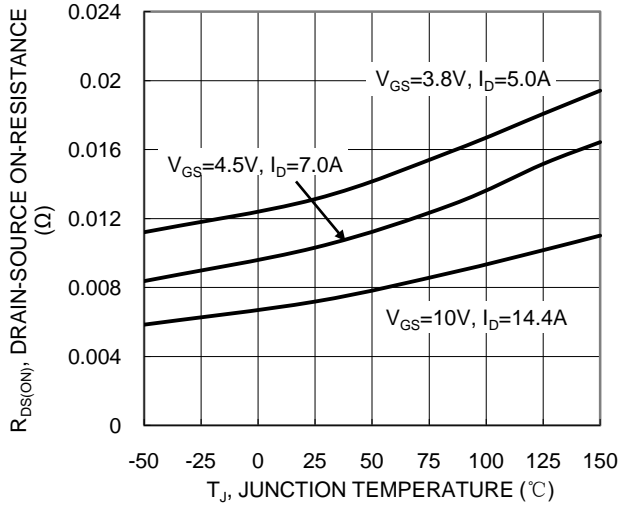


Figure 7. On-Resistance Variation with Junction Temperature

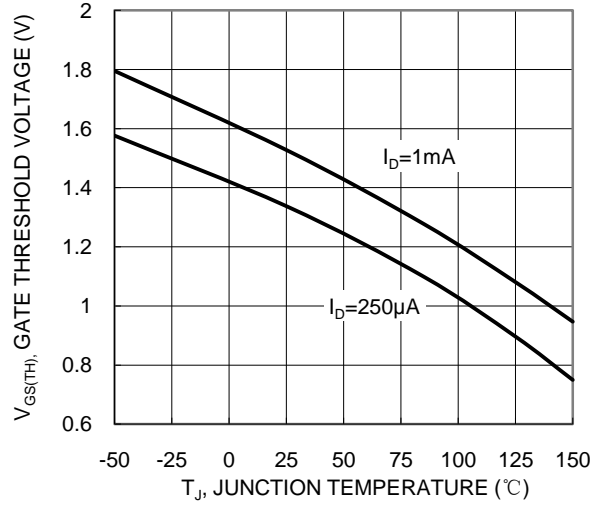


Figure 8. Gate Threshold Variation vs. Junction Temperature

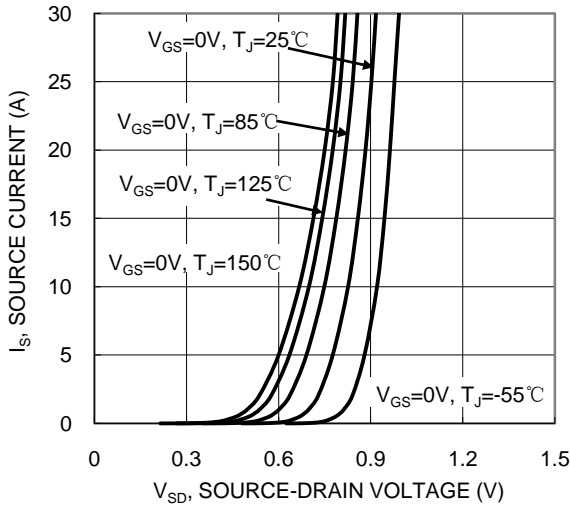


Figure 9. Diode Forward Voltage vs. Current

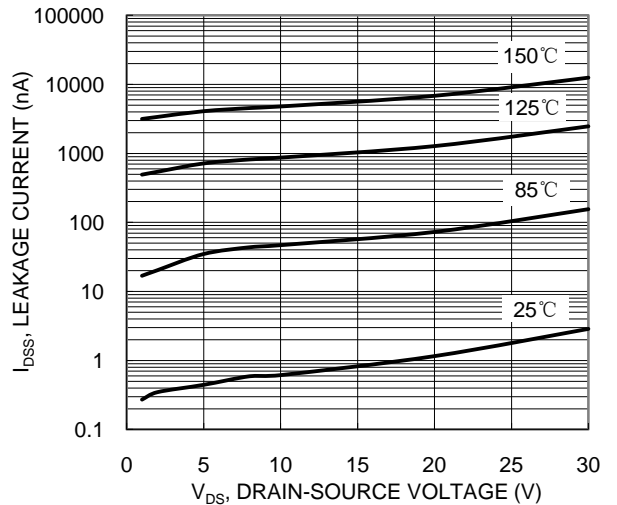


Figure 10. Typical Drain-Source Leakage Current vs. Voltage

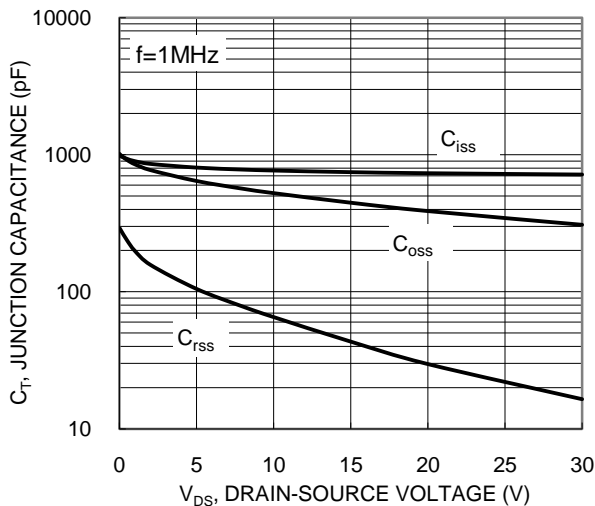


Figure 11. Typical Junction Capacitance

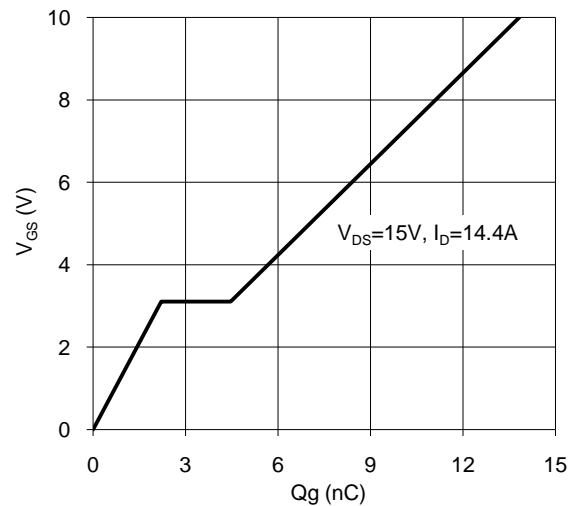


Figure 12. Gate Charge

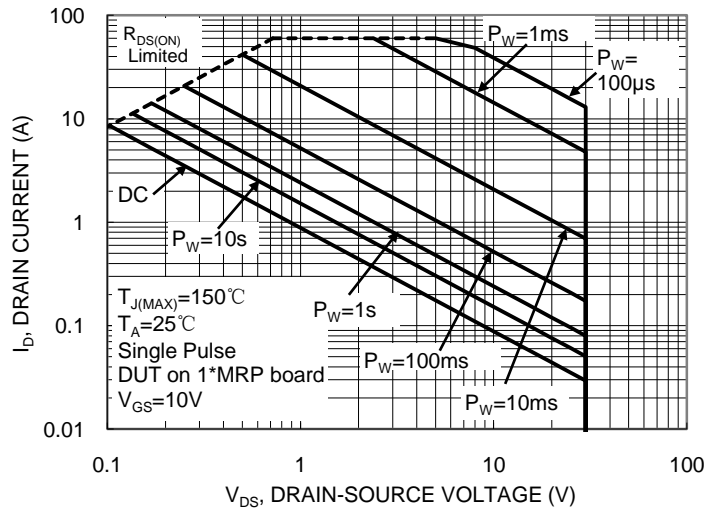


Figure 13. SOA, Safe Operation Area

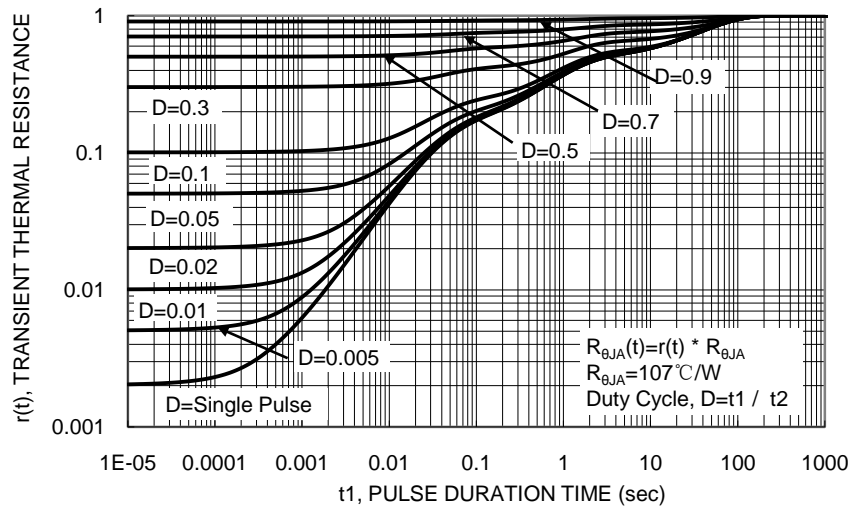
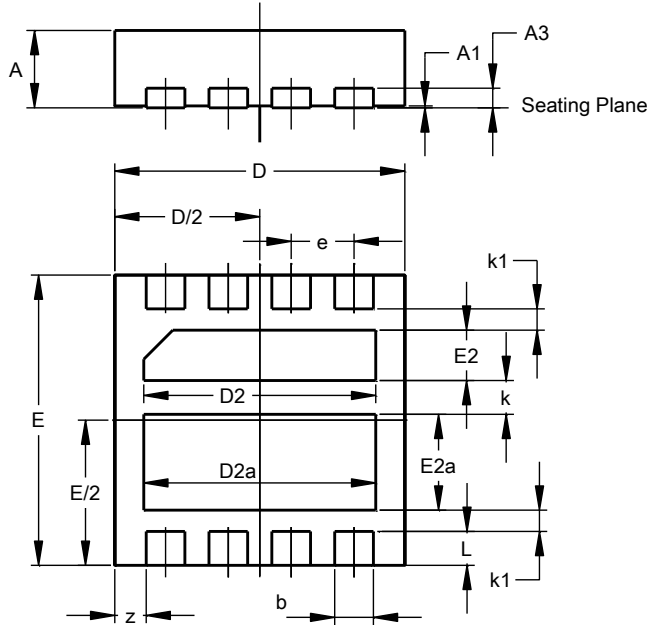


Figure 14. Transient Thermal Resistance

## Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3030-8 (Type K)

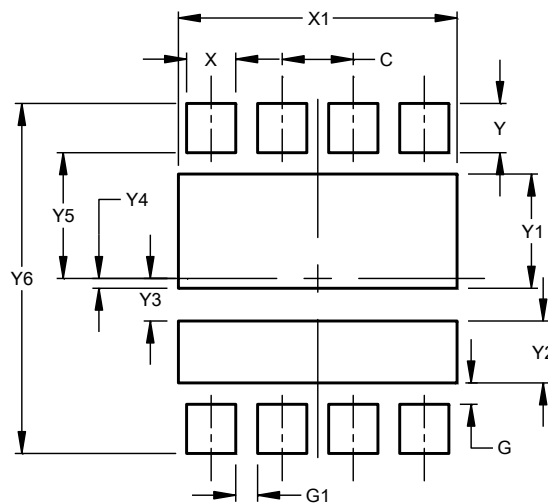


V-DFN3030-8 (Type K)			
Dim	Min	Max	Typ
A	0.77	0.85	0.80
A1	0.00	0.05	0.02
A3	0.20BSC		
b	0.35	0.45	0.40
D	2.95	3.050	3.00
D2	2.30	2.50	2.40
D2a	2.30	2.50	2.40
E	2.95	3.050	3.00
E2	0.42	0.62	0.52
E2a	0.89	1.09	0.99
e	0.65BSC		
k	-	-	0.35
k1	-	-	0.22
L	0.30	0.40	0.35
z	0.325BSC		
All Dimensions in mm			

## Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

V-DFN3030-8 (Type K)



Dimensions	Value (in mm)
C	0.650
G	0.195
G1	0.200
X	0.450
X1	2.550
Y	0.450
Y1	1.044
Y2	0.566
Y3	0.389
Y4	0.089
Y5	1.150
Y6	3.200

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