



40V N-CHANNEL ENHANCEMENT MODE MOSFET **POWERDI**

Product Summary

BV _{DSS}	R _{DS(ON)} max	I _D T _C = +25°C (Note 9)
40V	$1.8m\Omega$ @ $V_{GS} = 10V$	100A
	$3.1 \text{m}\Omega$ @ $V_{GS} = 4.5 \text{V}$	100A

Features

- 100% Unclamped Inductive Switching Ensures More Reliable and Robust End Application
- Thermally Efficient Package-Cooler Running Applications
- High Conversion Efficiency
- Low R_{DS(ON)} Minimizes On State Losses
- <1.1mm Package Profile Ideal for Thin Applications
- Lead-Free Finish; RoHS Compliant (Notes 1 & 2)
- Halogen and Antimony Free. "Green" Device (Note 3)

Description and Applications

This MOSFET has been designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

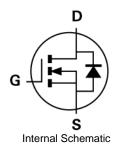
- **Engine Management Systems**
- **Body Control Electronics**
- **DC-DC Converters**

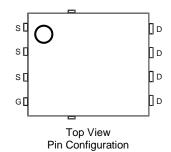
Mechanical Data

- Case: PowerDI5060-8 (Type K)
- Case Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminal Finish Matte Tin Annealed over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @3
- Weight: 0.097 grams (Approximate)



PowerDI5060-8 (Type K)





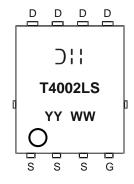
Ordering Information (Note 4)

Part Number	Case	Packaging
DMT4002LPS-13	PowerDI5060-8 (Type K)	2,500 / Tape & Reel

Notes:

- 1. EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant. All applicable RoHS exemptions applied.
- 2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green"
- 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- 4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information



T4002LS = Product Type Marking Code YYWW = Date Code Marking YY = Last Two Digits of Year (ex: 16 = 2016) WW = Week Code (01 to 53)



Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Value	Units	
Drain-Source Voltage	V_{DSS}	40	V	
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current, V _{GS} = 10V (Notes 6, 9)	$T_{C} = +25^{\circ}C$ $T_{C} = +70^{\circ}C$	I _D	100 100	А
Pulsed Drain Current (10µs pulse, duty cycle = 1%)		I _{DM}	200	Α
Continuous Body Diode Forward Current (Note 6)	T _C = +25°C	I _S	85	Α
Avalanche Current, L = 0.1mH		I _{AS}	48	Α
Avalanche Energy, L = 0.1mH		E _{AS}	115	mJ

Thermal Characteristics

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_{D}	2.3	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	55	°C/W
Total Power Dissipation (Note 6)	P_{D}	104	W
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	1.2	°C/W
Operating and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

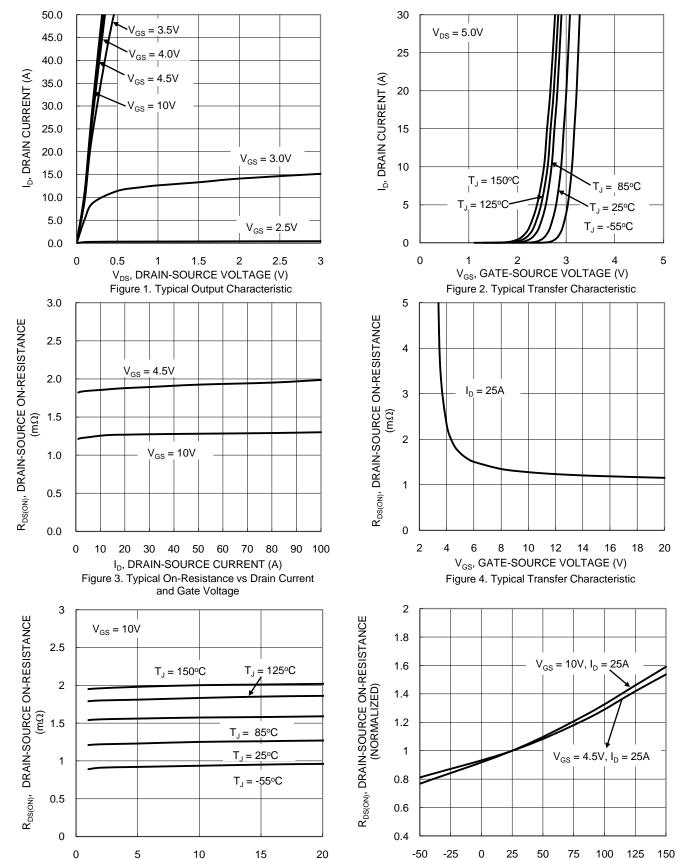
Characteristic	Symbol	Min	Тур	Max	Unit	Test Condition	
OFF CHARACTERISTICS (Note 7)							
Drain-Source Breakdown Voltage	BV _{DSS}	40	_	_	V	$V_{GS} = 0V, I_D = 250\mu A$	
Zero Gate Voltage Drain Current	I _{DSS}	_	_	1	μA	$V_{DS} = 32V$, $V_{GS} = 0V$	
Gate-Source Leakage	I _{GSS}	_	_	±100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$	
ON CHARACTERISTICS (Note 7)			l.	l .	l.	, ==	
Gate Threshold Voltage	V _{GS(TH)}	1	_	3	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$	
Static Drain-Source On-Resistance		_	1.3	1.8	mΩ	$V_{GS} = 10V, I_D = 25A$	
Static Drain-Source On-Resistance	R _{DS(ON)}	_	2	3.1	11177	$V_{GS} = 4.5V, I_D = 25A$	
Diode Forward Voltage	V_{SD}	_	_	1.2	V	$V_{GS} = 0V, I_{S} = 20A$	
DYNAMIC CHARACTERISTICS (Note 8)							
Input Capacitance	C _{iss}	_	6771	_		$V_{DS} = 20V$, $V_{GS} = 0V$, $f = 1MHz$	
Output Capacitance	Coss	_	2165	_	pF		
Reverse Transfer Capacitance	C_{rss}	_	176	_			
Gate Resistance	R _G	_	0.85	_	Ω	$V_{DS} = 0V$, $V_{GS} = 0V$, $f = 1MHz$	
Total Gate Charge (V _{GS} = 10V)	Q_{g}	-	116.1	_		V _{DD} = 20V, I _D = 25A, V _{GS} = 10V	
Total Gate Charge (V _{GS} = 4.5V)	Q_g	1	55.2	_	nC		
Gate-Source Charge	Q_{gs}	_	20.3	_	110		
Gate-Drain Charge	Q_{gd}	_	22.7	_			
Turn-On Delay Time	t _{D(ON)}	_	11.4	_		$V_{DD} = 20V, V_{GS} = 10V,$ $I_{D} = 25A, R_{G} = 3\Omega$	
Turn-On Rise Time	t _R	_	22.9	_			
Turn-Off Delay Time	t _{D(OFF)}	_	62.5	_	ns		
Turn-Off Fall Time	t _F	_	28	_			
Reverse Recovery Time	t _{RR}	_	58.6	_	ns	L_ 25A d:/dt 100A/us	
Reverse Recovery Charge	Q _{RR}	_	107	_	nC	I _F = 25A, di/dt = 100A/μs	

Notes:

- 5. Device mounted on FR-4 substrate PC board, 2oz copper, with thermal bias to bottom layer 1inch square copper plate.
- 6. Thermal resistance from junction to soldering point (on the exposed drain pad).
- 7. Short duration pulse test used to minimize self-heating effect.
- 8. Guaranteed by design. Not subject to product testing.
- 9. Package limited.







I_D, DRAIN CURRENT (A)

Figure 5. Typical On-Resistance vs Drain Current

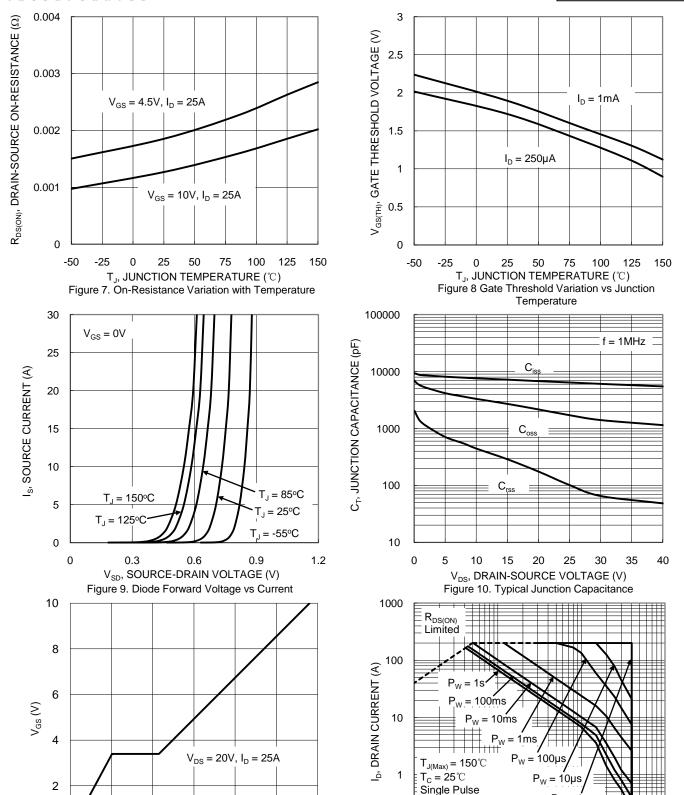
and Temperature

T_J, JUNCTION TEMPERATURE (°C)

Figure 6. On-Resistance Variation with Temperature







20

40

60

 Q_g (nC)

Figure 11. Gate Charge

80

100

120

0

0

100

 $= 1 \mu s$

10

V_{DS}, DRAIN-SOURCE VOLTAGE (V) Figure 12. SOA, Safe Operation Area

DUT on Infinite Heatsink

 $V_{GS} = 10V$

0.1

0.1



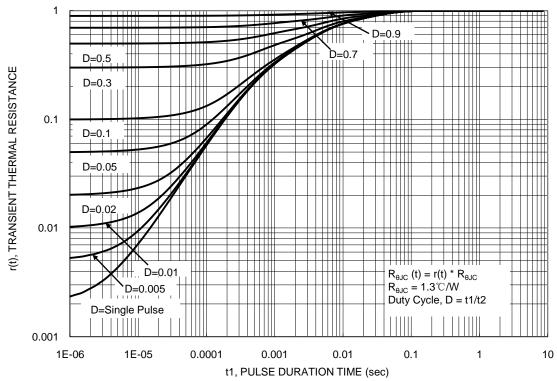


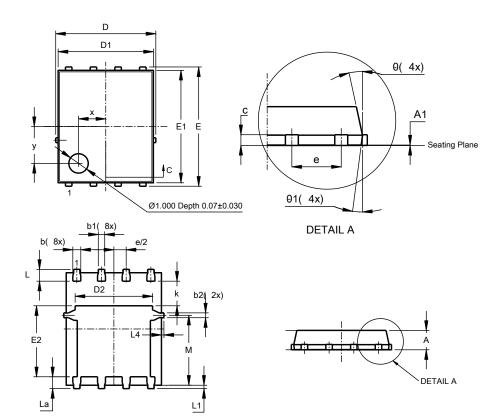
Figure 13. Transient Thermal Resistance



Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type K)

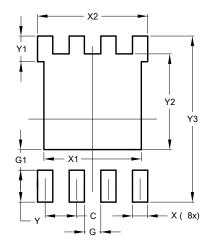


PowerDI5060-8 (Type K)					
Dim	Min	Max	Тур		
Α	0.90	1.10	1.00		
A1	0	0.05	0.02		
b	0.33	0.51	0.41		
b1	0.300	0.366	0.333		
b2	0.20	0.35	0.25		
С	0.23	0.33	0.277		
D	5	.15 BS0)		
D1	4.85	4.95	4.90		
D2	-	-	3.98		
E	6	.15 BS0	2		
E1	5.75	5.85	5.80		
E2	3.56	3.725	3.66		
E	1	.27BSC)		
k	-	-	1.27		
L	0.51	0.71	0.61		
La	0.51	0.675	0.61		
L1	0.05	0.20	0.175		
L4	-	-	0.125		
М	3.50	3.71	3.605		
X	-	-	1.400		
у	-	-	1.900		
θ	10°	12°	11°		
θ1	6°	8°	7°		
All Dimensions in mm					

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

PowerDI5060-8 (Type K)



Dimensions	Value (in mm)		
С	1.270		
G	0.660		
G1	0.820		
X	0.610		
X1	3.910		
X2	4.420		
Y	1.270		
Y1	1.020		
Y2	3.810		
Y3	6.610		



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