
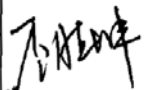
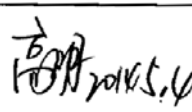



# Product Specification

**Product Name: VGM128128A4W13**

**Product Code: M0039F**

<b>Customer</b>
<b>Approved by Customer</b>
<b>Approved Date:</b>

Designed By	Checked By	Approved By	
		R&D	QA
 2014. 4. 23	 5.3/14	 2014.5.14	 5/4.14

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## 1 Overview

VGM128128A4W13 is a gray scale OLED display module with 128×128 dot matrix. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

## 2 Features

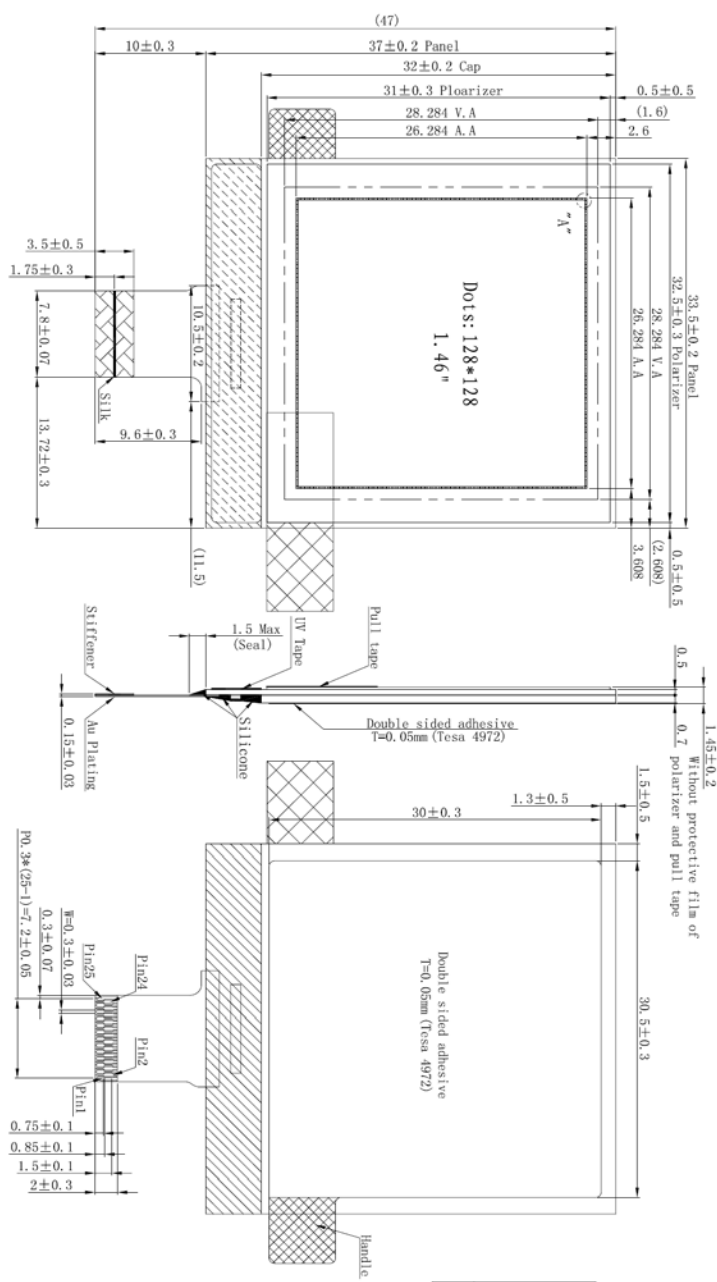
- Display Color: White
- Dot Matrix:128×128
- Driver IC: SSD1327Z
- Interface: 8-bit 8080,8-bit 6800,4-SPI,I<sup>2</sup>C
- Wide range of operating temperature: -40°C to 70°C

## 3 Mechanical Data

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W)×128(H)	-
2	Dot Size	0.1855(W)×0.1855(H)	mm <sup>2</sup>
3	Dot Pitch	0.2055(W)×0.2055(H)	mm <sup>2</sup>
4	Aperture Rate	81	%
5	Active Area	26.284(W)×26.284(H)	mm <sup>2</sup>
6	Panel Size	33.5(W) ×37.0(H) × 1.2(T)	mm <sup>3</sup>
7	Module Size	33.5(W) ×47.0(H) × 1.45(T)	mm <sup>3</sup>
8	Diagonal A/A Size	1.46	inch
9	Module Weight	3.25±10%	gram

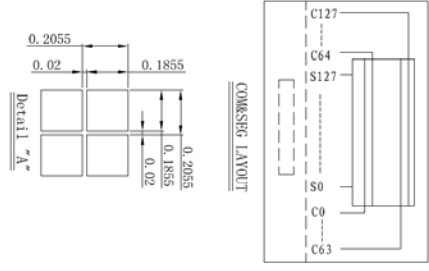
### 4 Mechanical Drawing

如本印章非红色, 则表明该文件为非受控版本, 不会受到控制和更新. 请使用受控文件.  
受控章  
分发号:



1. Display: OLED (White)
2. Format: 128\*128
3. Driver IC: SSD13272
4. General Tolerance: ±0.3
5. Operate Temp: -40° C ~ 70° C
6. Storage Temp: -40° C ~ 85° C
7. RoHS Compliant

Customer Approval Signature	Part Name Module Ass'y	Date 2014.04.09	Rev. 01	Unit mm	Sheet 1/1
Project Code Part No.	0039F 0039F-MA1-A	DES'D BY CHK'D BY	CHK'D BY	CHK'D BY	APPROVED



Rev.	Date	Note
1	2014.04.09	Based on 0039A; Modify the size of FPC
2		

## 5 Module Interface

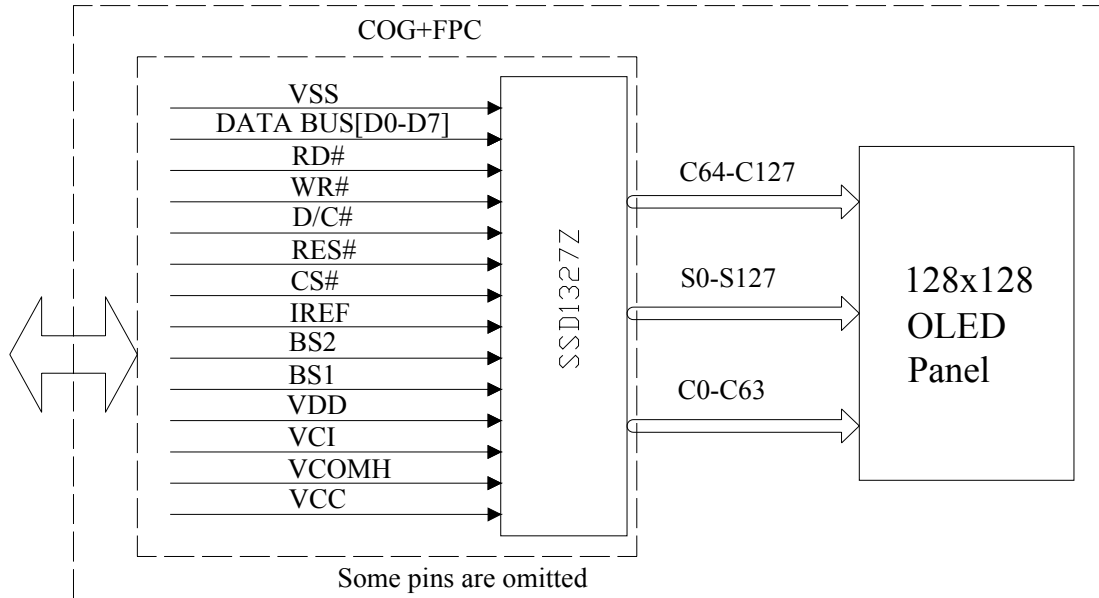
PIN NO.	PIN NAME	DESCRIPTION
1	VSS	Ground pin. It must be connected to external ground.
2	VCC	Power supply for panel driving voltage.
3	VCOMH	COM signal deselected voltage level. A capacitor should be connected between this pin and Vss. No external power supply is allowed to connect to this pin.
4	GPIO	It is a GPIO pin. Details refer to command B5h.
5	VCI	VCI must always set to be equivalent to or higher than VDD.
6	VDD	Power supply pin for core logic operation.
7	BS1	MCU bus interface selection pins. Table 5-1
8	BS2	
9	VSS	Ground pin. It must be connected to external ground.
10	IREF	This pin is the segment output current reference pin. A resistor should be connected between this pin and VSS to maintain the current around 10uA.
11	CS#	This pin is the chip select input connecting to the MCU.
12	RES#	This pin is reset signal input.
13	D/C#	This pin is Data/Command control pin connecting to the MCU.
14	WR#	This pin is read/write control input pin connecting to the MCU Interface. When 6800 interface mode is selected, this pin will be used as Read/Write (R/W#) Selection input. Read mode will be carried out when this pin is pulled HIGH and Write mode when LOW. When 8080 interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I <sup>2</sup> C interface is selected, this pin must be connected to Vss.
15	RD#	This pin is MCU interface input. When 6800 interface mode is selected, this pin will be used as the Enable(E) signal. Read/write operation is initiated when this pin is pulled HIGH and the chip is selected. When 8080 interface mode is selected, this pin receives the Read (RD#) signal. Read Operation is initiated when this pin is pulled LOW and the chip is selected. When serial or I <sup>2</sup> C interface is selected, this pin must be connected to Vss.
16	D7	These pins are bi-directional data bus connecting to the MCU data bus. Unused pins are recommended to tie LOW. When serial interface mode is selected, D0 will be the serial clock input: SCLK; D1 Will be the serial data input: SDIN and D2 should be kept NC. When I <sup>2</sup> C mode is selected, D2, D1 should be tied together and serve as SDAout, SDAin in application and D0 is the serial clock input, SCL.
17	D6	
18	D5	
19	D4	
20	D3	
21	D2	
22	D1	
23	D0	
24	NC	
25	NC	
		No Connection.

Table 5-1:

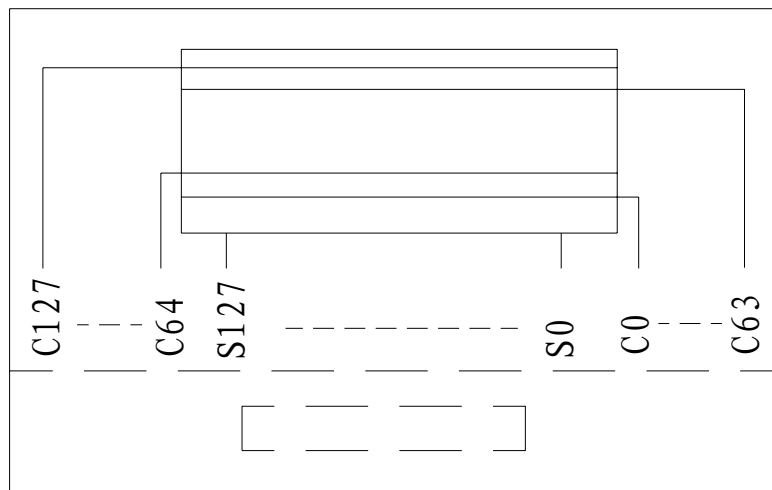
BS[2:1]	Interface
00	4 line SPI
01	I <sup>2</sup> C
10	8-bit 6800 parallel
11	8-bit 8080 parallel

## 6 Function Block Diagram

### 6.1 Function Block Diagram



### 6.2 Panel Layout Diagram



COM&SEG LAYOUT

## 7 Absolute Maximum Ratings

ITEM	SYMBOL	MIN	MAX	UNIT	REMARK
Supply voltage	VDD	-0.5	2.75	V	IC maximum rating
	VCC	-0.5	19.0	V	IC maximum rating
	VCI	-0.3	4.0	V	IC maximum rating
Operating Temp.	Top	-40	70	°C	-
Storage Temp	Tstg	-40	85	°C	-

Note (1): All of the voltages are on the basis of “VSS = 0V”.

Note (2): Permanent breakage of module may occur if the module is used beyond the maximum rating. The module can be normal operated under the conditions according to Section 8 “Electrical Characteristics”. Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the conditions.

## 8 Electrical Characteristics

### 8.1 DC Electrical Characteristics

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
Operating Voltage	VCC	-	14.5	15	15.5	V
Logic Supply Voltage	VDD	-	1.65	-	2.6	V
Low voltage power supply, power supply for I/O pins	VCI	-	1.65	3.0	3.5	V
High Logic Output Level	V <sub>OH</sub>	I <sub>out</sub> =100uA	0.9×VCI	-	VCI	V
Low Logic Output Level	V <sub>OL</sub>	I <sub>out</sub> =100uA	0	-	0.1×VCI	V
High Logic Input Level	V <sub>IH</sub>	-	0.8×VCI	-	VCI	V
Low Logic Input Level	V <sub>IL</sub>	-	0	-	0.2×VCI	V



**8.2 Electro-optical Characteristics**

ITEM	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT	REMARK	
Normal Mode Brightness	L <sub>br</sub>	All pixels ON	60	80	-	cd/m <sup>2</sup>	Note(1)	
VDD Sleep mode Current	ISLP_VDD	VCI=2.8V, VCC=OFF VDD(external)=2.5V, Display OFF, No panel attached	-	-	20	uA		
VCI Sleep mode Current	ISLP_VCI	VCI=2.8V, VCC=OFF, Display OFF, No panel attached	External VDD=2.5V	-	-	20	uA	
			Enable Internal VDD during Sleep mode	-	80	120	uA	
			Disable Internal VDD during Sleep mode (Deep Sleep mode)	-	-	20	uA	
VCC Sleep mode Current	ISLP_VCC	VCI=2.8V, VCC=8-18V VCC(external)=2.5V, Display OFF, No panel attached	-	-	20	uA		
Normal Mode Power Consumption	Pt	All pixels ON	-	555	675	mW	Note(1)	
C.I.E(White)	(x)	x,y(CIE1931)	0.26	0.30	0.34	-		
	(y)		0.32	0.36	0.40	-		
Dark Room Contrast	CR	-	≥2000:1	-	-	-		
Response Time	-	-	---	10	-	us		
View Angle	-	-	≥160	-	-	Degree		

**Note(1) Normal Mode test conditions are as follows:**

- Driving voltage : 15V
- Contrast setting : 0x80
- Frame rate : 100Hz
- Duty setting : 1/128

### 8.3 AC Electrical Characteristics

#### (1)8080-series MCU Parallel Interface Timing characteristics

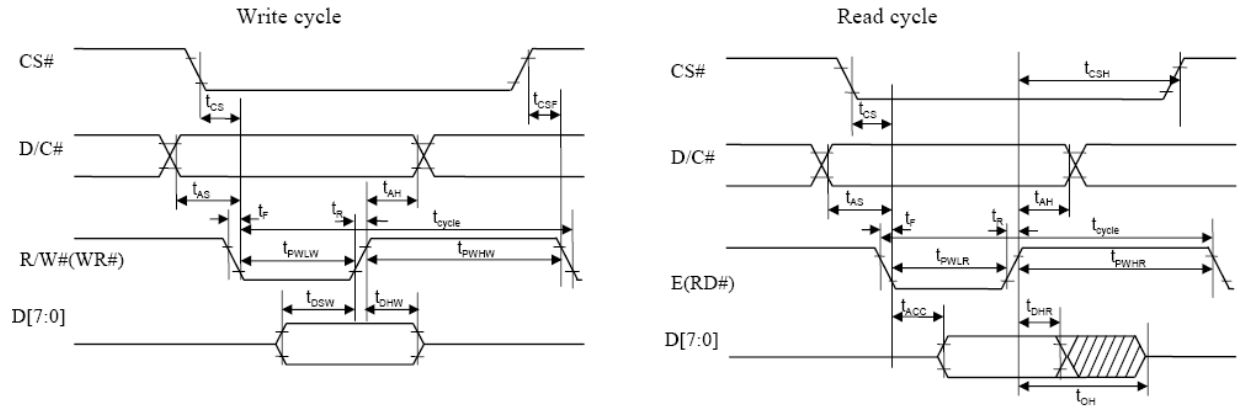
 $V_{CI} - V_{SS} = 1.65V \text{ to } 2.1V (T_A = 25^\circ C)$ 

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	30	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	20	-	-	ns
$t_{DHW}$	Write Data Hold Time	42	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLR}$	Read Low Time	150	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHR}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

 $V_{CI} - V_{SS} = 2.1V \text{ to } 3.5V (T_A = 25^\circ C)$ 

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	18	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	14	-	-	ns
$t_{DHW}$	Write Data Hold Time	20	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$t_{PWLR}$	Read Low Time	150	-	-	ns
$t_{PWLW}$	Write Low Time	60	-	-	ns
$t_{PWHR}$	Read High Time	60	-	-	ns
$t_{PWHW}$	Write High Time	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns
$t_{CS}$	Chip select setup time	0	-	-	ns
$t_{CSH}$	Chip select hold time to read signal	0	-	-	ns
$t_{CSF}$	Chip select hold time	20	-	-	ns

8080-series MCU Parallel Interface characteristics



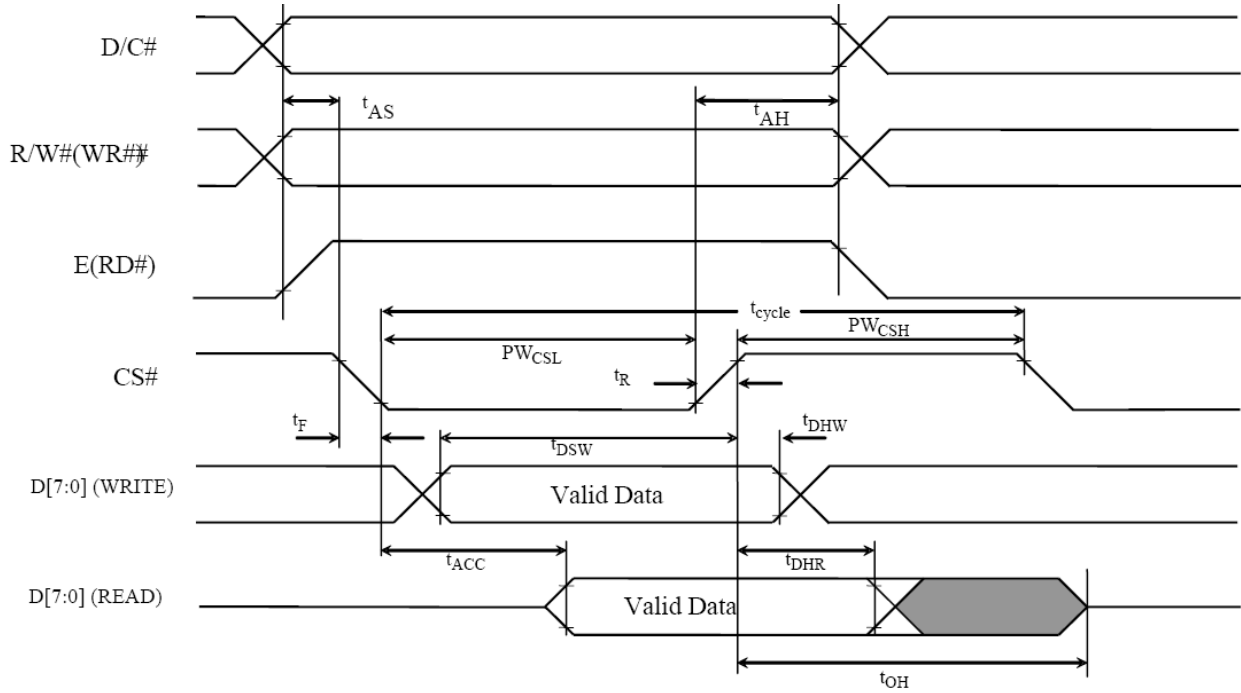
**(2)6800-seres MCU parallel interface Timing characteristics**
 $V_{CI} - V_{SS} = 1.65V \text{ to } 2.1V (T_A = 25^\circ C)$ 

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	44	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	250	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

 $V_{CI} - V_{SS} = 2.1V \text{ to } 3.5V (T_A = 25^\circ C)$ 

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	300	-	-	ns
$t_{AS}$	Address Setup Time	10	-	-	ns
$t_{AH}$	Address Hold Time	0	-	-	ns
$t_{DSW}$	Write Data Setup Time	40	-	-	ns
$t_{DHW}$	Write Data Hold Time	20	-	-	ns
$t_{DHR}$	Read Data Hold Time	20	-	-	ns
$t_{OH}$	Output Disable Time	-	-	70	ns
$t_{ACC}$	Access Time	-	-	140	ns
$PW_{CSL}$	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
$PW_{CSH}$	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

**6800-Series MCU Parallel Interface Timing Characteristics**



(3)Serial Interface Timing Characteristics (4-wire SPI)

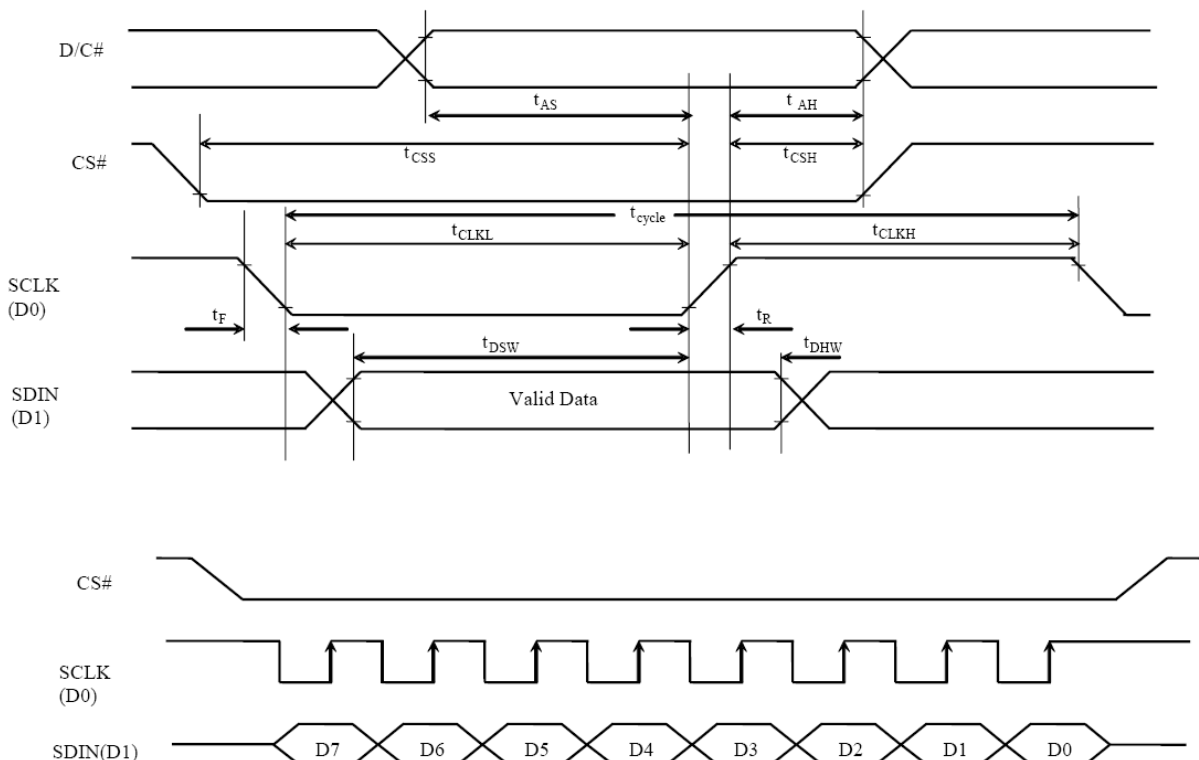
$V_{CI} - V_{SS} = 1.65V$  to  $2.1V$  ( $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	220	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	10	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	30	-	-	ns
$t_{CLKL}$	Clock Low Time	25	-	-	ns
$t_{CLKH}$	Clock High Time	20	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

$V_{CI} - V_{SS} = 2.1V$  to  $3.5V$  ( $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	160	-	-	ns
$t_{AS}$	Address Setup Time	15	-	-	ns
$t_{AH}$	Address Hold Time	15	-	-	ns
$t_{CSS}$	Chip Select Setup Time	20	-	-	ns
$t_{CSH}$	Chip Select Hold Time	10	-	-	ns
$t_{DSW}$	Write Data Setup Time	15	-	-	ns
$t_{DHW}$	Write Data Hold Time	15	-	-	ns
$t_{CLKL}$	Clock Low Time	20	-	-	ns
$t_{CLKH}$	Clock High Time	20	-	-	ns
$t_R$	Rise Time	-	-	15	ns
$t_F$	Fall Time	-	-	15	ns

Serial Interface characteristics (4-line SPI)

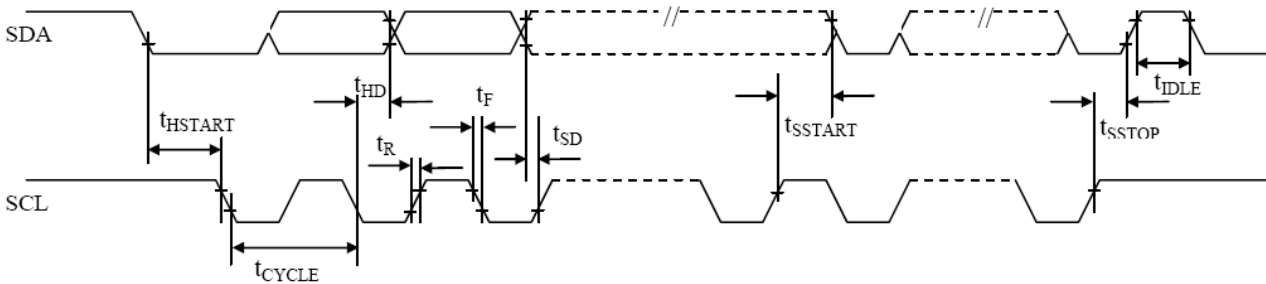


(4) I<sup>2</sup>C Interface Timing Characteristics

( $V_{CI} - V_{SS} = 1.65V$  to  $3.5V$ ,  $T_A = 25^\circ C$ )

Symbol	Parameter	Min	Typ	Max	Unit
$t_{cycle}$	Clock Cycle Time	2.5	-	-	$\mu s$
$t_{HSTART}$	Start condition Hold Time	0.6	-	-	$\mu s$
$t_{HD}$	Data Hold Time (for “SDA <sub>OUT</sub> ” pin)	0	-	-	ns
	Data Hold Time (for “SDA <sub>IN</sub> ” pin)	300	-	-	ns
$t_{SD}$	Data Setup Time	100	-	-	ns
$t_{SSTART}$	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	$\mu s$
$t_{SSTOP}$	Stop condition Setup Time	0.6	-	-	$\mu s$
$t_R$	Rise Time for data and clock pin	-	-	300	ns
$t_F$	Fall Time for data and clock pin	-	-	300	ns
$t_{IDLE}$	Idle Time before a new transmission can start	1.3	-	-	$\mu s$

I<sup>2</sup>C Interface Timing characteristics

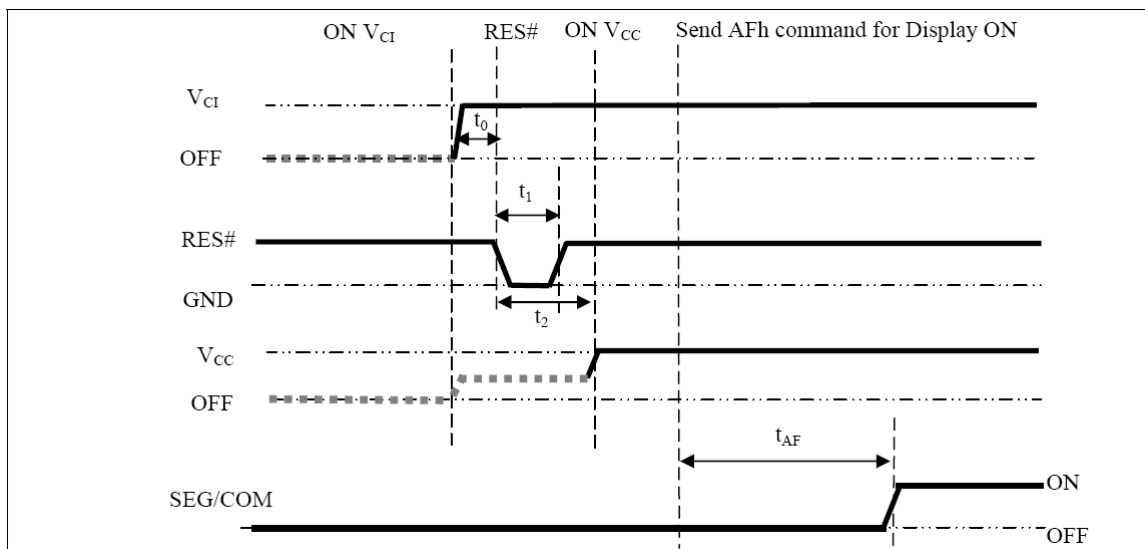


## 9 Functional Specification and Application Circuit

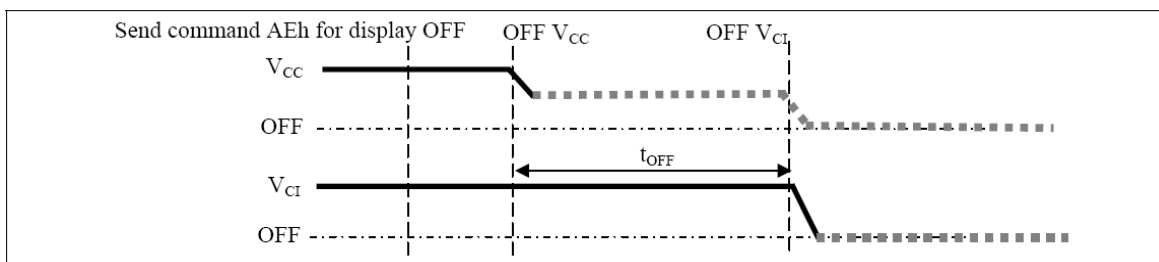
### 9.1 Power ON and Power OFF Sequence

The following figures illustrate the recommended power ON and power OFF sequence of SSD1327 (assume internal VDD is used)

1. Power ON VCI.
2. After VCI becomes stable, set wait time at least 1ms( $t_0$ ) for internal VDD become stable. Then set RES# pin LOW(logic low), for at least 100us( $t_1$ )(4) and then HIGH(logic high).
3. After set RES# pin LOW(logic low), wait for least 100us( $t_2$ ). Then Power ON VCC.(1)
4. After VCC become stable, send command AFh for display ON. SEG/COM will be ON after 200ms( $t_{AF}$ ).



1. Send command AEh for display OFF.
2. Power OFF VCC.(1),(2),(3)
3. Wait for  $t_{OFF}$ . Power OFF VCI (where Minimum  $t_{OFF}=0ms$ (5), Typical  $t_{OFF}=100ms$ )



Note:

- (1) Since an ESD protection circuit is connected between VCI and VCC, VCC becomes lower than VCI whenever VCI is ON and VCC is OFF as shown in the dotted line of VCC in above figures.
- (2) VCC should be kept float (disabled) when it is OFF.
- (3) Power pins(VCI, VCC) can never be pulled to ground under any circumstance.
- (4) The register values are reset after  $t_1$ .
- (5) VCI should not be Power OFF before VCC Power OFF.



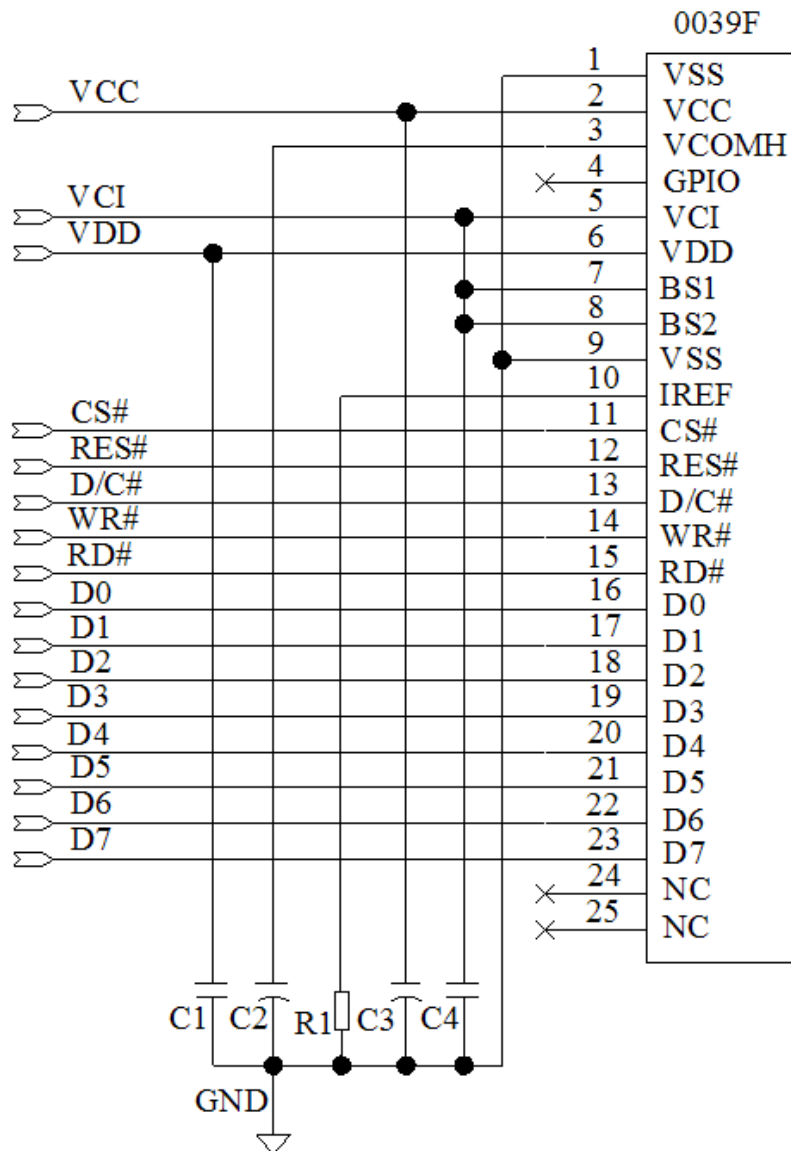
### 9.2 Application Circuit

The double byte command for 0xAB is used to enable or disable the VDD regulator.

No matter VDD is supplied by external source or internal regulated; VCI must always be set equivalent to or higher than VDD.

(A) .VDD can be supplied externally (with the range of 1.65V to 2.6V, VCI must always be set equivalent to or higher than VDD.) when A[0] is set to 0b.

(1).The configuration for 8-bit 8080-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0],RD#,WR#,D/C#,RES#,CS#

#### Recommended components

C1,C4: 0.1uF-0603-X7R±10%.RoHS

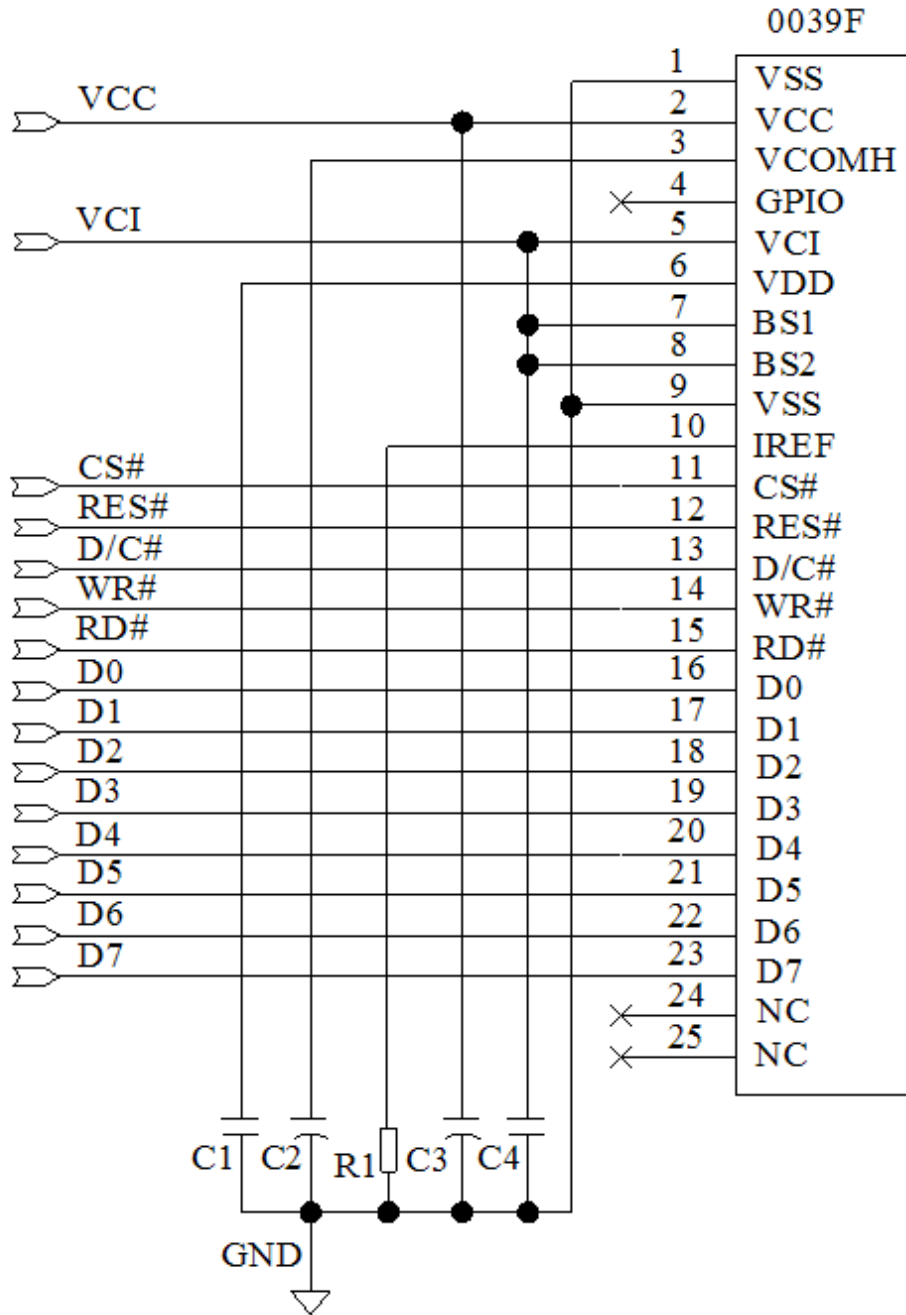
C2,C3: 4.7μF/25V.RoHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 1.2Mohm.RoHS

(B) .VDD can be supplied regulated internally from VCI when A[0] is set to 1b.

(VCI must be > 2.6V)

(1).The configuration for 8-bit 8080-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0],RD#,WR#,D/C#,RES#,CS#

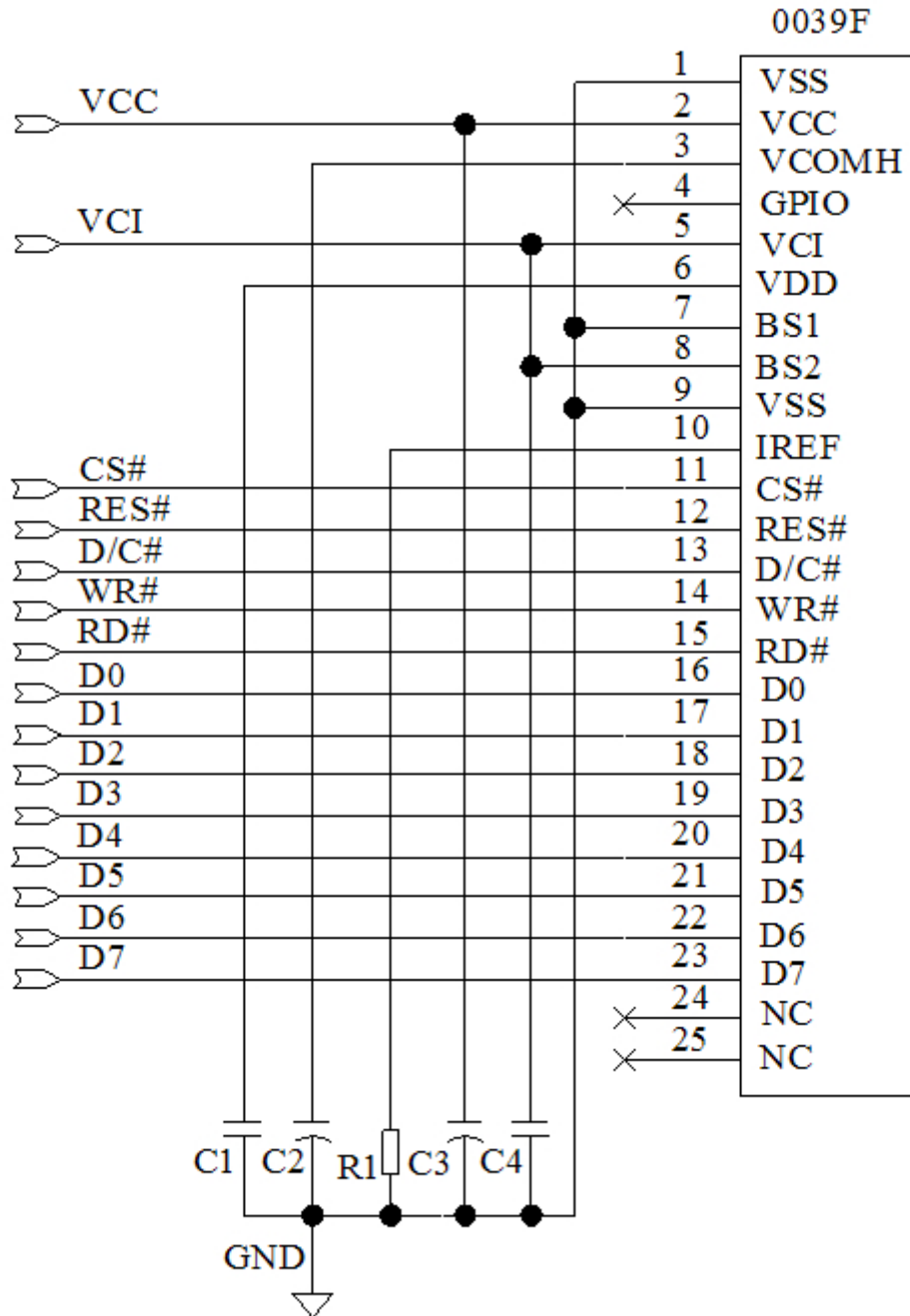
**Recommended components**

C1,C4: 0.1uF-0603-X7R±10%.RoHS

C2,C3: 4.7µF/25V.RoHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 1.2Mohm.RoHS

(2).The configuration for 8-bit 6800-parallel interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: D[7:0],RD#,WR#,D/C#,RES#,CS#

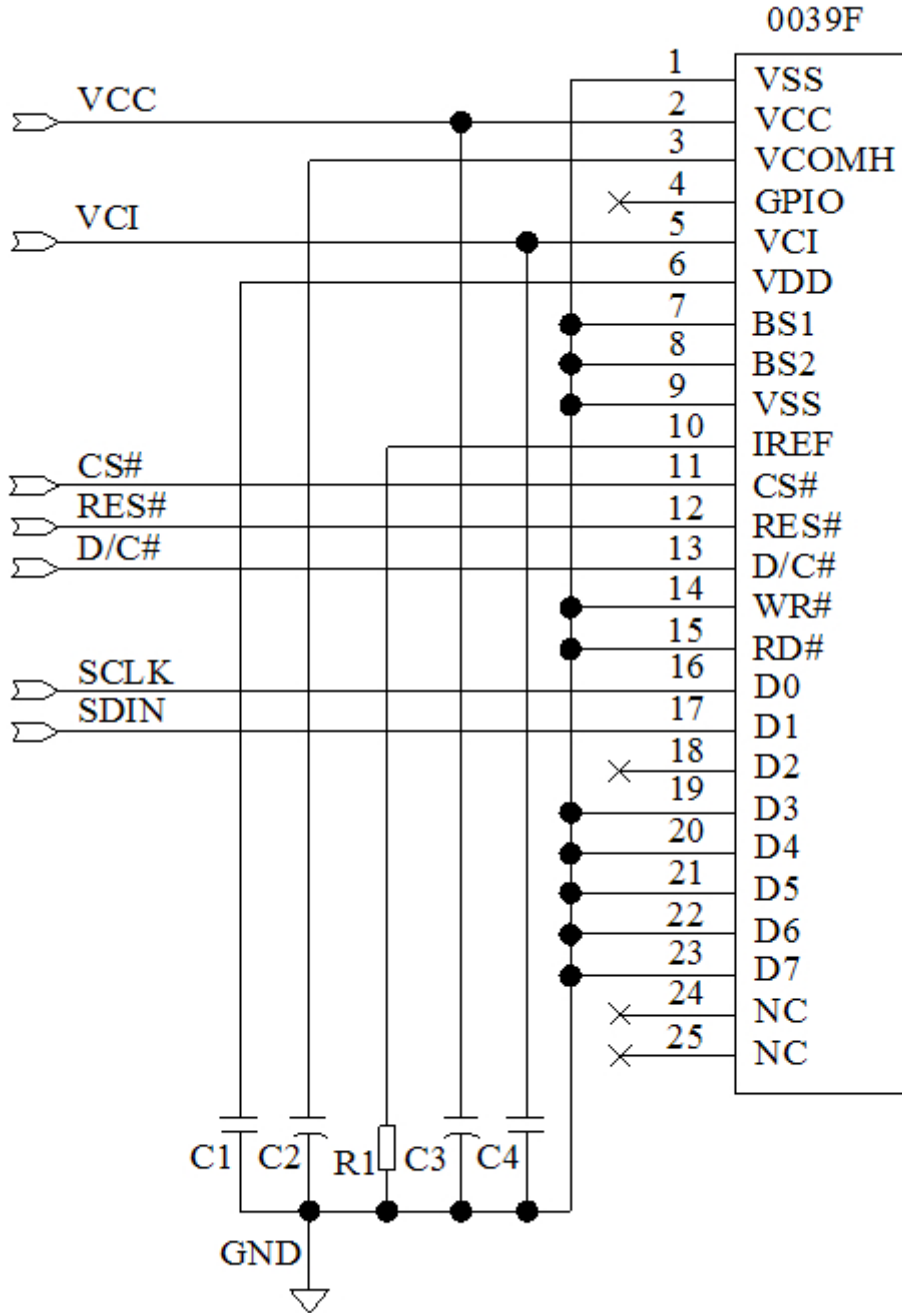
**Recommended components**

C1,C4: 0.1uF-0603-X7R±10%.RoHS

C2,C3: 4.7μF/25V.RoHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 1.2Mohm.RoHS

(3).The configuration for 4-wire SPI interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface: SDIN,SCLK,D/C#,RES#,CS#

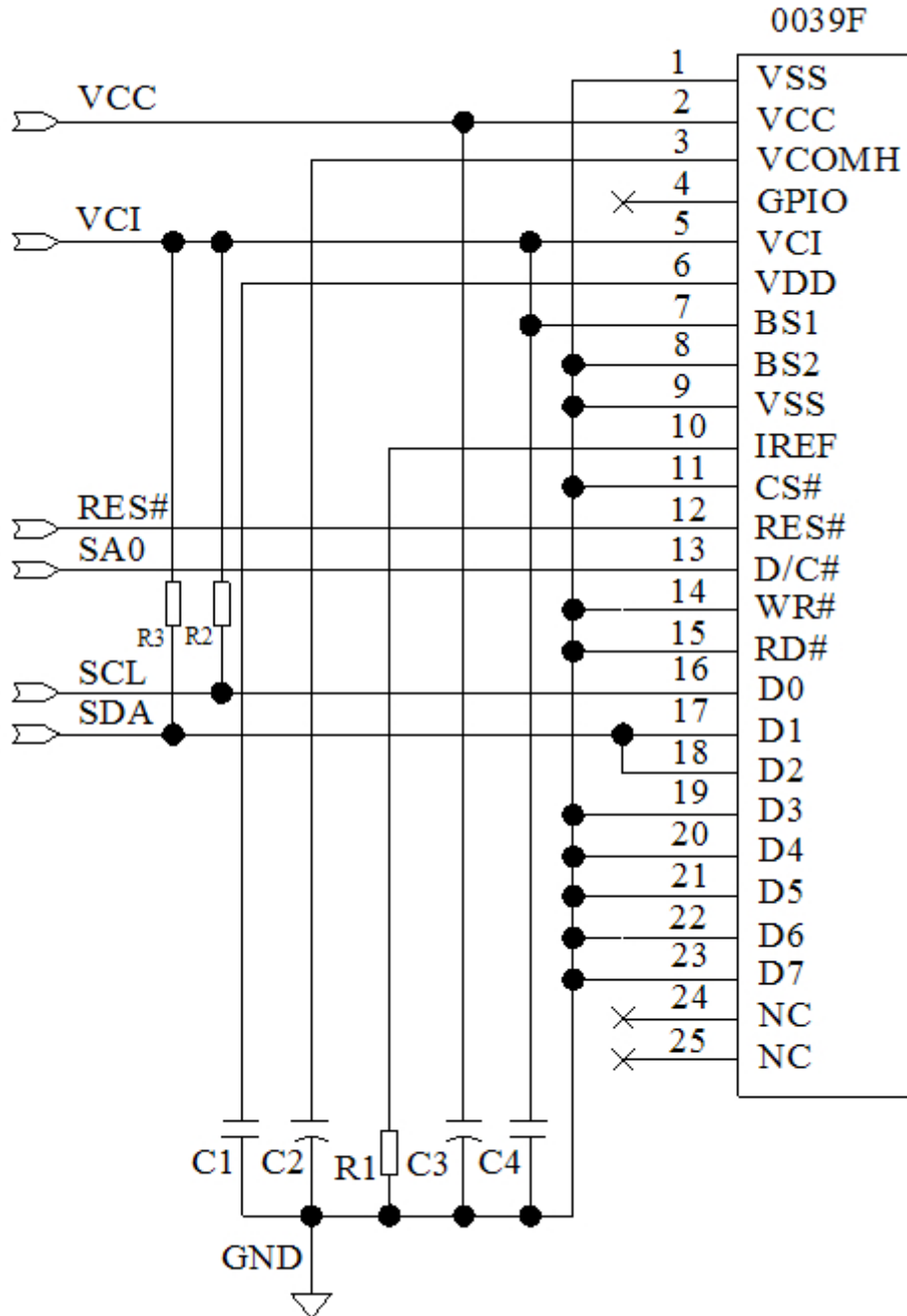
**Recommended components**

C1,C4: 0.1uF-0603-X7R±10%.RoHS

C2,C3: 4.7μF/25V.RoHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 1.2Mohm.RoHS

(4).The configuration for I<sup>2</sup>C interface mode, external VCC is shown in the following diagram:



Pin connected to MCU interface:SDA,SCL,SA0,RES#

**Recommended components**

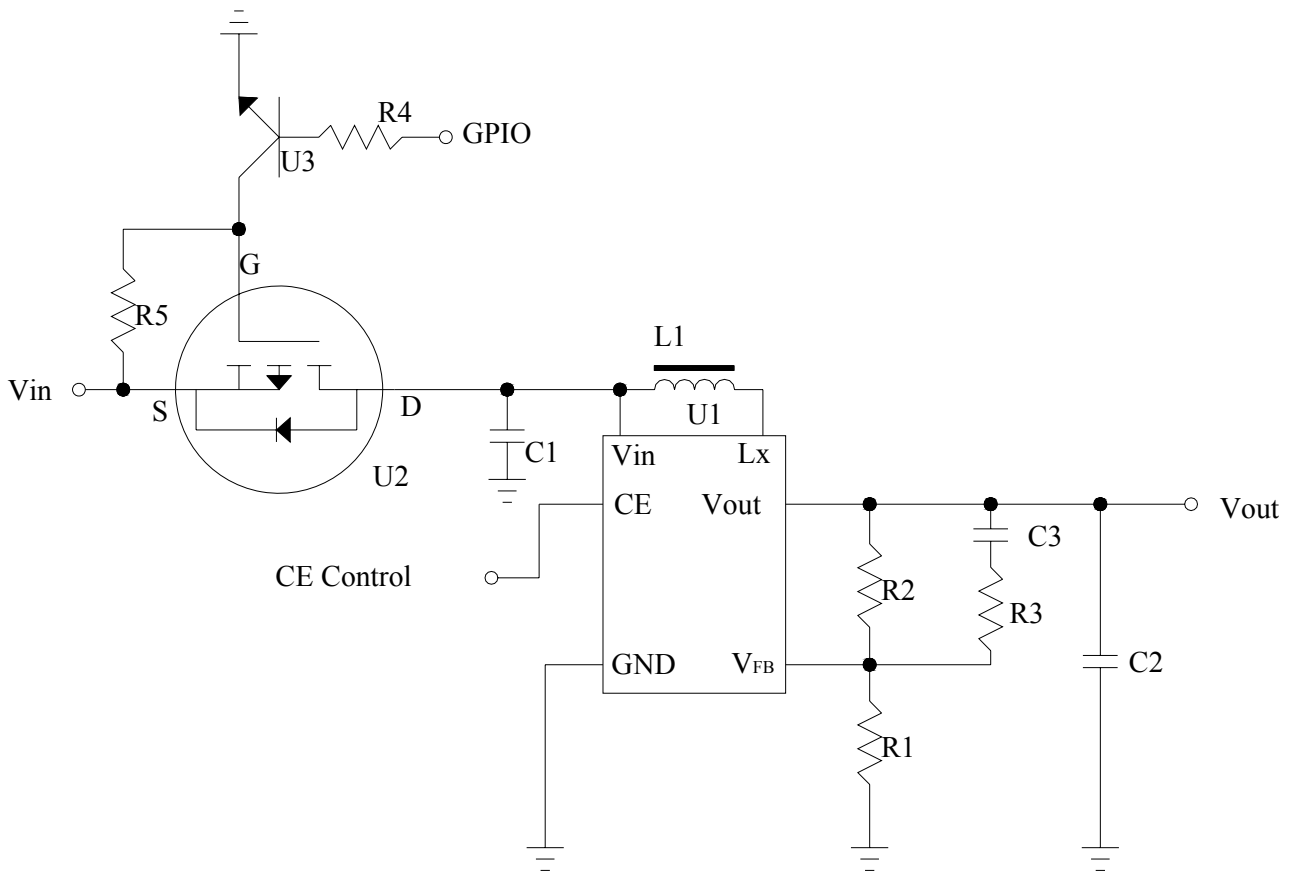
C1,C4: 0.1uF-0603-X7R±10%.RoHS

C2,C3: 4.7μF/25V.RoHS (Tantalum Capacitors)

R1: 0603 1/10W +/-5% 1.2Mohm.RoHS

R2,R3: 0603 1/10W +/-5% 10Kohm.RoHS

### 9.3 External DC-DC application circuit



#### Recommend component

The C1	: 1 uF-0603-X7R±10%.RoHS
The C2	: 1 uF-0603-X7R±10%.RoHS
The C3	: 220pF-0603-X7R±10%.RoHS
The R1	: 0603 1/10W +/-5% 10Kohm.RoHS
The R2	: 0603 1/10W +/-5% 140Kohm.RoHS
The R3	: 0603 1/10W +/-5% 2Kohm.RoHS
The R4	: 0603 1/10W +/-5% 1Kohm.RoHS
The R5	: 0603 1/10W +/-5% 10Kohm.RoHS
The L1	: 22uH
The U1	: R1200
The U2	: FDN338P
The U3	: 8050

## 9.4 Display Control Instruction

Refer to SSD1327Z IC Specification.

## 9.5 Recommended Software Initialization

In order to ensure the reliability and stability of the module, the module must initialized use the following code, Malfunctioning of the module may occur and the reliability of the module may deteriorate if the module is used beyond the initialize code.

```
void init_program()
{
    write_c(0xae);
    write_c(0x15);    // Set column address
    write_c(0x00);    // Start column    0
    write_c(0x3f);    // End column    127
    write_c(0x75);    // Set row address
    write_c(0x00);    //Start row    0
    write_c(0x7f);    //End row    127
    write_c(0x81);    //Set contrast control
    write_c(0x80);
    write_c(0xa0);    //Segment remap
    write_c(0x51);
    write_c(0xa1);    // Start line
    write_c(0x00);
    write_c(0xa2);    //Display offset
    write_c(0x00);
    write_c(0xa4);    //Normal display
    write_c(0xa8);    // Set multiplex ratio
    write_c(0x7f);
    write_c(0xb1);    //Set phase length
    write_c(0xf1);
    write_c(0xb3);    // Set dclk
    write_c(0x00);    //80Hz:0xc1  90Hz:0xe1  100Hz:0x00  110Hz:0x30
                    //120Hz:0x50  130Hz:0x70

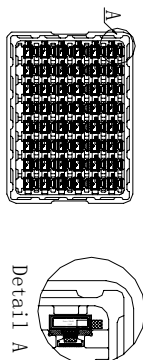
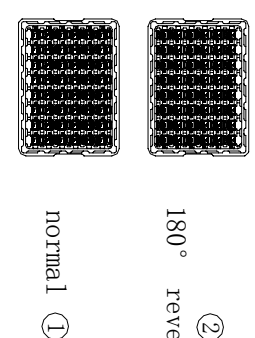
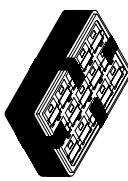
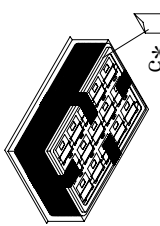
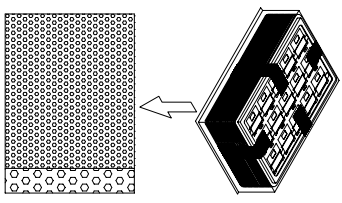
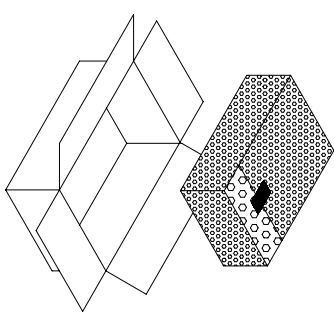
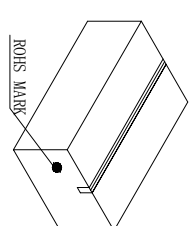
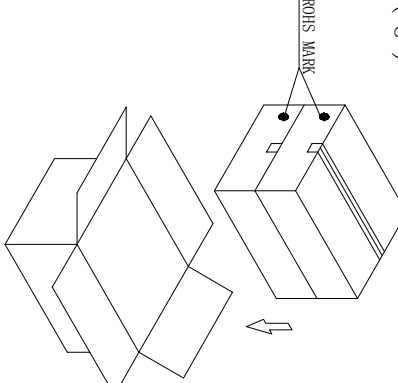
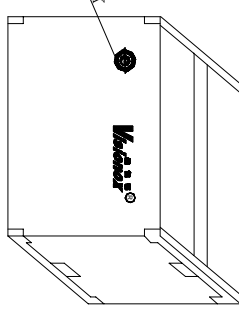

    write_c(0xab);
    write_c(0x01);
    write_c(0xb6);    // Set phase length
    write_c(0x0f);
    write_c(0xbe);
    write_c(0x0f);
    write_c(0xbc);
```

```
write_c(0x08);  
write_c(0xd5);  
write_c(0x62);  
write_c(0xfd);  
write_c(0x12);  
clear_screen();  
write_c(0xae);  
}
```



### 10 Package Specification

Controlled Seal  
Packing Process (1) ~ (9)

<p>( 1 ) Tray Type:00390-MT6-A</p> 	<p>( 2 )</p>  <p>TRAY normal ① 180° revers ②</p>	<p>( 3 ) order ①, ②, ①, ② fix trays with tape 500 pcs of 1 small carton 1 tray contain 30 pcs 17 contained trays, 1 empty tray quantity distribution:16*30+1*20</p>  <p>small carton package</p>	<p>( 4 ) Use vacuum bag to package the tray and add 5 bags of desiccant into the vacuum bag *5</p> 
<p>( 5 ) After tray be packaged, wrap the package in a bubble bag and seal with scotch tape.</p> 	<p>( 6 )</p> 	<p>( 7 )</p>  <p>ROHS MARK</p>	<p>( 8 )</p>  <p>ROHS MARK</p> <p>2 small cartons in 1 big carton</p>
<p>( 9 ) 34 contained trays, 2 empty trays, Package quantity products: 1000 pcs of 1 big carton</p>  <p>ROHS MARK</p> <p>Package finished L450*W350*L1352 mm</p>	<p>NOTE:1、The inner carton and master carton must be sealed with adhesive tape. 2、Fill up the gap with tray. 3、If the customer has special needs with the RoHS making, the inner carton and master carton need adhesive new RoHS marking at .</p>		

## 11 Reliability

### 11.1 Reliability Test

NO.	ITEM	CONDITION	QUANTITY
1	High Temperature (Non-operation)	85°C,240hrs	4
2	Low Temperature (Non-operation)	-40°C,240hrs	4
3	High Temperature (Operation)	70°C,240hrs	4
4	Low Temperature (Operation)	-40°C,240hrs	4
5	High Temperature / High Humidity (Operation)	60°C,90%RH,240hrs	4
6	Thermal shock (Non-operation)	-40°C~85°C (-40°C/30min;transit/3min;85°C/30min ;transit/3min) 1cycle: 66min,100 cycles	4
7	Vibration	Frequency: 5~50Hz,0.5G Scan rate: 1 oct/min Time: 2 hrs/axis Test axis: X,Y, Z	1 Carton
8	Drop	Height: 100 cm Sequence: 1 angle, 3 edges and 6 faces	1 Carton

#### Test and measurement conditions

- All measurements shall not be started until the specimens attain to temperature stability, the stable time is at least 15 minutes.
- The degradation of polarizer is ignored for item 5.
- The tolerance of temperature is  $\pm 3^{\circ}\text{C}$ , and the tolerance of relative humidity is  $\pm 5\%$ .

#### Evaluation criteria

- The function test is OK.
- No observable defects.
- Luminance:  $\geq 50\%$  of initial value.
- Current consumption: within  $\pm 50\%$  of initial value.

### 11.2 Lifetime

End of lifetime is specified as 50% of initial brightness and the test pattern at operating condition is 50% alternating checkerboard.

ITEM	MIN	MAX	UNIT	CONDITION
Operation Life Time	16,000	-	hrs	80 cd/m <sup>2</sup> , 50% alternating Checkerboard, 22 $\pm$ 3°C, 55 $\pm$ 15% RH

### 11.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 22 $\pm$ 3°C; 55 $\pm$ 15% RH.



### 13 Outgoing Quality Control Specifications

#### 13.1 Sampling Method

- (1) GB/T 2828.1-2003/ISO2859-1: 1999, inspection level II , normal inspection, single sample inspection
- (2) AQL: Major 0.65; Minor 1.0

#### 13.2 Inspection Conditions

The environmental conditions for test and measurement are performed as follows.

Temperature:  $22 \pm 3^{\circ}\text{C}$

Humidity:  $55 \pm 15\% \text{R.H}$

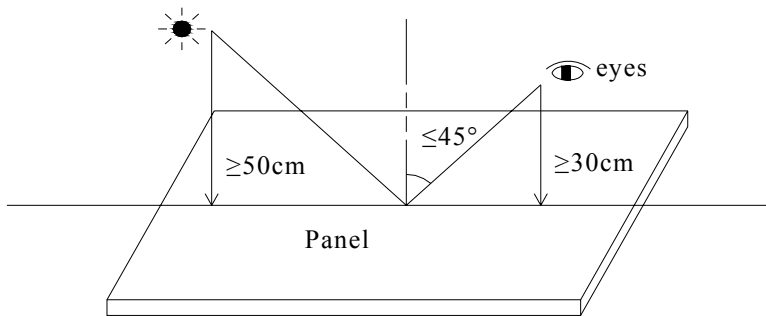
Fluorescent Lamp: 30W

Distance between the Panel & Lamp:  $\geq 50\text{cm}$

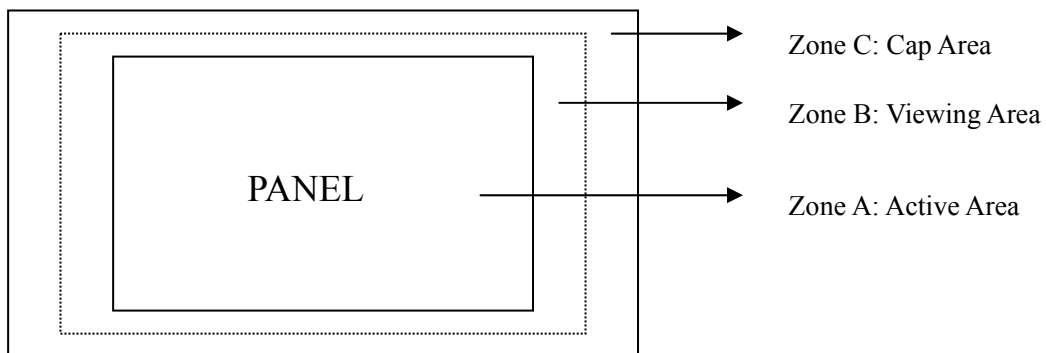
Distance between the Panel & Eyes:  $\geq 30\text{cm}$

Viewing angle from the vertical in each direction:  $\leq 45^{\circ}$

(See the sketch below)

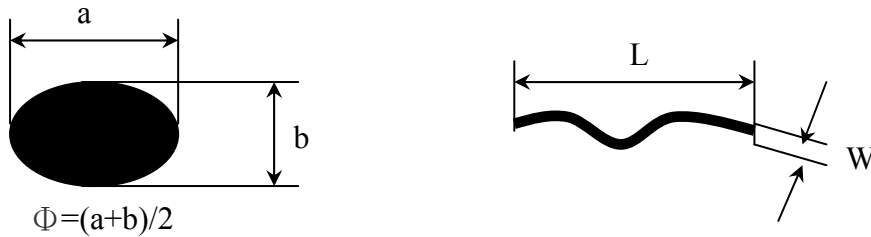


#### 13.3 Quality Assurance Zones



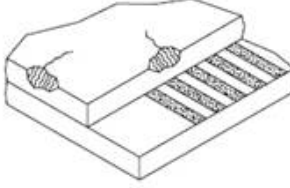
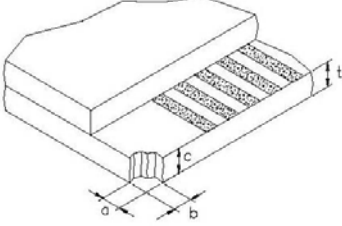
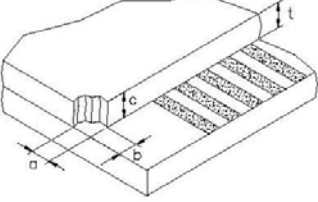
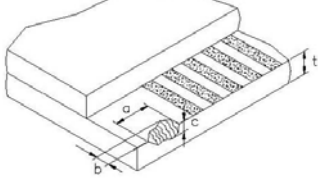
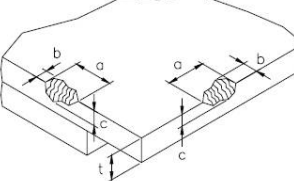
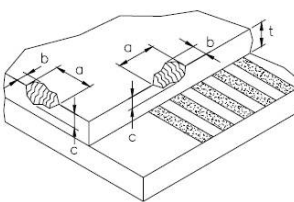
### 13.4 Inspection Standard

Definition of  $\Phi$ &L&W (Unit: mm)



#### I . Appearance Defects

NO.	ITEM	CRITERIA	CLASSIFICATION																	
1	Polarizer Black or White spot, Dirty spot, Foreign matter, Dent on the polarizer	<table border="1"> <thead> <tr> <th rowspan="2">Average Diameter (mm)</th> <th colspan="2">Acceptable Number</th> </tr> <tr> <th>Zone A,B</th> <th>Zone C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.15</math></td> <td colspan="2">Ignore</td> </tr> <tr> <td><math>0.15 &lt; \Phi \leq 0.30</math></td> <td>3</td> <td rowspan="2">Ignore</td> </tr> <tr> <td><math>\Phi &gt; 0.30</math></td> <td>0</td> </tr> </tbody> </table>	Average Diameter (mm)	Acceptable Number		Zone A,B	Zone C	$\Phi \leq 0.15$	Ignore		$0.15 < \Phi \leq 0.30$	3	Ignore	$\Phi > 0.30$	0	Minor				
Average Diameter (mm)	Acceptable Number																			
	Zone A,B	Zone C																		
$\Phi \leq 0.15$	Ignore																			
$0.15 < \Phi \leq 0.30$	3	Ignore																		
$\Phi > 0.30$	0																			
2	Scratch/line on the glass/Polarizer	<table border="1"> <thead> <tr> <th rowspan="2">Width (mm)</th> <th rowspan="2">Length (mm)</th> <th colspan="2">Acceptable Number</th> </tr> <tr> <th>Zone A,B</th> <th>Zone C</th> </tr> </thead> <tbody> <tr> <td><math>W \leq 0.03</math></td> <td>---</td> <td colspan="2">Ignore</td> </tr> <tr> <td><math>0.03 &lt; W \leq 0.08</math></td> <td><math>L \leq 5.0</math></td> <td>3</td> <td rowspan="2">Ignore</td> </tr> <tr> <td><math>W &gt; 0.08</math></td> <td>---</td> <td>0</td> </tr> </tbody> </table>	Width (mm)	Length (mm)	Acceptable Number		Zone A,B	Zone C	$W \leq 0.03$	---	Ignore		$0.03 < W \leq 0.08$	$L \leq 5.0$	3	Ignore	$W > 0.08$	---	0	Minor
Width (mm)	Length (mm)	Acceptable Number																		
		Zone A,B	Zone C																	
$W \leq 0.03$	---	Ignore																		
$0.03 < W \leq 0.08$	$L \leq 5.0$	3	Ignore																	
$W > 0.08$	---	0																		
3	Polarizer Bubble	<table border="1"> <thead> <tr> <th rowspan="2">Average Diameter (mm)</th> <th colspan="2">Acceptable Number</th> </tr> <tr> <th>Zone A,B</th> <th>Zone C</th> </tr> </thead> <tbody> <tr> <td><math>\Phi &gt; 0.5</math></td> <td>0</td> <td rowspan="3">Ignore</td> </tr> <tr> <td><math>0.2 &lt; \Phi \leq 0.5</math></td> <td>3</td> </tr> <tr> <td><math>\Phi \leq 0.2</math></td> <td>Ignore</td> </tr> </tbody> </table>	Average Diameter (mm)	Acceptable Number		Zone A,B	Zone C	$\Phi > 0.5$	0	Ignore	$0.2 < \Phi \leq 0.5$	3	$\Phi \leq 0.2$	Ignore	Minor					
Average Diameter (mm)	Acceptable Number																			
	Zone A,B	Zone C																		
$\Phi > 0.5$	0	Ignore																		
$0.2 < \Phi \leq 0.5$	3																			
$\Phi \leq 0.2$	Ignore																			
4	Any Dirt & Scratch on Polarizer's Protective Film	Ignore for not affect the polarizer.	Minor																	
5	Any Dirt on Cap Glass	<table border="1"> <thead> <tr> <th>Average Diameter (mm)</th> <th>Acceptable Number</th> </tr> </thead> <tbody> <tr> <td><math>\Phi \leq 0.5</math></td> <td>Ignore</td> </tr> <tr> <td><math>0.5 &lt; \Phi \leq 1.0</math></td> <td>3</td> </tr> <tr> <td><math>\Phi &gt; 1.0</math></td> <td>0</td> </tr> </tbody> </table>	Average Diameter (mm)	Acceptable Number	$\Phi \leq 0.5$	Ignore	$0.5 < \Phi \leq 1.0$	3	$\Phi > 1.0$	0	Minor									
Average Diameter (mm)	Acceptable Number																			
$\Phi \leq 0.5$	Ignore																			
$0.5 < \Phi \leq 1.0$	3																			
$\Phi > 1.0$	0																			

6	Glass Crack	 <p>Propagation crack is not acceptable.</p>	Major
7	Corner Chip on Substrate Glass	 <p>t= Glass thickness Accept <math>a \leq 2.0\text{mm}</math> or <math>b \leq 2.0\text{mm}</math>, <math>c \leq t</math></p>	Minor
8	Corner Chip on Cap Glass	 <p>t= Glass thickness Accept <math>a \leq 1.5\text{mm}</math> or <math>b \leq 1.5\text{mm}</math>, <math>c \leq t</math></p>	Minor
9	Chip on Contact Pad of Substrate Glass	 <p>t= Glass thickness Accept <math>a \leq 2.0\text{ mm}</math> or <math>b \leq 0.5\text{mm}</math>, <math>c \leq t</math> (on the contact pin) <math>a \leq 2.0\text{ mm}</math> or <math>b \leq 1.5\text{mm}</math>, <math>c \leq t</math> (outside of the contact pin)</p>	Minor
10	Chip on Face of Display	 <p>t= Glass thickness Accept <math>a \leq 1.5\text{mm}</math> or <math>b \leq 1.5\text{mm}</math>, <math>c \leq t</math></p>	Minor
11	Chip on Cap Glass	 <p>t= Glass thickness Accept <math>a \leq 2.0\text{mm}</math> or <math>b \leq 2.0\text{mm}</math>, <math>c \leq t/2</math> <math>a \leq 1.5\text{mm}</math> or <math>b \leq 1.5\text{mm}</math>, <math>t/2 \leq c \leq t</math></p>	Minor
12	Stain on Surface	Stain removable by soft cloth or air blow is acceptable.	Minor
13	TCP/FPC Damage	<p>(1) Crack, deep scratch, deep hole and deep pressure mark on the TCP/FPC are not acceptable.</p> <p>(2) Terminal lead twisted or broken is not allowable.</p> <p>(3) Copper exposed is not allowed by naked eye inspection.</p>	Minor
14	Dimension Unconformity	Checking by mechanical drawing.	Major

**II. Displaying Defects**

NO.	ITEM	CRITERIA	CLASSIFICATION															
1	Black/White spot Dirty spot Foreign matter	<table border="1"> <thead> <tr> <th data-bbox="517 367 794 434">Average Diameter (mm)</th> <th colspan="2" data-bbox="794 367 1155 405">Pieces Permitted</th> </tr> <tr> <td data-bbox="517 434 794 472"><math>\Phi \leq 0.10</math></td> <td data-bbox="794 405 979 434">Zone A,B</td> <td data-bbox="979 405 1155 434">Zone C</td> </tr> <tr> <td data-bbox="517 472 794 510"><math>0.10 &lt; \Phi \leq 0.20</math></td> <td colspan="2" data-bbox="794 434 1155 472">Ignore</td> </tr> <tr> <td data-bbox="517 510 794 539"><math>\Phi &gt; 0.20</math></td> <td data-bbox="794 472 979 510">3</td> <td data-bbox="979 472 1155 510">Ignore</td> </tr> <tr> <td data-bbox="517 539 794 568"><math>\Phi &gt; 0.20</math></td> <td colspan="2" data-bbox="794 510 1155 539">0</td> </tr> </thead> </table>	Average Diameter (mm)	Pieces Permitted		$\Phi \leq 0.10$	Zone A,B	Zone C	$0.10 < \Phi \leq 0.20$	Ignore		$\Phi > 0.20$	3	Ignore	$\Phi > 0.20$	0		Minor
Average Diameter (mm)	Pieces Permitted																	
$\Phi \leq 0.10$	Zone A,B	Zone C																
$0.10 < \Phi \leq 0.20$	Ignore																	
$\Phi > 0.20$	3	Ignore																
$\Phi > 0.20$	0																	
2	No Display	Not allowable.	Major															
3	Irregular Display	Not allowable.	Major															
4	Missing Line (row or column)	Not allowable.	Major															
5	Short	Not allowable.	Major															
6	Flicker	Not allowable.	Major															
7	Abnormal Color	Refer to the SPEC.	Major															
8	Luminance NG	Refer to the SPEC.	Major															
9	Over Current	Refer to the SPEC.	Major															

## 14 Precautions for operation and Storage

### 14.1 Precautions for Operation

- (1) Since OLED panel is made of glass, do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).
- (2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing. When the surface of the polarizer of OLED Module is contaminated, please wipe it off gently by using moisten soft cloth with isopropyl alcohol, do not use water, ketone or aromatics. If there is saliva or water on the OLED surface, please wipe it off immediately.
- (3) When handling OLED module, please be sure that the body and the tools are properly grounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.
- (4) Do not attempt to disassemble or process the OLED module.
- (5) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.
- (6) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.
- (7) An afterimage is created by the difference in brightness between unused dot and the fixed dot, according to the decrease of brightness of the emitting time. Therefore, to avoid having an afterimage, the full set should be thoroughly used instead of using a fixed dot. When the fixed dot emits, an afterimage can be created.
- (8) Flicker could be come out at full on display. And it disappears when frame frequency increase, but brightness decreases too.

### 14.2 Soldering

- (1) Soldering should be performed only on the I/O terminals.
- (2) Use soldering irons with proper grounding and no leakage.
- (3) Iron: no higher than 300°C and 3~4 sec during soldering.

### 14.3 Precautions for Storage

- (1) Please store OLED module in a dark place. Avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.
- (2) Keep the environment temperature between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature and high humidity.
- (3) Keep the OLED modules stored in the container when shipped from supplier before using them is recommended.
- (4) Do not leave any article on the OLED module surface for an extended period of time.

### 14.4 Warranty period

Visionox warrants for a period of 12 months from the shipping date when stored or used under normal condition.



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