1GbE PCS IP Core

User's Guide

October 2005
ipug28_02.0

Introduction

The 1GbE PCS Intellectual Property (IP) Core targets the programmable array section of the ORCA® ORT42G5 device and provides the PCS (Physical Coding Sublayer) function.

PCS (Physical Coding Sublayer) and PMA (Physical Media Attachment) are sublayers of the physical layer implementation of IEEE 802.3 standards. The PCS provides a uniform interface to the MAC sublayer through GMII (Gigabit Media Independent Interface) for all 1000Mb/s PHY implementations.

The ORT42G5 device is built on the Series 4 re-configurable embedded System-on-a-Chip (SoC) architecture and is made up of SERDES transceivers containing four channels, each operating at up to 3.7Gbits/s, with a full-duplex synchronous interface with built-in RX Clock and Data Recovery (CDR), and transmitter pre-emphasis, for high-speed data transmission.

This user's guide explains the functionality of the 1GbE PCS core and how to achieve the maximum level of performance.

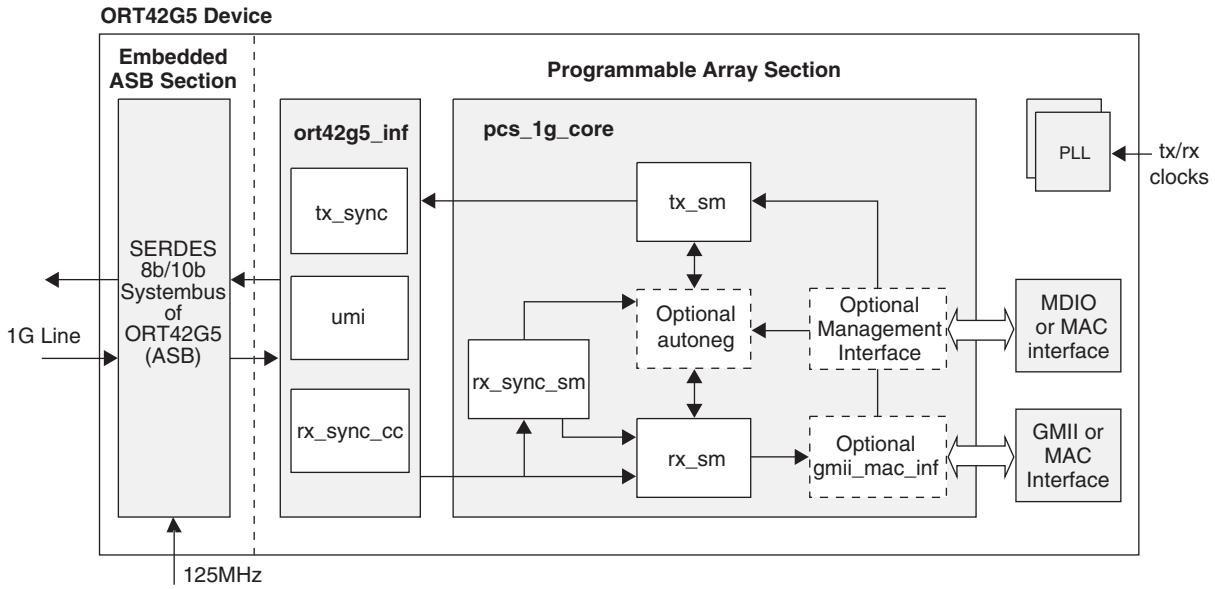
The 1GbE PCS core comes with the documentation and the files listed below:

- Data sheet
- Lattice gate level netlist
- Simulation models and test benches available for free evaluation
- Core instantiation template

Features

- Complete 1Gb Ethernet Physical Coding Sublayer solution based on the ORCA ORT42G5 device
- IP targeted to the ORT42G5 programmable array section implements functionality conforming to IEEE 803.2-2002
  - Encoding/decoding of GMII data octets
  - Optional Auto-negotiation function with management registers and interface
  - 10Gbps aggregate throughput
- Ethernet functionality supported by the embedded section of the ORT42G5
  - Supports 8b/10b encoding/decoding
  - Serialization/deserialization of code groups for transmit/receive
  - Clock recovery from encoded data stream

Figure 1. 1GbE PCS Solution



Note: Optional interfaces are not needed if an Ethernet MAC Interfafce is present on-chip

Functional Description

The major blocks in the 1GbE PCS core are shown in Figure 1. Descriptions of these blocks follow.

Transmit Section

This section implements the Transmit State Machine which is specified by Figures 36-5 and 36-6 in Clause 36 of the IEEE 802.3-2002 Standard.

The PCS Transmit process continuously generates code-groups based upon the `TXD <7:0>`, `TX_EN` and `TX_ER` signals on the GMII, sending them immediately to the Line Interface. The PCS Transmit process monitors the Auto-negotiation process transmit flag to determine whether to transmit data or reconfigure the link.

Receive Section

Receive Synchronization State Machine

This module implements the synchronization state machine which is specified by the Figure 36-9 of the IEEE 802.3-2002 Standard.

The Synchronization process is responsible for determining whether the underlying receive channel is ready for operation. The process continuously accepts code-groups from the Line Interface and scans them to detect the acquisition and maintenance of code group synchronization. This state machine also sets the `sync_status` flag which is monitored by the receive state machine.

Receive State Machine

This module implements the receive state machine, which is specified by Figures 36-7a and 36-7b in Clause 36 of the IEEE 802.3-2002 Standard.

The PCS Receive process continuously accepts and monitors code-groups from the Line Interface and generates `RXD <7:0>`, `RX_DV` and `RX_ER` on the GMII, and the internal receiving flag used by the Carrier Sense and Transmit processes.

Auto-negotiation

This module implements the Auto-negotiation state machine, which is specified by the Figure 37-6 in Clause 37 of the IEEE 802.3-2002 Standard.

The Auto-negotiation function that allows a device (local device) to advertise modes of operation it possesses to a device at the remote end of a link segment (link partner) and to detect corresponding operational modes that the link partner may be advertising. The Auto-negotiation function exchanges information between two devices that share a link segment and automatically configures both devices to take maximum advantage of their abilities.

Management Interface

The MDIO Management Interface is implemented based on specifications in Clause 22 of the IEEE 802.3-2002 standard.

The management interface is used to connect a management entity and a managed PHY for the purposes of controlling the PHY and gathering status from the PHY. The management interface consists of a pair of signals that physically transport the management information across the GMII, a frame format and a protocol specification for exchanging management frames, and a register set that can be read and written using these frames.

GMII Interface

This module, depending on the configuration, provides a GMII Interface or a connection to an on-chip MAC.

ORT42G5 Interface

This section provides the following functions:

- A bridging function between the 8-bit PCS core and the 32-bit Application Specific Block (ASB). The data rate translation cross the two clock domains is achieved using asynchronous FIFOs.
- Clock compensation to a tolerance of +/- 100 ppm between the recovered clock and IP system clock. This is done by insertion or deletion of idle characters.
- Logic to program the control registers inside the ASB through the system bus User Master Interface.

Design Parameters

Table 1. Parameter Descriptions

Parameter	Description
GMII_INF	If this parameter is set to "yes", a GMII interface will be provided through the FPGA I/Os to an external device. If this parameter is set to "no", an internal interface will be provided to a MAC on the same chip.
AUTO_NEG	If this parameter is set to "yes", the Auto-negotiation module and Management registers will be enabled. If this parameter is set to "no", the Auto-negotiation module and Management registers will be disabled.
MDIO_INF	The optional MDIO Interface is only available if the Auto-negotiation parameter is set to "yes". If the MDIO parameter is set to "yes", an MDIO interface will be provided through the FPGA I/Os to an external device.

Register Descriptions

These registers are accessed through the Management Interface (SMI). They are only present if Auto-negotiation and Management Interface options are selected. The registers are based on the register definition in the Section 22 of IEEE 802.3-2002.

Table 2. Top Level Register Addresses

Register Name	Register Address
Control Register	0x0
Status Register	0x1
PHY Identifier Register	0x2
PHY Identifier Register	0x3
Auto-negotiation Advertisement Register	0x4
Auto-negotiation Link Partner Ability Register	0x5
Auto-negotiation Expansion Register	0x6
Extended Status Register	0xf

Table 3. Register Map for 1GbE PCS Core

Address: **0x0**				Name: **Control Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RST	LP	SS0	ANE	PD	IS	RAN	DUP	COL	SS1	RESERVED					
Default value: 0x0140								Mode: Read/Write							
Description:															
RST				1 = Reset; 0 = Normal operation. Self clearing											
LP				Enables Loopback mode											
SS0, SS1				Speed Selection set to "01" – indicates 1000 Mb/s. Read only											
ANE				Auto-negotiation Enable											
RAN				Restart Auto-negotiation. Self clearing											
PD				Unsupported functions. Set to Zero. Read only											
IS				Unsupported functions. Set to Zero. Read only											
COL				Unsupported functions. Set to Zero. Read only											
DUP				Duplex mode. Set to One – only Full Duplex supported. Read only.											

Table 3. Register Map for 1GbE PCS Core (Continued)

Address: **0x1**				Name: **Status Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESERVED							ES	R	PS	ANC	RF	ANA	LS	JD	EC
Default value: 0x0109								Mode: Read Only							
Description:															
ES				Extended Status Information in Register 15. Bit set to One											
R				Reserved. Bit set to zero											
PS				Preamble Suppression. Not supported. Bit set to zero											
RF				Remote Fault											
ANA				Auto-negotiation Ability. Bit set to One											
LS				Link Status											
JD				Jabber Detect. Not supported. Bit set to zero											
EC				Extended Register capability											
ANC				Auto-negotiation Complete											

Address: **0x2**				Name: **PHY Identifier Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PHY2															
Default value: 0x2222								Mode: Read Only							
Description:															
PHY2				Combined with Register 3 it forms a 32-bit value which serves as an identifier.											

Address: **0x3**				Name: **PHY Identifier Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
PHY3															
Default value: 0x3333								Mode: Read Only							
Description:															
PHY3				Combined with Register 2 it forms a 32-bit value which serves as an identifier.											

Address: **0x4**				Name: **Auto-negotiation Advertisement Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
NP	R	RF		RESERVED			PAUSE		HD	FD	RESERVED				
Default value: 0x01								Mode: Read/Write							
Description: This register contains the Advertised Ability of the PHY.															
RESERVED, R				Reserved bits are set to zero											
FD				Full Duplex mode supported. Bit set to One											
HD				Half Duplex mode not supported. Bit set to Zero											
PAUSE				Provides Pause capability exchange mechanism											
RF				Remote Fault encoding not supported. Bits set to zero											
NP				Next Page Function. Not supported. Bit set to zero.											

Table 3. Register Map for 1GbE PCS Core (Continued)

Address: **0x5**				Name: **Auto-negotiation Link Partner Ability Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
LP_ADV_ABILITY															
Default value: 0x0000								Mode: Read Only							
Description:															
LP_ADV_ABILITY				This register contains the Advertised Ability of the Link Partner's PHY.											

Address: **0x6**				Name: **Auto-negotiation Expansion Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RESERVED													NP	AN	R
Default value: 0x0000								Mode: Read Only							
Description:															
RESERVED, R				Reserved bits are set to zero											
NP				Next Page Able (In this core the value is "0")											
AN				New Page Received											

Address: **0xF**				Name: **Extended Status Register**											
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FD	RESERVED														
Default value: 0x8000								Mode: Read Only							
Description:															
RESERVED				Reserved bits are set to zero											
FD				1000BaseX Full Duplex supported (set to "1" in this core)											

Signal Descriptions

Table 4. Signal Definitions for 1GbE PCS Solution I/O

Signal Name	Direction	Description
Clocks and Resets		
RX_CLK_125	Input	Receive Clock (125MHz)
TX_CLK_125	Input	Transmit Clock (125MHz)
RST_N	Input	Active Low Reset
USR_CLK	Input	Clock for the User Master Interface
GMII/MAC Interface		
RX_DV	Output	Receive Data Valid
RX_D [7:0]	Output	Receive Data Bus
RX_ER	Output	Receive
TX_ER	Input	Transmit Error Indicator
TX_D [7:0]	Input	Transmit Data Bus
TX_DV	Input	Transmit Data Valid
MDIO Signals		
MDC	Input	MDIO clock
MDIO	Input/Output	MDIO bi-directional data
Line Interface[1]		
REFCLKN_A	Input	CML reference clock input – SERDES Quad A
REFCLKP_A	Input	CML reference clock input – SERDES Quad A
HDINN_AC	Input	High-speed CML receive data input – SERDES Quad A, Channel C
HDINP_AC	Input	High-speed CML receive data input – SERDES Quad A, Channel C
HDOUTN_AC	Output	High-speed CML receive data output – SERDES Quad A, Channel C
HDOUTP_AC	Output	High-speed CML receive data output – SERDES Quad A, Channel C
Auto-negotiation Signals (if MDIO is not implemented)		
MR_ADV_ABILITY[15:0]	Input	Advertisement Register
MR_AN_ENABLE	Input	Enable Auto-negotiation
MR_RESTART_EN	Input	Restart Auto-negotiation
MR_AN_COMPLETE	Output	Auto-negotiation Complete
MR_LP_ADV_ABILITY[15:0]	Output	Link Partner Ability Register
MR_PAGE_RX	Output	Page Received
LINK_STATUS	Output	Link Status
Control Signals (if MDIO is not implemented)		
MR_MAIN_RESET	Input	Core Reset
MR_LOOPBACK	Input	Enable Loopback

1. The signals listed here are required for the Embedded SPI-4 interface Quad A, Channel C. Please refer to the ORT42G5 Data Sheet for additional information on configuring the SPI-4 interface for specific applications.

Table 5. Signal Definitions for 1GbE PCS Solution - FPGA/Embedded ASB Interface (Internal to ORT42G5 Device)[1]

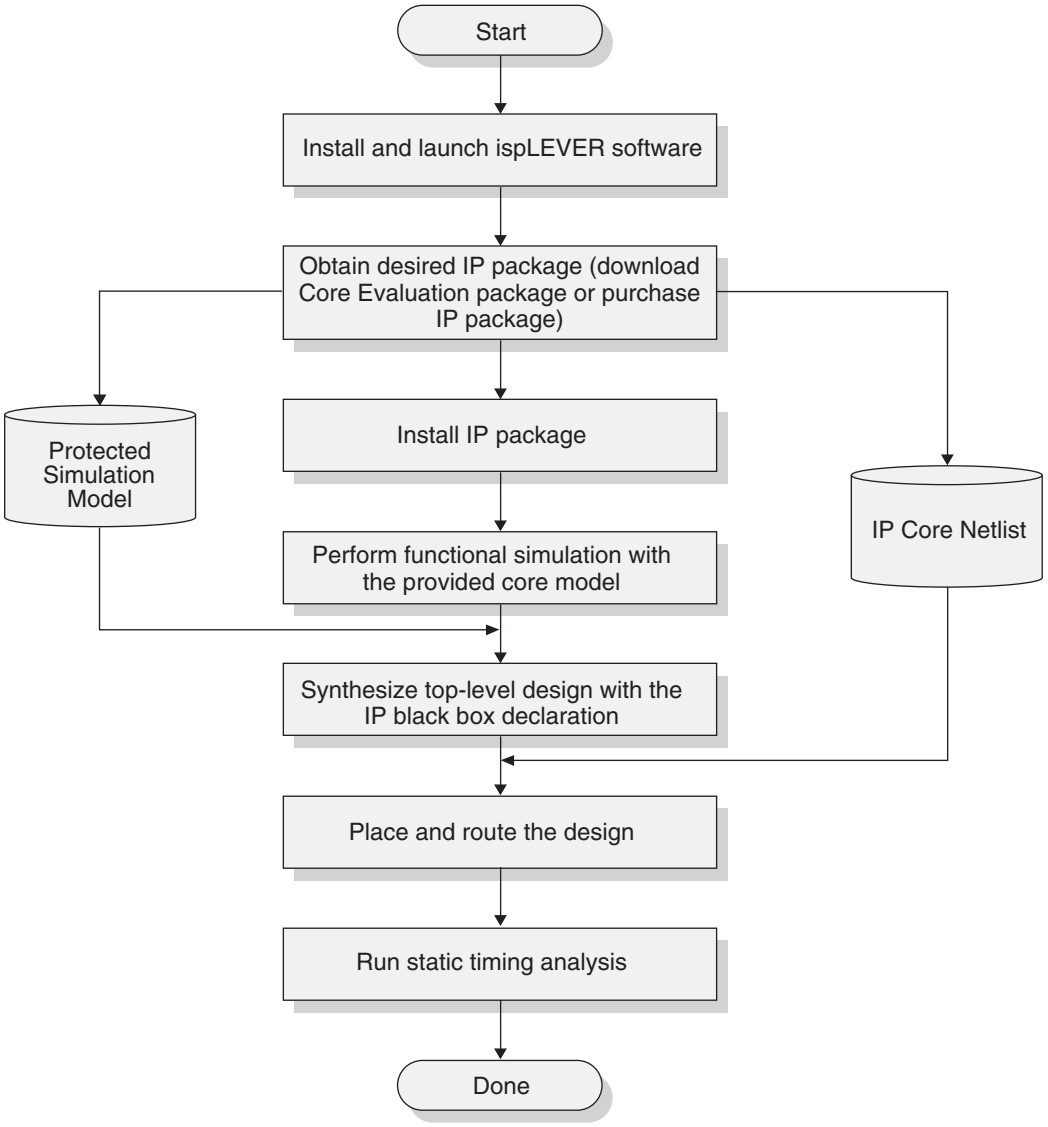
Signal Name	FPGA Direction	Description
Receive Interface Signals		
RSYSCLK_A2	Output	Low-speed receive FIFO clock for Channel AC
RCK78A	Input	Receive low-speed clock to FPGA – SERDES Quad A
MRWDAC[39]	Input	Code violation for Receive Data Byte 3 Channel AC
MRWDAC[38]	Input	K_CTRL for Receive Data Byte 3 Channel AC
MRWDAC[37:30]	Input	Receive Data Byte 3 Channel AC
MRWDAC[29]	Input	Code violation for Receive Data Byte 2 Channel AC
MRWDAC[28]	Input	K_CTRL for Receive Data Byte 2 Channel AC
MRWDAC[27:20]	Input	Receive Data Byte 2 Channel AC
MRWDAC[19]	Input	Code violation for Receive Data Byte 1 Channel AC
MRWDAC[18]	Input	K_CTRL for Receive Data Byte 1 Channel AC
MRWDAC[17:10]	Input	Receive Data Byte 1 Channel AC
MRWDAC[9]	Input	Code violation for Receive Data Byte 0 Channel AC
MRWDAC[8]	Input	K_CTRL for Receive Data Byte 0 Channel AC
MRWDAC[7:0]	Input	Receive Data Byte 0 Channel AC
Transmit Interface Signals		
TSYSCLK_AC	Output	Transmit Low Speed Clock Channel AC
TCK78A	Input	Transmit Low Speed Clock to FPGA – SERDES Quad A
TWDAC[31:0]	Output	Transmit Data Channel AC
TCOMMAAC[3:0]	Output	Transmit Comma Character Channel AC
TBIT9AC[3:0]	Output	Transmit Force Negative Disparity Channel AC

1. The signals listed here are required for the Embedded SPI-4 interface Quad A, Channel C. Please refer to the ORT42G5 Data Sheet for additional information on configuring the SPI-4 interface for specific applications.

1GbE PCS Core Design Flow

The 1GbE PCS IP Core can be implemented using various methods. The scope of this document covers only the push-button Graphical User Interface (GUI) flow. Figure 2 illustrates the software flow model used when evaluating with the 1GbE PCS.

Figure 2. Lattice IP Core Evaluation Flow



Functional Simulation

Simulation script files are provided in the "eval" directory for RTL simulation. These scripts rely on the sysbus and ORT42G5 models already installed with the ispLEVER® software which includes the ORT42G5 device. If these models are not installed, they should be installed before proceeding with this IP Core evaluation.

The script file <user_compile.do > will compile all of the user code in the evaluation. The user code for this IP core is the top level chip module. The script file <user_vsim.do> will need to be modified by the user to point to the sysbus and ORT42G5 simulation models (The ORT42G5 uses the ort82g5_work simulation model). Once modified this script will load the full chip and testbench. The script file <user_wave.do> will add all of the appropriate wave-

forms for the user. These scripts care located in the `1gbe_pcs_o4_1_001\orca4\ver1.0\eval\simulation\scripts`.

NOTE: The procedure described here is applicable ONLY when using ModelSim for simulation.

Simulation Procedures

1. Launch ModelSim
2. Using the main GUI, change the directory location
   Select: File -> Change Directory -> 1gbe_pcs_o4_1_001\orca4\ver1.0\eval\simulation
3. Execute <user_compile.do> to compile the full chip design and testbench files.
   Select: Macro -> Execute Macro -> scripts\<user_compile.do>

   For ModelSim 5.6a or above:
   Select: Tools -> Execute Macro -> scripts\<user_compile.do>
4. Modify the script <user_vsim.do> to point to the sysbus_work and ort82g5_work simulation model. These models are provided in the ispLEVER installation and ORT42G5.
5. Execute <user_vsim.do> to load the full chip design and testbench
   Select: Macro -> Execute Macro -> scripts\<user_vsim.do>

   For ModelSim 5.6a or above:
   Select: Tools -> Execute Macro -> scripts\<user_vsim.do>
6. Execute <user_wave.do> to load the appropriate waveforms for the simulation
   Select: Macro -> Execute Macro -> scripts\<user_wave.do>

   For ModelSim 5.6a or above:
   Select: Tools -> Execute Macro -> scripts\<user_wave.do>
7. Run the simulation.
   Select: Simulate -> Run -> Run-all

Core Implementation

Running Synthesis Using Synplicity's Synplify

The step-by-step procedure provided below describes how to run synthesis using Synplify outside the ispLEVER Project Navigator.

1. Change directory to 1gbe_pcs_o4_1_001\orca4\ver1.0\eval\synthesis\synplicity
2. Launch the Synplify synthesis tool
3. Select: Run -> Run TCL Script... -> pcs_1g_top.tcl
4. Within the provided project file the speed grade, implementation and device are preselected.
5. A default EDIF is also provided by the project file. This top-level EDIF netlist will be used during Place and Route.
6. Within the supplied synthesis scripts the necessary options have been supplied for a complete synthesis pass.
7. Select Run
8. The EDIF file (.edn) will be located in the ver1.0 directory.

Running Synthesis Using LeonardoSpectrum
The step-by-step procedure provided below describes how to run synthesis using LeondardoSpectrum outside the ispLEVER Project Navigator.

1. Change directory to: 1gbe_pcs_o4_1_001\orca4\ver1.0\eval\synthesis\exemplar
2. Launch the LeonardoSpectrum synthesis tool
3. Start a new project by opening <pcs_1g_top.tcl>
   Select: File -> Run Script -> pcs_1g_top.tcl
4. The script file contains the necessary parameters to target an ORCA 4 device.
5. The EDIF and generated preference file will be located in the same directory.

Running Place and Route (PAR) for ORCA devices in ispLEVER
The step-by-step procedure provided below describes how to perform Place and Route in ispLEVER for an ORCA device.

The core is required to internally interface with the customer application logic. The Place and Route tool requires a parameter constraint file for the particular GbE PCS IP core in order to correctly create an .NCD file.

1. Launch the Lattice Project Navigator tool.
2. Start a new project: File -> New Project
3. Browse to the directory of the desired location of the project. The generated files will be placed in this directory.
4. Enter the project name and then select EDIF as the project type.
5. Change the device type to an ORT42G5 with a -2 speed grade and BM484 package.
6. Copy the following files to the Place and Route working directory:
   a) ..\eval\ngo\1gbe_pcs_o4_1_001.ngo
   b) ..\eval\prf\<synthesis tool>\pcs_1g_top.prf
   c) The top-level EDIF netlist generated from running synthesis
7. Import the EDIF netlist into the project: Source -> Import...
8. Import the preference file into the project: Source -> Import Constraint File...
9. In the ispLEVER Project Navigator, highlight Place & Route Design, with a right mouse click select Properties. Set the following properties:
   - Placement Iterations: <5 >
   - Routing Passes: <15>
   All other options remain at their default values.
10. Select the Place & Route Trace Report in the project navigator to execute Place and Route and generate a timing report for ORCA.

Reference Information

The 1GbE PCS IP core solution is compliant with the standard IEEE 803.2-2002. A complete description of this standard is given in the specification document.

Additional information on implementing this solution is contained in the following documents:

- ORCA ORT42G5 FPSC Data Sheet
- ORCA Series 4 FPGAs Data Sheet
- Lattice technical note number TN1017, *ORCA Series4 MPI/System Bus*

These documents are available on the Lattice web site at www.latticesemi.com.

Technical Support Assistance

Hotline: 1-800-LATTICE (North America)
+1-503-268-8001 (Outside North America)
e-mail: techsupport@latticesemi.com
Internet: www.latticesemi.com

Appendix for ORCA Series 4 ORT42G5 FPSC

Table 6. Available Configuration

Configuration Number	Configuration Features
001	• GMII interface through FPGA I/Os. • No auto-negotiation and Management registers. • No MDIO interface.

Table 7. Performance and Utilization[1]

Configuration	PFUs	Block RAM	PLL	LUTs	Registers	f_{MAX}
1gbe_pcs_o4_1_001	157	4	2	622	605	125 MHz tx_clk rx_clk

1. Performance and utilization characteristics are generated using an ORT42G5-2BM484C in Lattice's ispLEVER 4.0 software. When using this IP core in a different density, package, speed, or grade within the ORT42G5 family, performance may vary.

Supplied Netlist Configurations

The Ordering Part Number (OPN) for all configurations of this core is 1GBE-PCS-O4-N1.

You can use the IPexpress™ software tool to help generate new configurations of this IP core. IPexpress is the Lattice IP configuration utility, and is included as a standard feature of the ispLEVER design tools. Details regarding the usage of IPexpress can be found in the IPexpress and ispLEVER help system. For more information on the ispLEVER design tools, visit the Lattice web site at: www.latticesemi.com/software.

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