

**Vishay Siliconix** 

RoHS

COMPLIANT HALOGEN

FREE

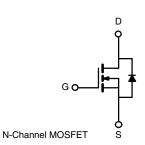
# Automotive N-Channel 60 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V <sub>DS</sub> (V)	60			
$R_{DS(on)} (\Omega)$ at $V_{GS} = 10 V$	0.006			
I <sub>D</sub> (A)	119			
Configuration	Single			
Package	TO-220			



#### **FEATURES**

- TrenchFET<sup>®</sup> power MOSFET
- · Package with low thermal resistance
- AEC-Q101 qualified d
- 100 %  $\rm R_g$  and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>



<b>ABSOLUTE MAXIMUM RATINGS</b> ( $T_c = 25 \degree C$ , unless otherwise noted)					
PARAMETER	SYMBOL	LIMIT	UNIT		
Drain-Source Voltage		V <sub>DS</sub>	60	V	
Gate-Source Voltage		V <sub>GS</sub>	± 20	v	
Continuous Drain Current	T <sub>C</sub> = 25 °C	Ι <sub>D</sub>	119		
Continuous Drain Current	T <sub>C</sub> = 125 °C		68		
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	120	А	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	480		
Single Pulse Avalanche Current L = 0.1 mH		I <sub>AS</sub>	65		
Single Pulse Avalanche Energy	Inche Energy		211	mJ	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	П	175	W	
Maximum Power Dissipation ~	T <sub>C</sub> = 125 °C	P <sub>D</sub>	56	VV	
Operating Junction and Storage Temperature Range		TJ, T <sub>stg</sub>	-55 to +175	°C	

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	40	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	0.88	0/W

#### Notes

- a. Package limited.
- b. Pulse test; pulse width  $\leq 300 \ \mu$ s, duty cycle  $\leq 2 \ \%$ .
- c. When mounted on 1" square PCB (FR4 material).
- d. Parametric verification ongoing.



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PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static		•					<b>I</b>
Drain-Source Breakdown Voltage	V <sub>DS</sub>	V <sub>GS</sub>	= 0, I <sub>D</sub> = 250 μA	60	-	-	v
Gate-Source Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> =	= V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.5	3.0	3.5	
Gate-Source Leakage	I <sub>GSS</sub>	V <sub>DS</sub> =	0 V, $V_{GS} = \pm 20$ V	-	-	± 100	nA
		$V_{GS} = 0 V$	V <sub>DS</sub> = 60 V	-	-	1	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 125 ^{\circ}\text{C}$	-	-	50	μA
		$V_{GS} = 0 V$	$V_{DS} = 60 \text{ V}, \text{ T}_{J} = 175 ^{\circ}\text{C}$	-	-	250	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	$V_{GS} = 10 V$	$V_{DS} \ge 5 V$	120	-	-	Α
		$V_{GS} = 10 V$	I <sub>D</sub> = 30 A	-	0.0045	0.0060	
Drain-Source On-State Resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V	I <sub>D</sub> = 30 A, T <sub>J</sub> = 125 °C	-	-	0.0104	Ω
		$V_{GS} = 10 V$	I <sub>D</sub> = 30 A, T <sub>J</sub> = 175 °C	-	-	0.0129	
Forward Transconductance <sup>b</sup>	9 <sub>fs</sub>	V <sub>DS</sub>	= 15 V, I <sub>D</sub> = 30 A	-	94	-	S
Dynamic <sup>b</sup>	<u>.</u>						
Input Capacitance	C <sub>iss</sub>			-	5196	6495	
Output Capacitance	C <sub>oss</sub>	$V_{GS} = 0 V$	V <sub>DS</sub> = 25 V, f = 1 MHz	-	708	885	pF
Reverse Transfer Capacitance	C <sub>rss</sub>	]		-	336	420	
Total Gate Charge <sup>c</sup>	Qg			-	96.5	145	
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>	$V_{GS} = 10 V$	$V_{DS} = 30 \text{ V}, I_D = 75 \text{ A}$	-	24.6	-	nC
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			-	27.2	-	
Gate Resistance	Rg		f = 1 MHz		1	1.7	Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>			-	16	24	
Rise Time <sup>c</sup>	t <sub>r</sub>	$\begin{array}{l} V_{\text{DD}}=30~V,~R_{L}=0.4~\Omega\\ I_{\text{D}}\cong75~A,~V_{\text{GEN}}=10~V,~R_{\text{g}}=1~\Omega \end{array}$		-	14	21	ns
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			-	34	51	
Fall Time <sup>c</sup>	t <sub>f</sub>	]		-	9	14	1
Source-Drain Diode Ratings and Chara	acteristics <sup>b</sup>	·					
Pulsed Current <sup>a</sup>	I <sub>SM</sub>			-	-	480	Α
Forward Voltage	V <sub>SD</sub>	$I_{\rm F} = 75 \text{ A}, V_{\rm GS} = 0$		-	0.9	1.5	V

Notes

a. Pulse test; pulse width  $\leq$  300 µs, duty cycle  $\leq$  2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

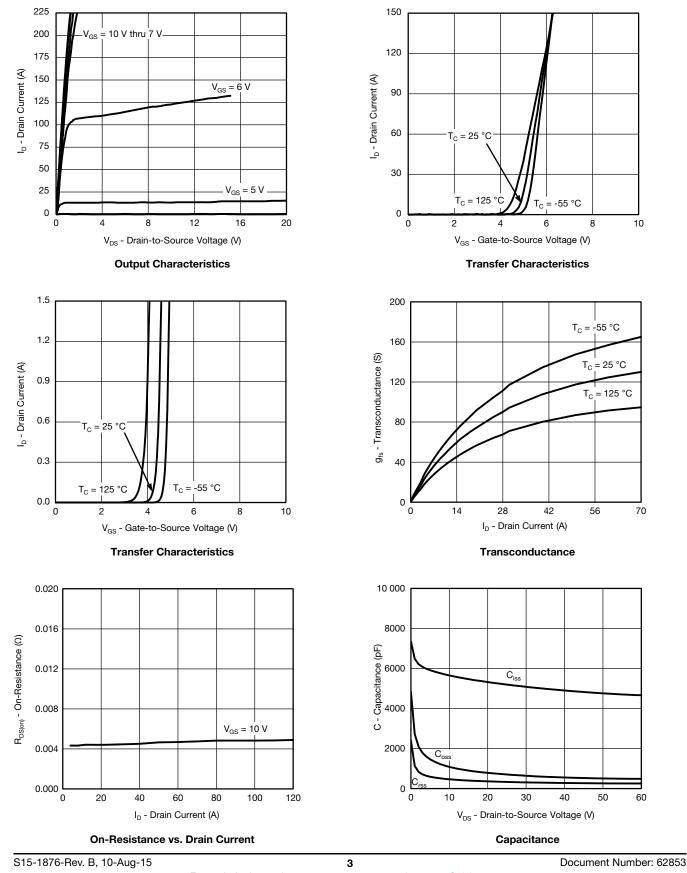
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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### **TYPICAL CHARACTERISTICS** ( $T_A = 25 \text{ °C}$ , unless otherwise noted)

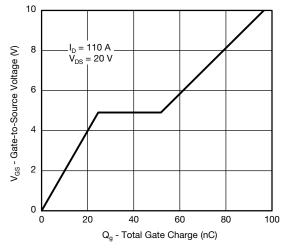


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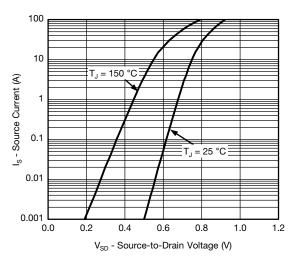


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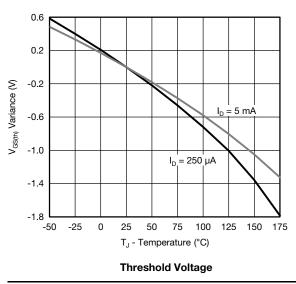
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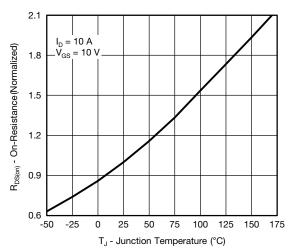


Gate Charge

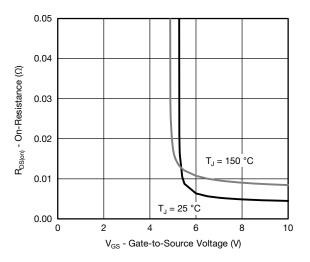


Source Drain Diode Forward Voltage

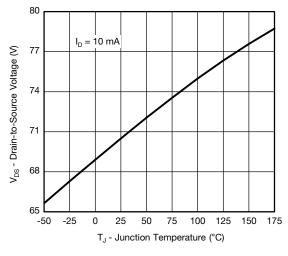




**On-Resistance vs. Junction Temperature** 



On-Resistance vs. Gate-to-Source Voltage



Drain Source Breakdown vs. Junction Temperature

S15-1876-Rev. B, 10-Aug-15

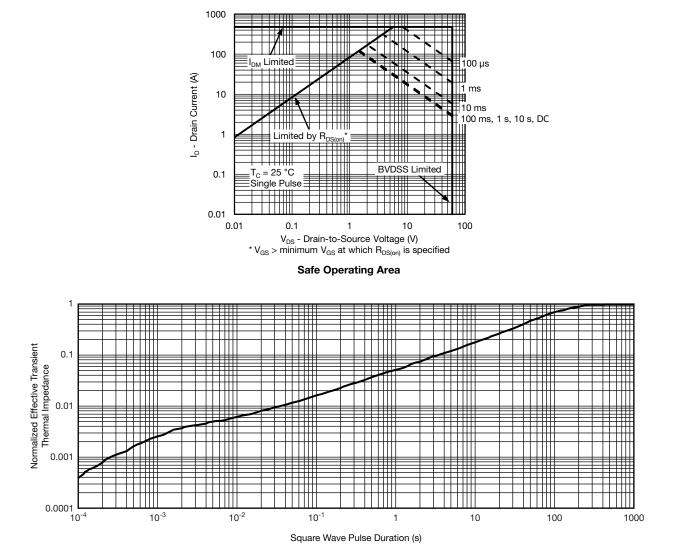
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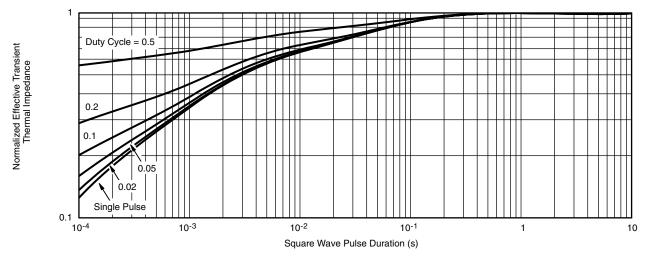


Normalized Thermal Transient Impedance, Junction-to-Ambient



### **Vishay Siliconix**

### **THERMAL RATINGS** (T<sub>A</sub> = 25 °C, unless otherwise noted)



#### Normalized Thermal Transient Impedance, Junction-to-Case

#### Note

• The characteristics shown in the two graphs

- Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)

- Normalized Transient Thermal Impedance Junction-to-Case (25 °C)

are given for general guidelines only to enable the user to get a "ball park" indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <a href="http://www.vishay.com/ppg?62853">www.vishay.com/ppg?62853</a>.



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REVISION HISTORY <sup>a</sup>			
REVISION	DATE	DESCRIPTION OF CHANGE	
В	04-Aug-15	Revised R <sub>g</sub> minimum limit	

Note

a. As of April 2014



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## **TO-220AB**



	MILLIMETERS		INC	HES
DIM.	MIN.	MAX.	MIN.	MAX.
А	4.25	4.65	0.167	0.183
b	0.69	1.01	0.027	0.040
b(1)	1.20	1.73	0.047	0.068
С	0.36	0.61	0.014	0.024
D	14.85	15.49	0.585	0.610
D2	12.19	12.70	0.480	0.500
E	10.04	10.51	0.395	0.414
е	2.41	2.67	0.095	0.105
e(1)	4.88	5.28	0.192	0.208
F	1.14	1.40	0.045	0.055
H(1)	6.09	6.48	0.240	0.255
J(1)	2.41	2.92	0.095	0.115
L	13.35	14.02	0.526	0.552
L(1)	3.32	3.82	0.131	0.150
ØР	3.54	3.94	0.139	0.155
Q	2.60	3.00	0.102	0.118
	0413-Rev. P,		0.102	0.118

Note

 $^{\star}$  M = 1.32 mm to 1.62 mm (dimension including protrusion) Heatsink hole for HVM



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