IXYSRF

IXZ631DF12N100
RF Power MOSFET & Driver

DE375-102N12 MOSFET and IXRFD631 Gate Driver Module

1000 V
12 A
1 Ω

Features

- Isolated substrate
  - High isolation voltage (>2500 V)
  - Excellent thermal transfer
  - Increased temperature and power cycling capability
- Low $R_{DS(ON)}$
- Very low insertion inductance
- No Beryllium Oxide (BeO) or other hazardous materials
- Latch-up protected
- Low quiescent supply current
- RoHS compliant

Advantages

- Optimized for RF and high speed
- Easy to mount, no insulators needed
- High power density
- Single package reduces size and heat sink area

Applications

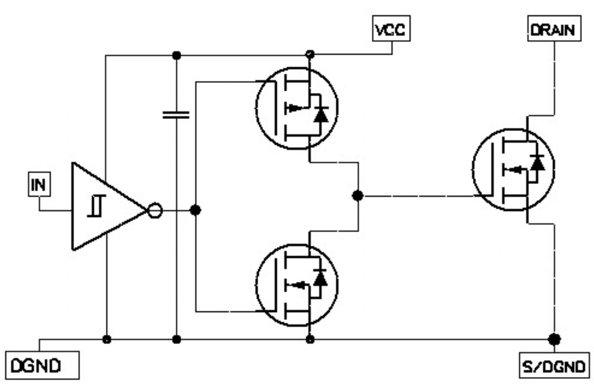
- Class D or E switching generators
- Switch mode power supplies (SMPS)
- Pulse generators
- Transducer driver

Description

The IXZ631DF12N100 is a CMOS high-speed, high-current gate driver and MOSFET combination module specifically designed for Class D, E, HF, and RF applications at up to 27 MHz, as well as other applications. The IXZ631DF12N100 in pulse mode can provide 72 A of peak current while producing voltage rise and fall times of less than 5 ns, and minimum pulse widths of 8 ns. The input of the driver is fully immune to latch-up over the entire operating range. Designed with small internal delays, the IXZ631DF12N100 is suitable for higher power operation where combiners are used. Its features and wide safety margin in operating voltage and power make the IXZ631DF12N100 unmatched in performance and value.

The IXZ631DF12N100 is packaged in IXYSRF's low-inductance RF package incorporating layout techniques to minimize stray lead inductances for optimum switching performance. The IXZ631DF12N100 is a surface-mountable device.

Figure 1
Functional diagram



Device Specifications

Parameter	Value
Maximum junction temperature	150 °C
Operating temperature range	- 40 °C to 85 °C
Weight	5.5 g

Symbol	Test Conditions	Maximum Ratings
f_{MAX}	$I_D = 0.5\ I_{DM25}$ A	27 MHz
V_{DSS}		1000 V
V_{CC}		20 V
I_{DSS}	$V_{DS} = 0.8\ V_{DSS}$ $T_J = 25°C$ $V_{GS} = 0$ V $T_J = 125°C$	50 uA 1 mA
I_{DM25}	$T_C = 25°C$	12 A
I_{DM}	$T_C = 25°C$, pulse limited by T_{JM}	72 A
I_{AR}	$T_C = 25°C$	12 A
P_T (MOSFET and Driver)	$T_C = 25°C$	625 W
R_{thJC}		0.2 °C/W
R_{thJHS}		0.4 °C/W

Device Performance

Symbol	Test Condition	Minimum	Typical	Maximum
$R_{DS(ON)}$	$V_{CC} = 15$ V, $I_D = 0.5I_{DM25}$ A Pulse t ≤ 300 µs, Duty Cycle ≤ 2%		1 Ω	
V_{CC}		8 V	15 V	20 V
IN (Signal Input)		- 5 V		V_{CC} + 0.3 V
V_{IH} (High Input Voltage)	$V_{CC} = 15$ V	3.5 V	3 V	
V_{IL} (Low Input Voltage)	$V_{CC} = 15$ V		2.8 V	0.8 V
V_{HYS} Input hysteresis			0.23 V	
Z_{IN}	f = 1 MHz		930-j7960 Ω	
C_{stray}	f = 1 MHz any one pin to the back plane metal		46 pF	
C_{OSS}	V_{IN} (V_{GS}) = 0 V, $V_{DS} = 0.8\ V_{DSS(max)}$ f =1 MHz		110 pF	
t_{ONDLY}	$T_C = 25$ °C $V_{CC} = 15$ V 1 µs pulse, $I_D = 6$ A		25 ns	
t_{OFFDLY}	$T_C = 25$ °C $V_{CC} = 15$ V 1 µs pulse, $I_D = 6$ A		28 ns	
t_R	$T_C = 25$ °C $V_{CC} = 15$ V 1 µs pulse, $I_D = 6$ A		2.4 ns	
t_F	$T_C = 25$ °C $V_{CC} = 15$ V 1 µs pulse, $I_D = 6$ A		1.55 ns	

Fig. 2

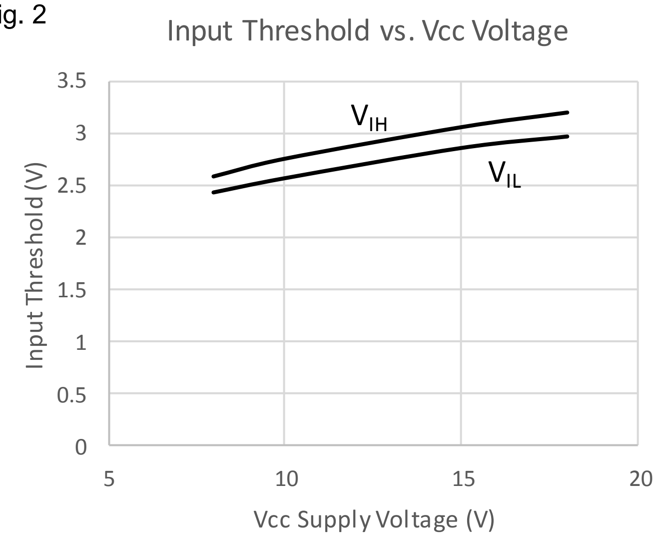


Fig. 3

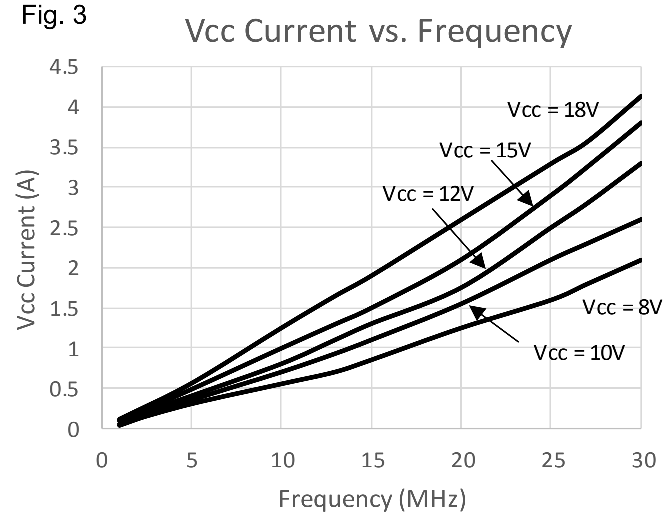


Fig. 4

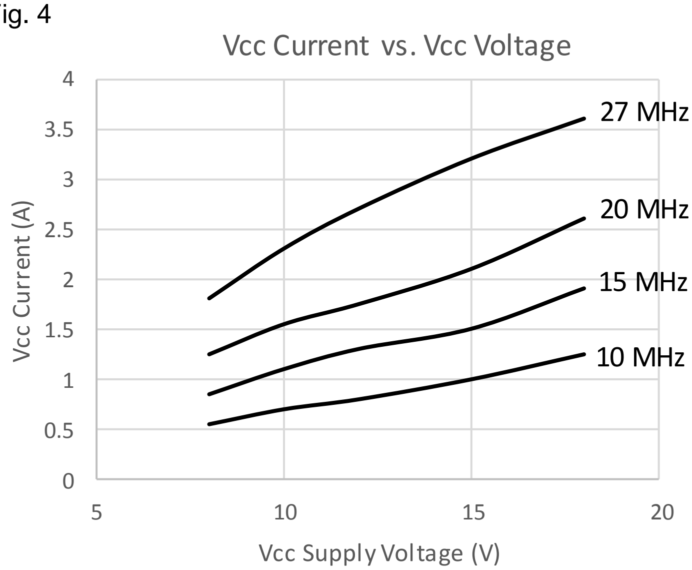


Fig. 5

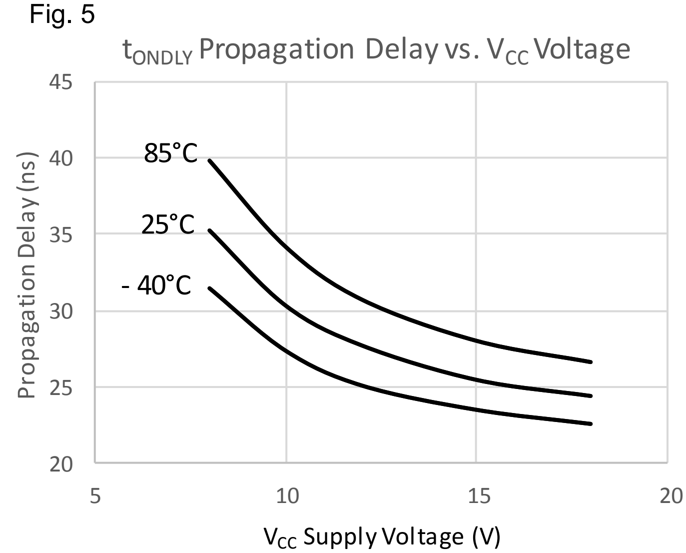


Fig. 6

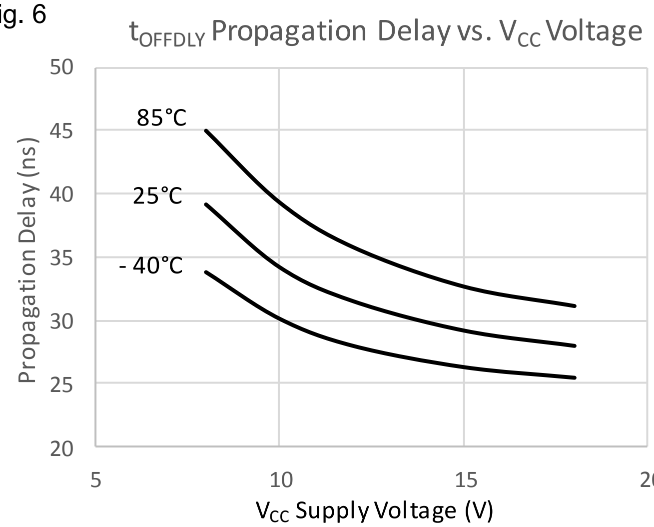


Fig. 7

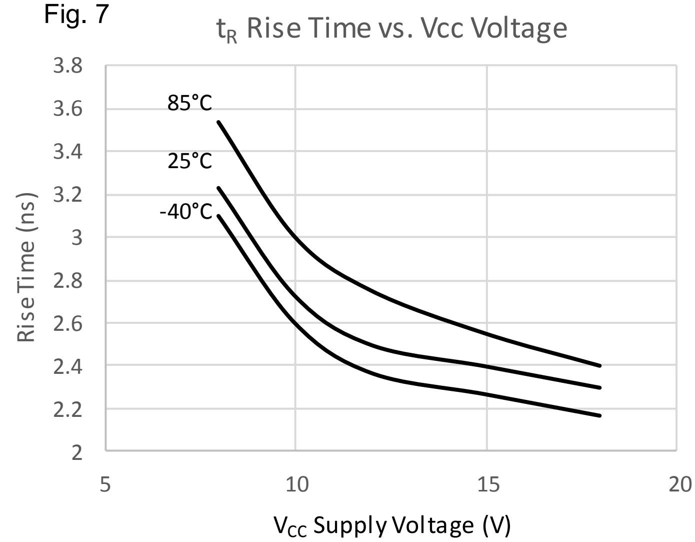


Fig. 8

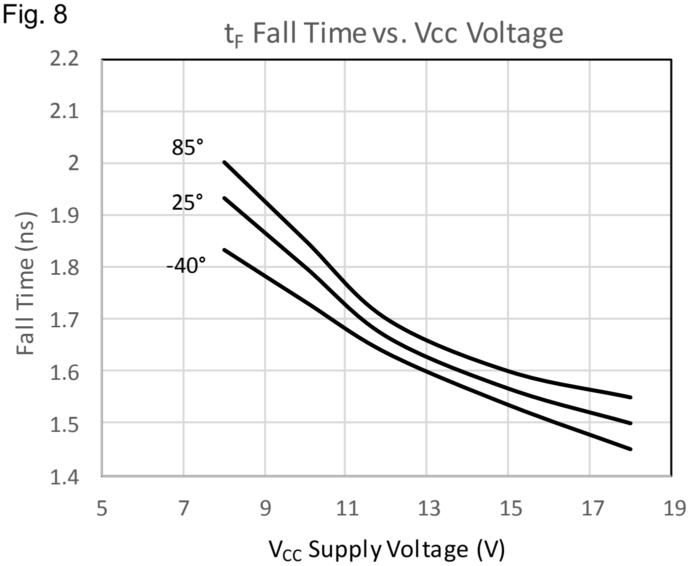


Fig. 9

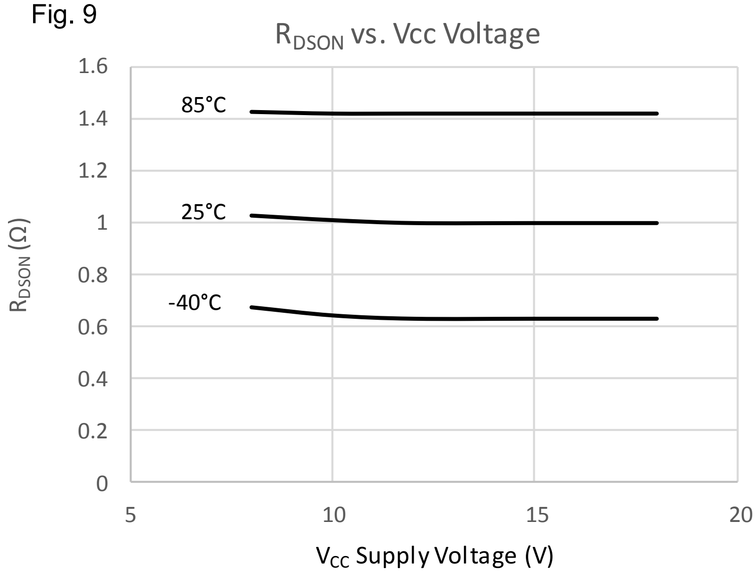


Fig. 10

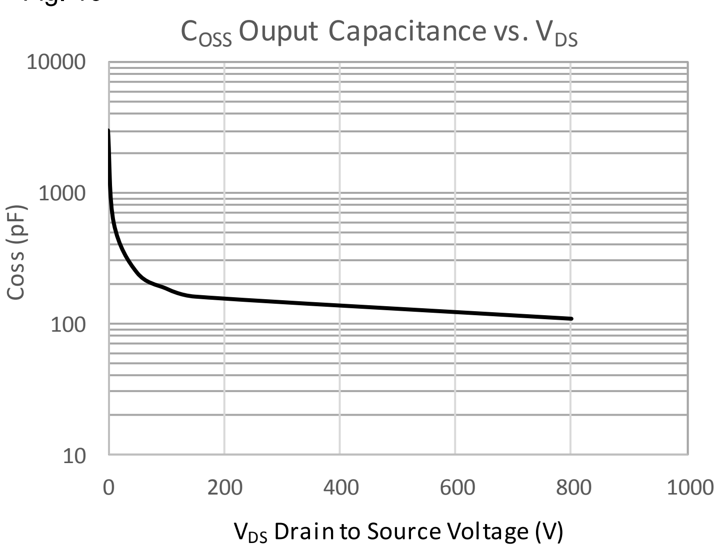


Fig. 11

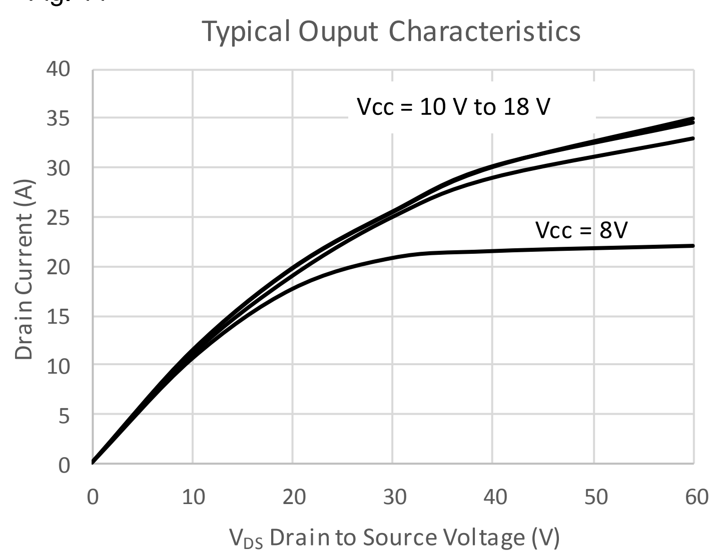


Fig. 12

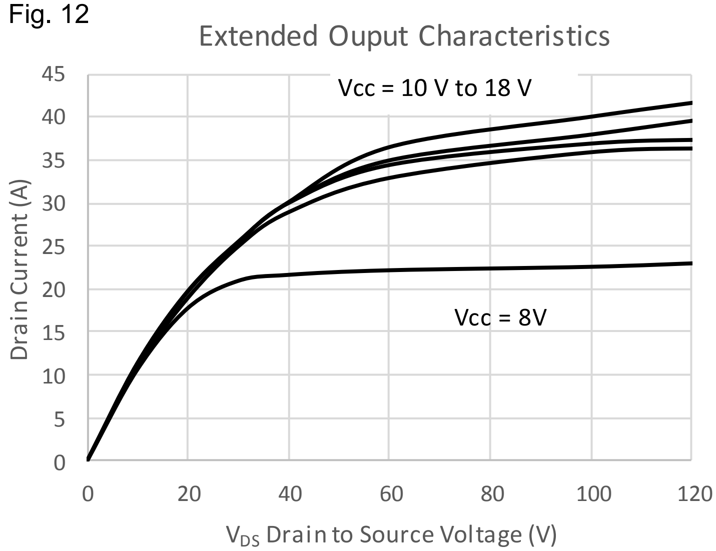
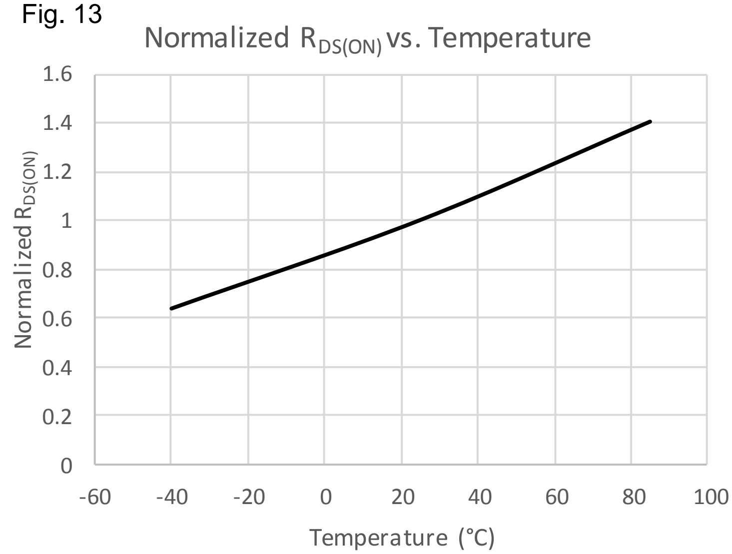


Fig. 13



Lead description

SYMBOL	FUNCTION	DESCRIPTION
Drain	MOSFET drain	Drain of power MOSFET.
S/DGND	MOSFET source	Source of power MOSFET. This connection is common to DGND.
Vcc	Driver section supply voltage	Power supply input for the logic input and driver output sections.
IN	Input	Input signal.
DGND	Driver power ground	The driver ground leads. Internally connected to all circuitry, these leads provide ground reference for the driver. These leads should be connected to a low-noise analog ground plane for optimum performance.
N/C	None	No connection to this lead.

Figure 14 Package drawing

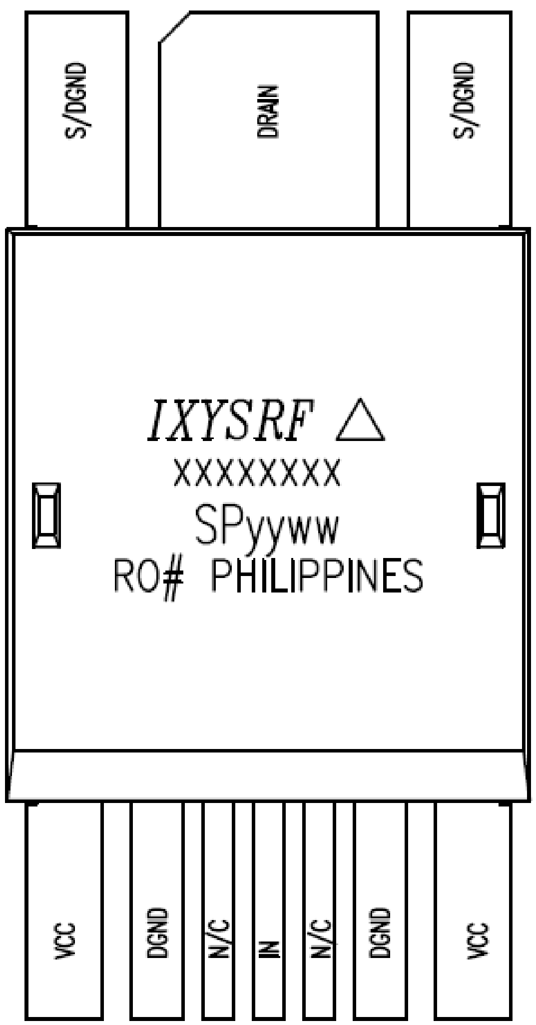
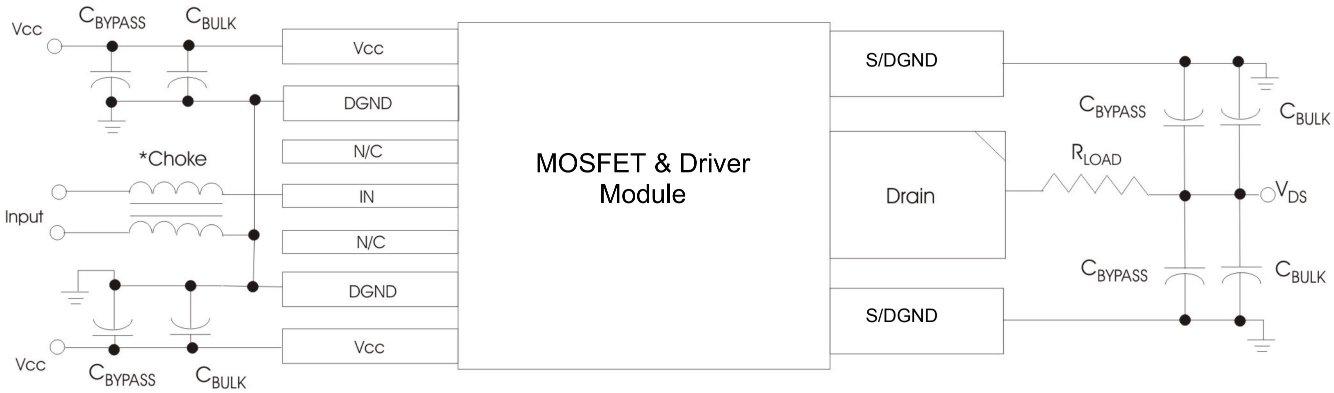


Figure 15 Test circuit



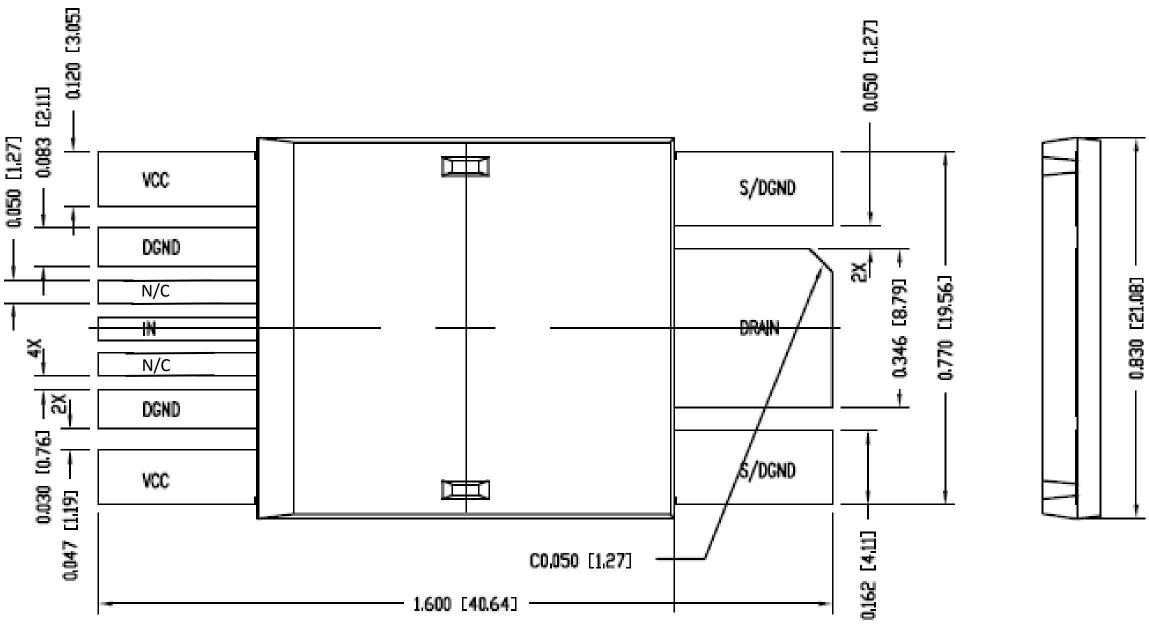
*Choke– A common-mode choke is optional and can be used to help stabilize the threshold level due to ground bounce and to minimize false triggering.

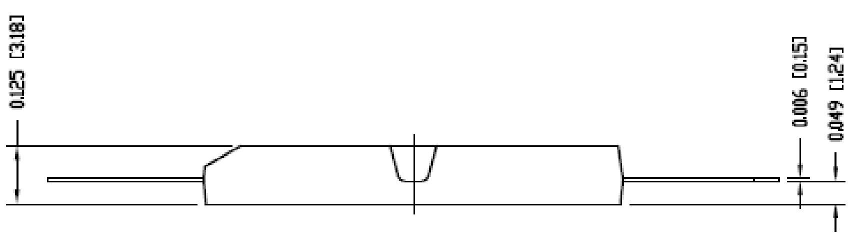
C_{BULK}- Bulk capacitance helps to stabilize both the high voltage V_{DS} for the drain circuit and low voltage Vcc for the driver circuit. Actual values vary according to load and operating conditions. For the driver section, tantalum capacitors are recommended for their fast energy delivery.

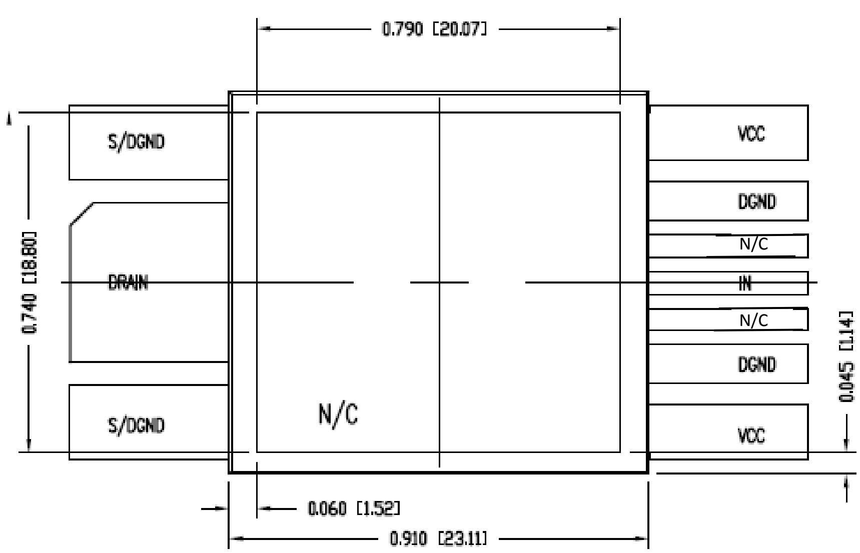
C_{BYPASS}- Ideally, the benefits realized through bypass capacitance increase as more is used by way of overlapping impedance curves, lowering the overall broadband impedance to ground. Typically a range of 0.1 µF, 0.01 µF, 0.001 µF capacitors in sufficient quantities give good results.

Circuit board layout should be carefully considered to optimize operation. Each of the Vcc leads on the driver section should be treated as its own power supply lead. Bulk and bypass capacitors attached between drain and source leads should be placed symmetrically between the leads. Excessive parasitic inductance can result in V = L di/dt inductive voltage drops, causing unpredictable operation.

Figure 16 IXZ631DF12N100 package outline







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