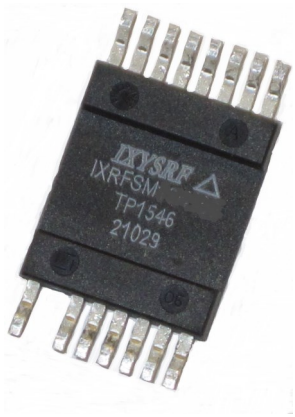
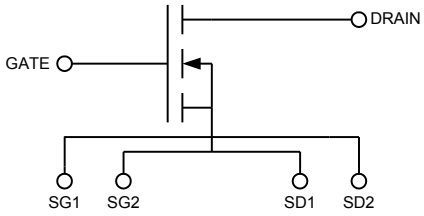
IXRFSM18N50
Z-MOS RF Power MOSFET

N-Channel Enhancement Mode Switch Mode RF MOSFET
Low Capacitance Z-MOS$_{TM}$ MOSFET Process
Optimized for RF Operation
Ideal for Class C, D, & E Applications

V_{DSS} = 500 V
I_{D25} = 19 A
$R_{DS(on)}$ ≤ 0.34 Ω
P_{DC} = 835 W

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	T_J = 25°C to 150°C	500	V
V_{DGR}	T_J = 25°C to 150°C; R_{GS} = 1 MΩ	500	V
V_{GS}	Continuous	±20	V
V_{GSM}	Transient	±30	V
I_{D25}	T_c = 25°C	19	A
I_{DM}	T_c = 25°C, pulse width limited by T_{JM}	95	A
I_{AR}	T_c = 25°C	19	A
E_{AR}	T_c = 25°C	30	mJ
dv/dt	$I_S \le I_{DM}$, di/dt ≤ 100A/μs, $V_{DD} \le V_{DSS}$, $T_j \le 150°C$, R_G = 0.2Ω	5	V/ns
	I_S = 0	>200	V/ns
P_{DC}		835	W
P_{DHS}	T_c = 25°C	370	W
P_{DAMB}	T_{amb} = 25°C	3.0	W





Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values min.	typ.	max.	
V_{DSS}	V_{GS} = 0 V, I_D = 4 ma	500			V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250μA	3.5	4.9	6.5	V
I_{GSS}	V_{GS} = ±20 V_{DC}, V_{DS} = 0			±100	nA
I_{DSS}	$V_{DS} = 0.8V_{DSS}$ T_J = 25C V_{GS}=0 T_J =125C			50 1	μA mA
$R_{DS(on)}$	V_{GS} = 20 V, $I_D = 0.5I_{D25}$ Pulse test, t ≤ 300μS, duty cycle d ≤ 2%		.32	.34	Ω
R_{thJC} R_{thJHS}			0.35	0.15	°C/W °C/W
g_{fs}	V_{DS} = 50 V, $I_D = 0.5I_{D25}$, pulse test	5.0	5.4	6.0	S
T_J		-55		+150	°C
T_{JM}			150		°C
T_{stg}		-55		+150	°C
T_L	1.6mm(0.062 in) from case for 10 s		300		°C
Weight			5		g

Features

- Isolated Substrate
  - high isolation voltage (>2500V)
  - excellent thermal transfer
  - Increased temperature and power cycling capability
- IXYS advanced Z-MOS process
- Low gate charge and capacitances
  - easier to drive
  - faster switching
- Low $R_{DS(on)}$
- Very low insertion inductance (<2nH)
- No beryllium oxide (BeO) or other hazardous materials

Advantages

- Optimized for RF and high speed
- Easy to mount—no insulators needed
- High power density

Symbol	Test Conditions (T_J = 25°C unless otherwise specified)	Characteristic Values min.	typ.	max.	
R_G			0.5		Ω
C_{iss}		1650	1950	2250	pF
C_{oss}	V_{GS} = 0 V, V_{DS} = 0.8 $V_{DSS(max)}$, f = 1 MHz	150	175	175	pF
C_{rss}		14	17	20	pF
C_{stray}	Back Metal to any Pin		33		pF
$T_{d(on)}$			4		ns
T_{on}	V_{GS} = 15 V, V_{DS} = 0.8 V_{DSS}		4		ns
$T_{d(off)}$	I_D = 0.5 I_{DM} R_G = 1 Ω (External)		5		ns
T_{off}			6		ns
$Q_{g(on)}$			42		nC
Q_{gs}	V_{GS} = 10 V, V_{DS} = 0.5 V_{DSS} I_D = 0.5 I_{D25}		13		nC
Q_{gd}			20		nC

Source-Drain Diode

Characteristic Values (T_J = 25°C unless otherwise specified)

Symbol	Test Conditions	min.	typ.	max.	
I_S	V_{GS} = 0 V			19	A
I_{SM}	Repetitive; pulse width limited by T_{JM}			95	A
V_{SD}	I_F = I_S, V_{GS}=0 V, Pulse test, t ≤ 300µs, duty cycle ≤2%			1.5	V
T_{rr}			200		ns

CAUTION: Operation at or above the Maximum Ratings values may impact device reliability or cause permanent damage to the device.

Fig. 1

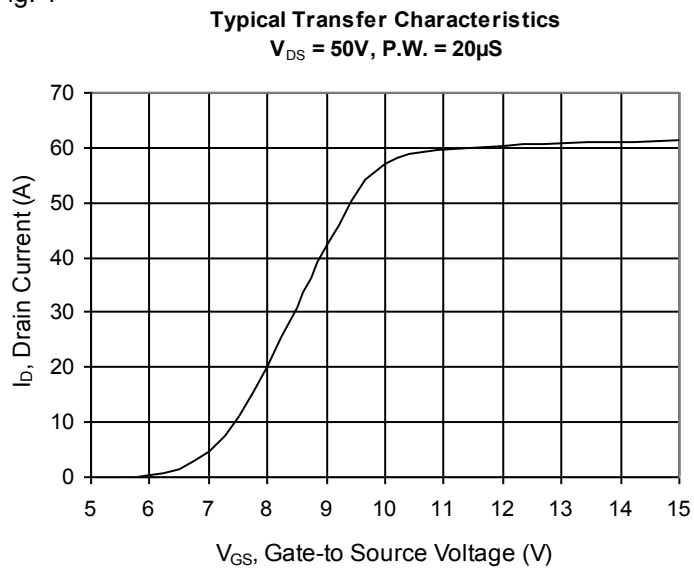


Fig. 2

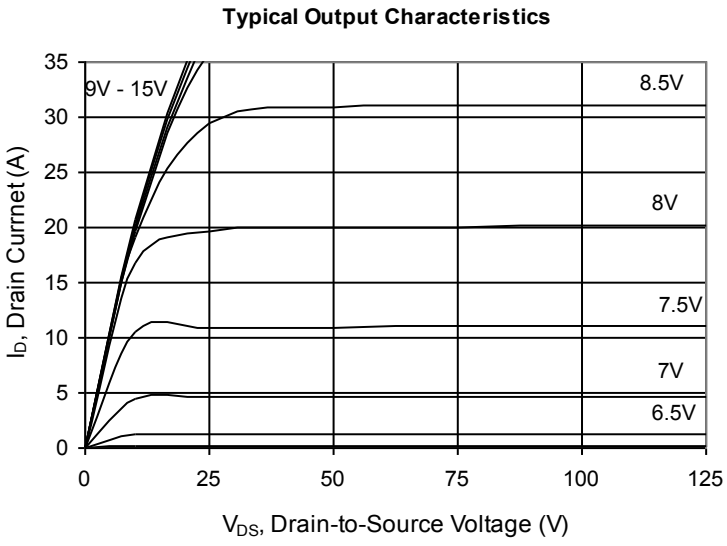


Fig. 3

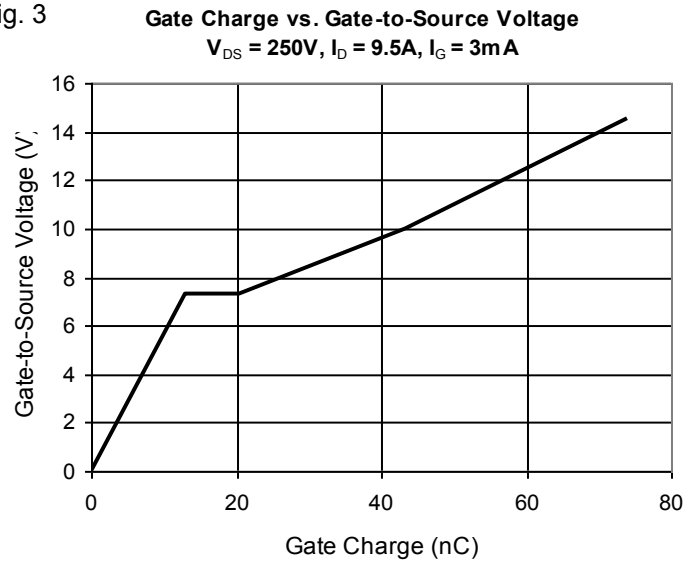


Fig. 4

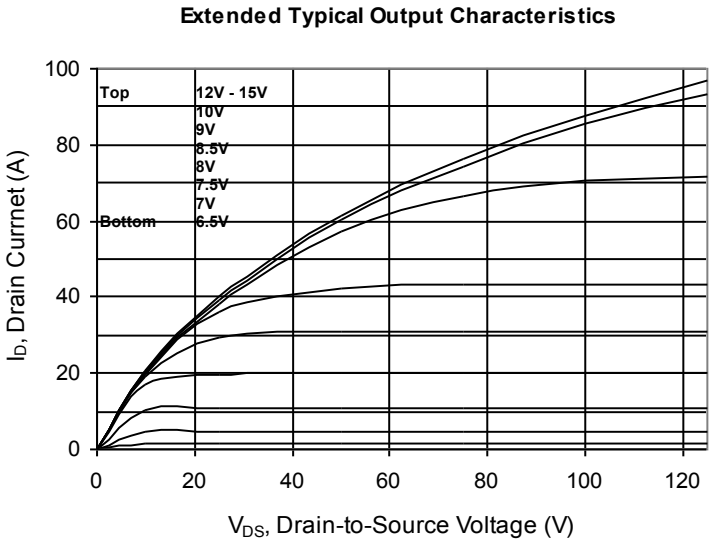


Fig. 5

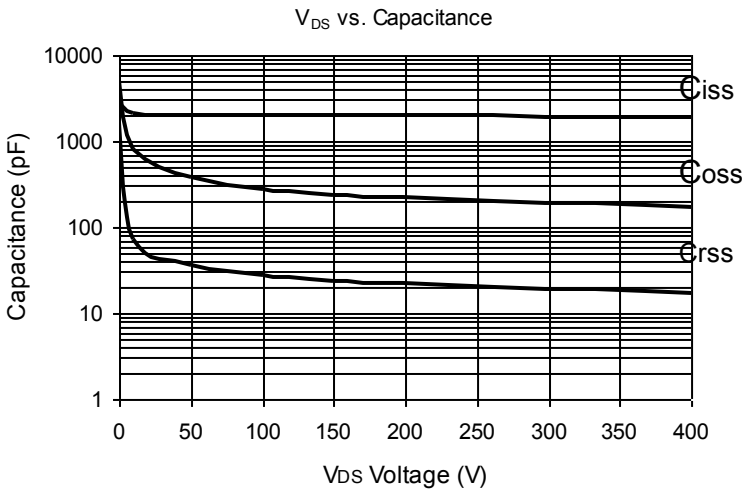


Fig. 6

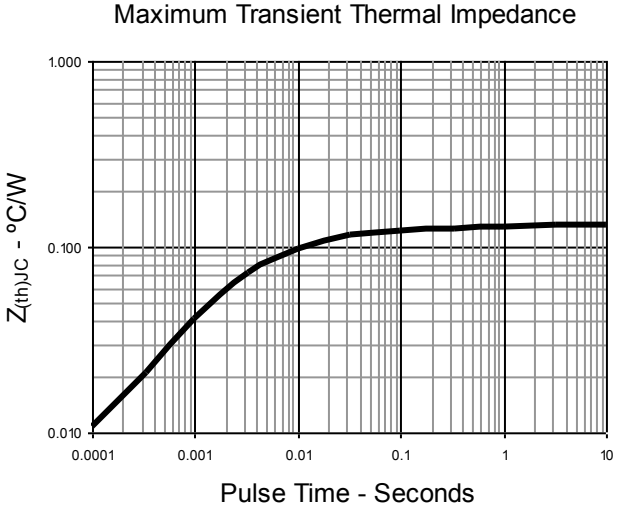
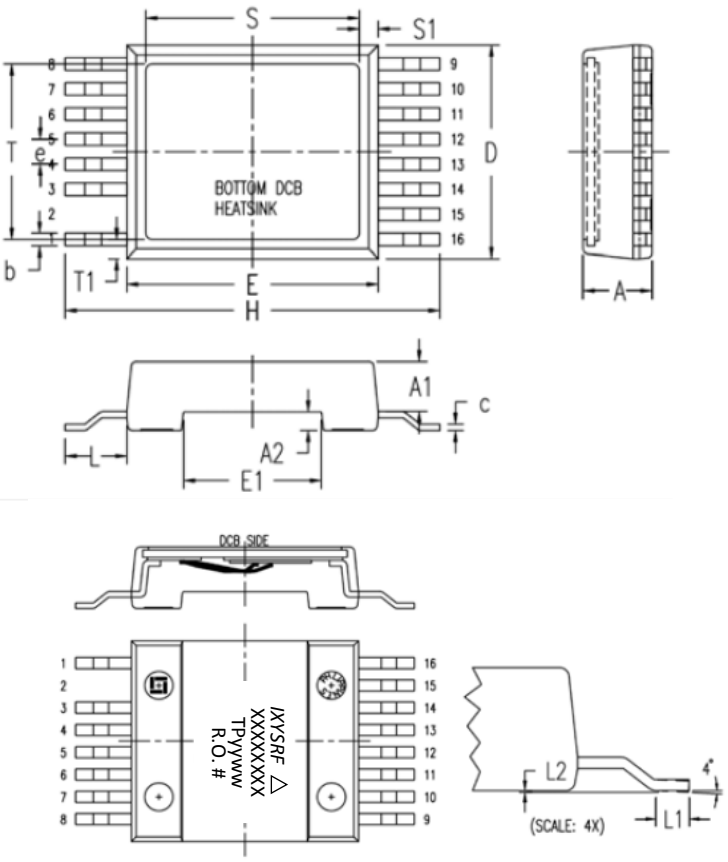


Fig. 7 Pin Description

Symbol	Function	Pin Number	Description
SG1	Source-gate side	1, 3	Source connection on gate side
SG2	Source-gate side	6, 7, 8	Source connection on gate side
SD1	Source-drain side	9, 10	Source connection on drain side
SD2	Source-drain side	15, 16	Source connection on drain side
Drain	Drain	11, 12, 13, 14	MOSFET Drain
Gate	Gate	4, 5	MOSFET Gate

Fig. 8 Package Description



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.661	.677	16.80	17.20
E	.780	.795	19.80	20.20
E1	.425	.441	10.80	11.20
e	.079 BSC		2.00 BSC	
H	1.161	1.185	29.50	30.10
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.661	.677	16.80	17.20
S1	.051	.067	1.30	1.70
T	.543	.559	13.80	14.20
T1	.051	.067	1.30	1.70

Note:
1. ALL LEADS ARE PURE MATTE TIN PLATED.
2. Cu SURFACE OF BOTTOM DCB IS PRE-Ni PLATED UNLESS OTHERWISE STATED
3. Cu SURFACE OF BOTTOM DCB IS ELECTRICALLY ISOLATED 2,500V AC FROM ALL OTHER LEADS.
4. PIN 2 N/A, missing, used for device orientation.

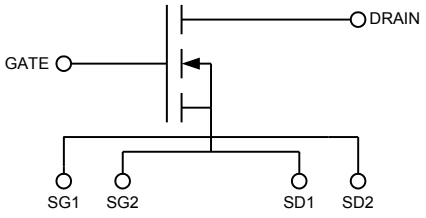
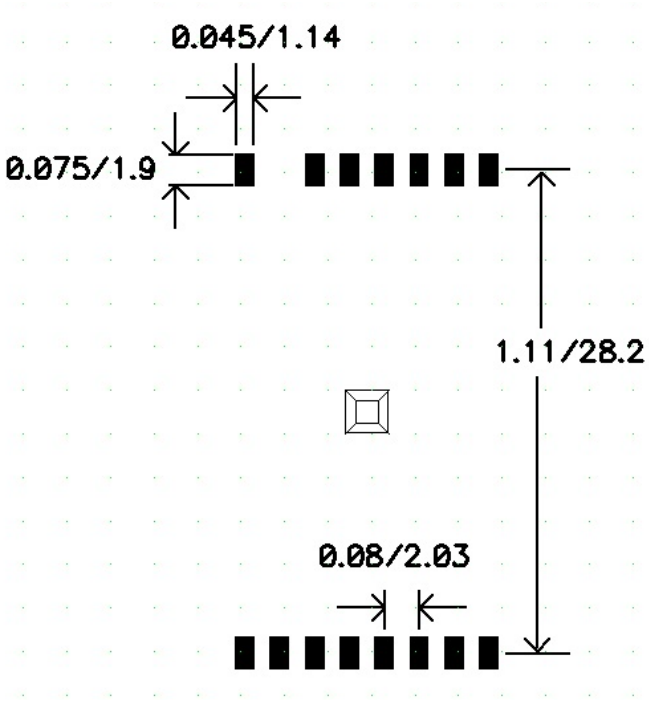
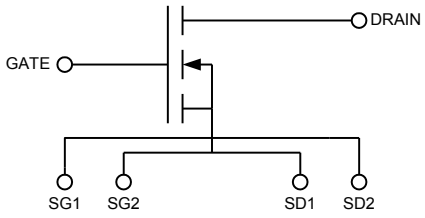


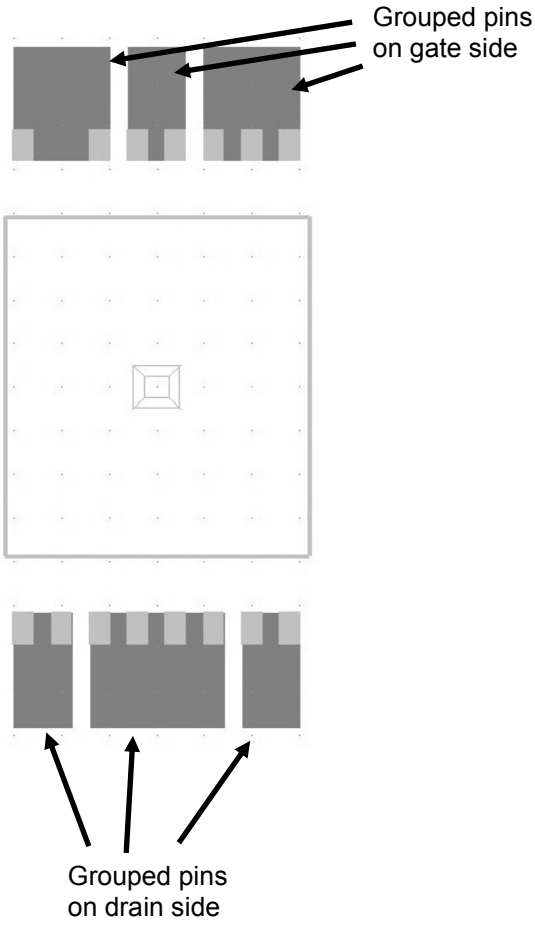
Fig. 9 Footprint and PCB layout

For optimum results, multiple pins of the same type should be grouped together on the PCB as shown below. This assures wide traces to the attached driver and load, minimizing parasitic inductance. The source pin groups, SG1, SG2, SD1, SD2, are all source connections at the die. For best operation, the source groups would be ideally incorporated into a large contiguous ground plane on the same side of mounting on the circuit board. In other words, instead of routing ground traces to the device during layout, the footprint would be set over a large ground plane with drain and gate traces routed out of the ground plane. This is done during layout by first establishing a polygon that covers the entire PCB, representing the ground plane, and that is 'poured' by the layout software around needed traces.



inch/mm





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