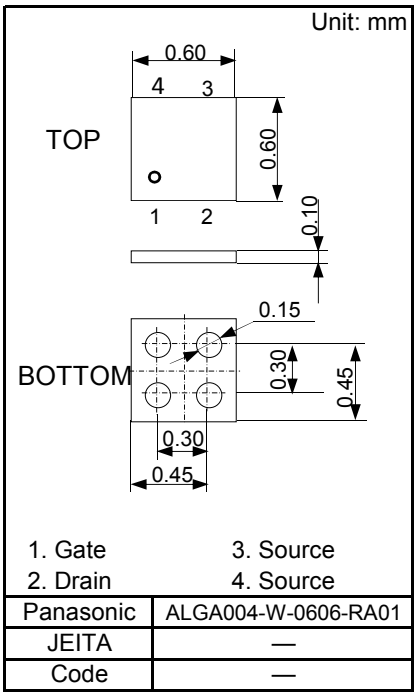
# FJ4B01110L

## Single P-channel MOS FET

For Load switching circuits




| | |
|---|---|
| Panasonic | ALGA004-W-0606-RA01 |
| JEITA | — |
| Code | — |

■ Features

- Drain-source ON resistance:Rds(on) typ. = 141 mΩ ( VGS = -2.5 V )
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

■ Marking Symbol: 1E

■ Packaging

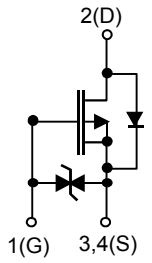
Embossed type (Thermo-compression sealing) : 20 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

| Parameter | Symbol | Rating | Unit |
|---|---|---|---|
| Drain-Source Voltage | VDS | -12 | V |
| Gate-Source Voltage | VGS | ±8 | V |
| Drain Current | ID1*1 | -1.4 | A |
| | ID2*2 | -2.2 | |
| | ID3*3 | -2.6 | |
| Peak Drain Current | IDp1*1*4 | -11 | A |
| | IDp2*2*4 | -17 | |
| | IDp3*3*4 | -20 | |
| Power Dissipation | PD1*1 | 0.34 | W |
| | PD2*2 | 0.76 | |
| | PD3*3 | 1.1 | |
| Channel Temperature | Tch | 150 | °C |
| Operating Ambient Temperature | Topr | -40 ~ +85 | °C |
| Storage Temperature | Tstg | -55 ~ +150 | °C |

Note *1 FR4 board (25.4mm×25.4mm×t1.0mm)、Min Cu 36mm$^2$ Copper
*2 FR4 board (25.4mm×25.4mm×t1.0mm)、Full Cu
*3 Ceramic substrate (70mm×70mm×t1.0mm)
*4 t = 10 µs, Duty Cycle < 1%

■ Internal Connection



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■ Electrical Characteristics Ta = 25 ºC ± 3 ºC

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Breakdown Voltage | VDSS | ID = -1 mA, VGS = 0 | -12 | | | V |
| Zero Gate Voltage Drain Current | IDSS | VDS = -12 V, VGS = 0 | | | -10 | μA |
| Gate-Source Leakage Current | IGSS | VGS = ±8 V, VDS = 0 V | | | ±10 | μA |
| Gate Threshold Voltage | Vth | ID = -0.598 mA, VDS =-10 V | -0.3 | | -1.0 | V |
| Drain-Source ON Resistance | RDS(on) | ID = -0.7 A, VGS = -4.5 V | | 118 | 153 | mΩ |
| | | ID = -0.7 A, VGS = -2.5 V | | 141 | 183 | |
| | | ID = -0.2 A, VGS = -1.8 V | | 169 | 287 | |
| | | ID = -0.1 A, VGS = -1.5 V | | 199 | 597 | |
| Input Capacitance *1 | Ciss | VDS = -10 V<br>VGS = 0<br>f = 1MHz | | 226 | | pF |
| Output Capacitance *1 | Coss | | | 62 | | |
| Reverse Transfer Capacitance *1 | Crss | | | 51 | | |
| Turn-on delay time *1,*2 | td(on) | VDD = -6 V<br>VGS = 0 to -4.5 V<br>ID = -1.0 A | | 3.8 | | ns |
| Rise time *1,*2 | tr | | | 2.5 | | |
| Turn-off delay time *1,*2 | td(off) | | | 30 | | |
| Fall time *1,*2 | tf | | | 5.4 | | |
| Total Gate Charge *1 | Qg | VDD = -6 V<br>VGS = -4.5 V<br>ID = -1.0 A | | 3.3 | | nC |
| Gate to Source Charge *1 | Qgs | | | 0.55 | | nC |
| Gate to Drain Miller Charge *1 | Qgd | | | 0.65 | | nC |
| Body Diode Forward Voltage | VF(D-S) | IF = -0.2A, VGS = 0V | | -0.7 | -1.2 | V |

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.
*1 Guaranteed by design, not subject to production testing
*2 Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

■ Electrical State Discharge Characteristics

| Standard | Test Type | Symbol | Conditions | Class | Value | Unit |
|---|---|---|---|---|---|---|
| AEC-Q101-001 | Human body model | HBM | C = 100 pF, R = 1.5 kΩ | H1B | >500 to ≦ 1k | V |
| | Machine model | MM | C = 200 pF, R = 0 Ω | M1B | >50 to ≦ 100 | V |



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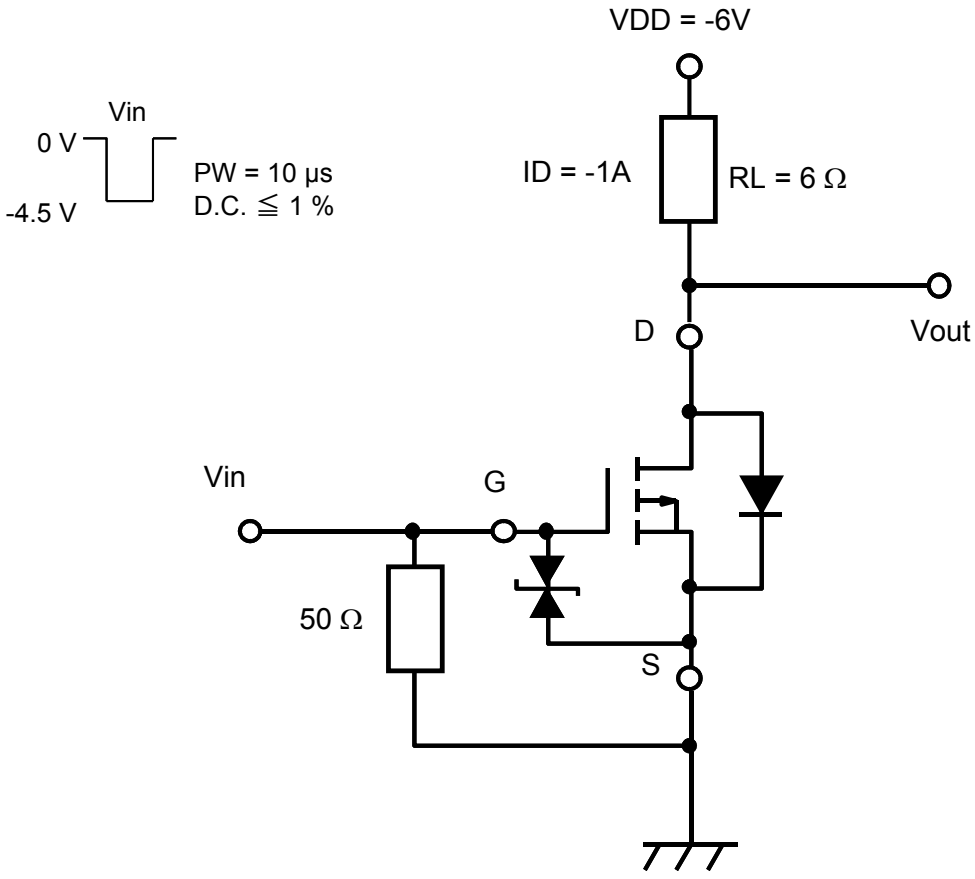
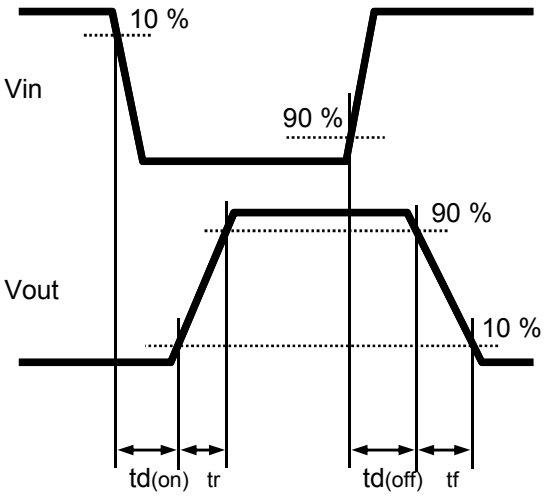
Note2: Measurement circuit



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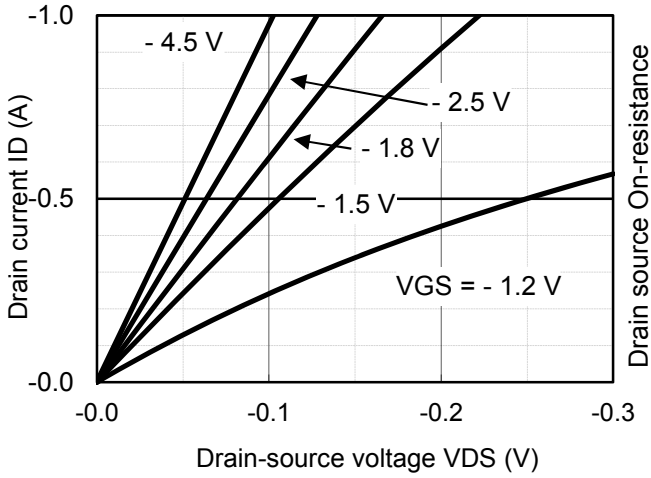
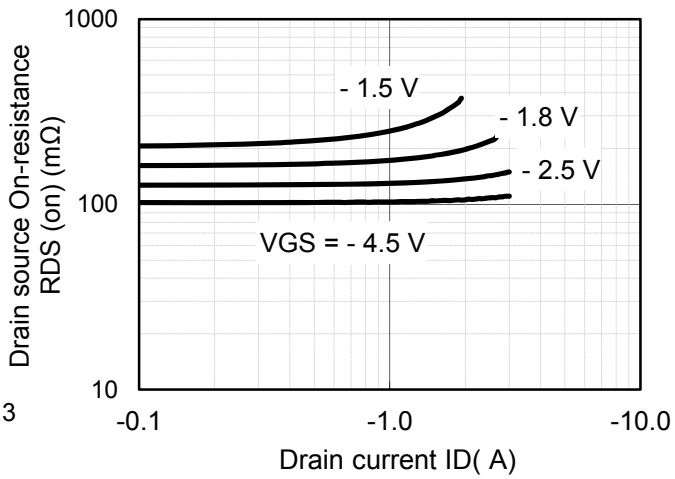
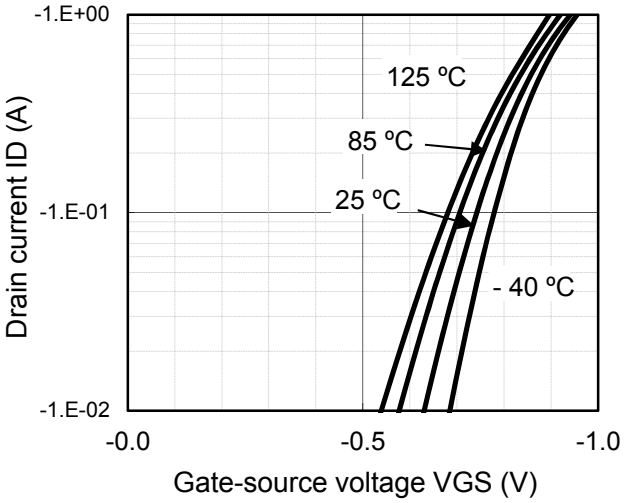
ID - VDS



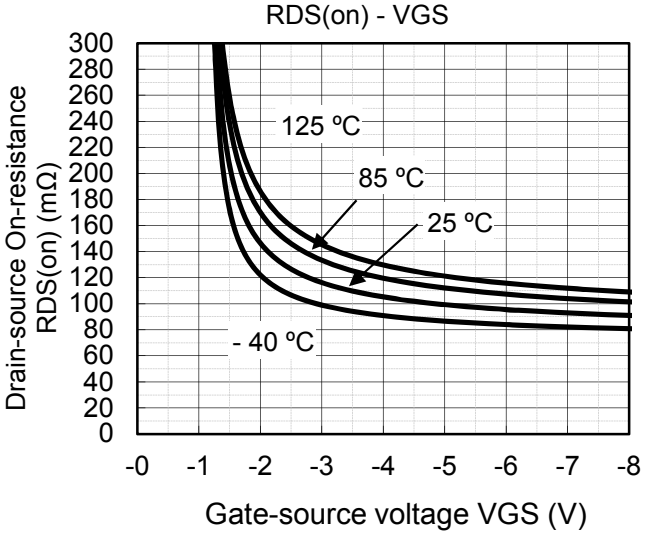

RDS(on) - ID



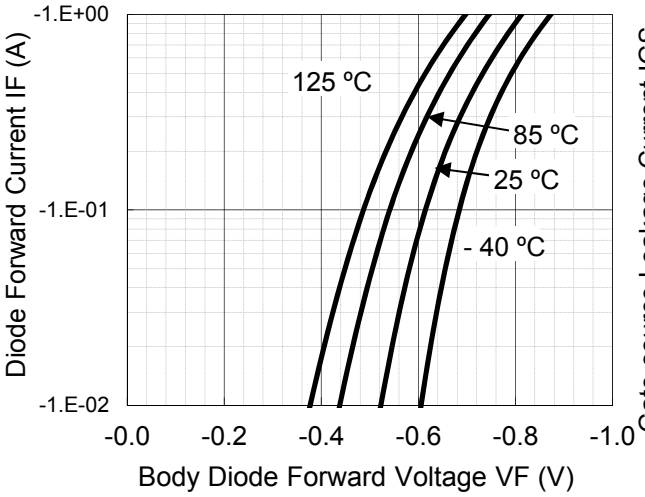

ID - VGS



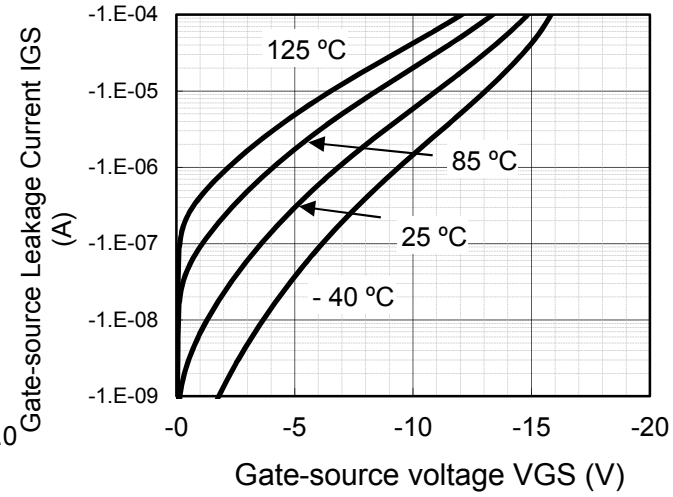

RDS(on) - VGS




IF - VF




IGS - VGS



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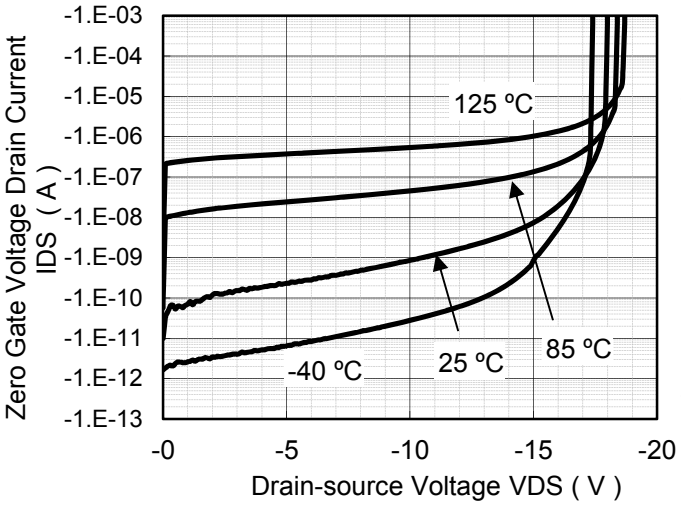
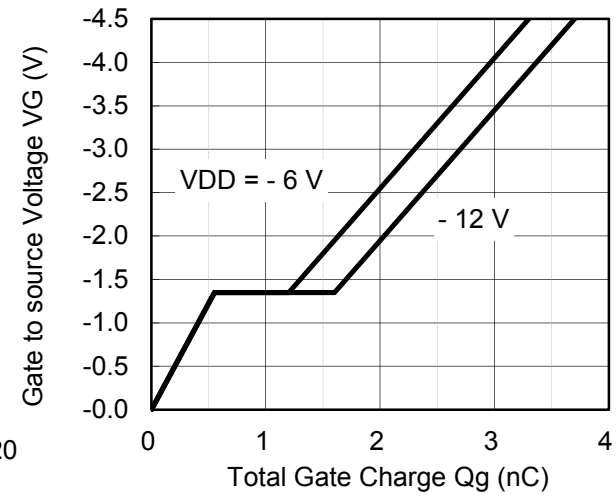
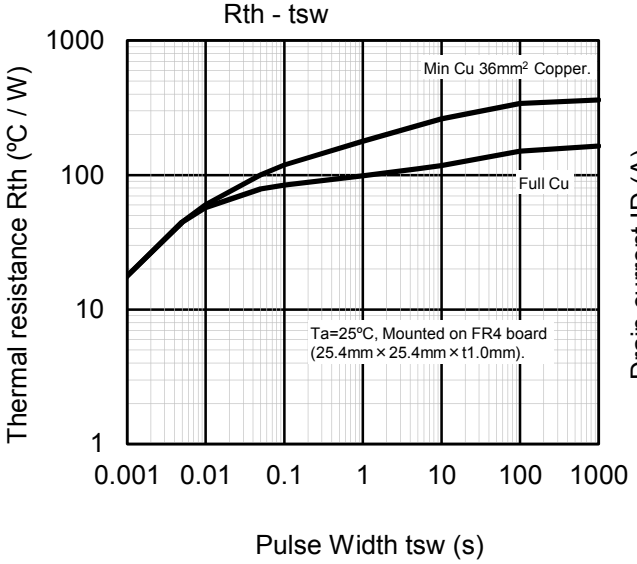
IDS - VDS



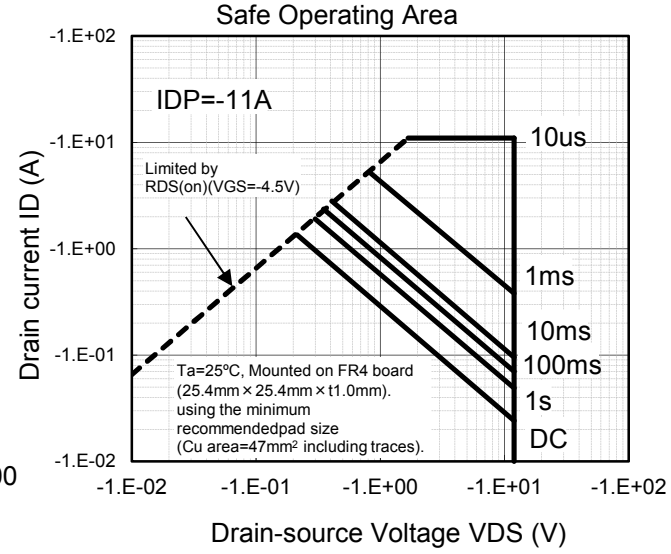

Dynamic Input/Output Characteristics




Rth - tsw




Safe Operating Area



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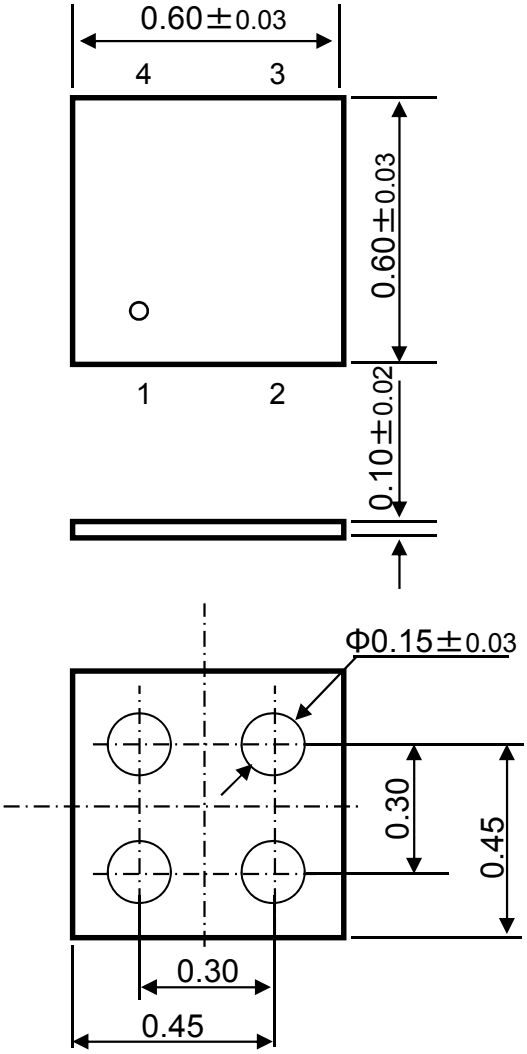
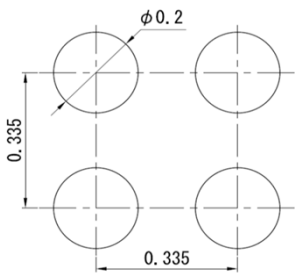
■ ALGA004-W-0606-RA01

Unit: mm




■ Land Pattern (Reference)



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