

MAX44244/MAX44245/MAX44248

36V, Precision, Low-Power, 90 μ A, Single/Quad/Dual Op Amps

General Description

The MAX44244/MAX44245/MAX44248 family of parts provide ultra-precision, low-noise, zero-drift single/quad/dual operational amplifiers featuring very low-power operation with a wide supply range. The devices incorporate a patented auto-zero circuit that constantly measures and compensates the input offset to eliminate drift over time and temperature as well as the effect of 1/f noise. These devices also feature integrated EMI filters to reduce high-frequency signal demodulation on the output. The op amps operate from either a single 2.7V to 36V supply or dual $\pm 1.35V$ to $\pm 18V$ supply. The devices are unity-gain stable with a 1MHz gain-bandwidth product and a low 90 μ A supply current per amplifier.

The low offset and noise specifications and high supply range make the devices ideal for sensor interfaces and transmitters.

The devices are available in μ MAX®, SO, SOT23, and TSSOP packages and are specified over the -40°C to +125°C automotive operating temperature range.

Applications

Sensors Interfaces
 4-20mA and 0 to 10V Transmitters
 PLC Analog I/O Modules
 Weight Scales
 Portable Medical Devices

Features

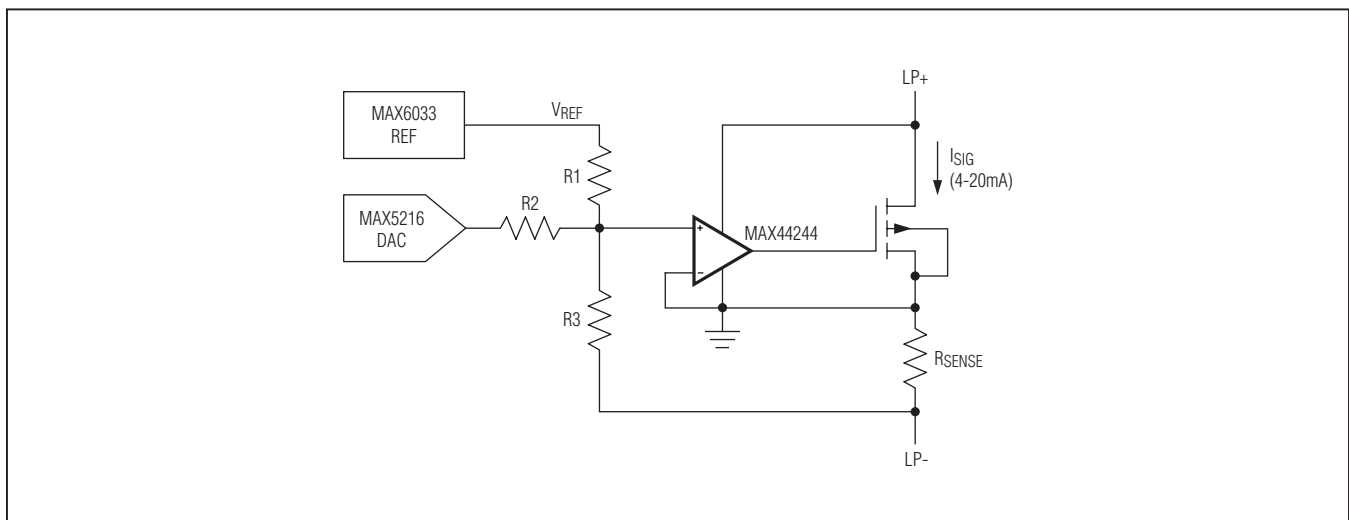
- ◆ Very Low Input Voltage Offset 7.5 μ V (max)
- ◆ Low 30nV/°C Offset Drift (max)
- ◆ Low 90 μ A Quiescent Current per Amplifier
- ◆ Low Input Noise
 50nV/ $\sqrt{\text{Hz}}$ at 1kHz
 0.5 μ V_{p-p} from 0.1Hz to 10Hz
- ◆ 1MHz Gain-Bandwidth Product
- ◆ EMI Suppression Circuitry
- ◆ Rail-to-Rail Output
- ◆ 2.7V to 36V Supply Range
- ◆ μ MAX, SO, SOT23, TSSOP packages

[Ordering Information](#) appears at end of data sheet.

For related parts and recommended products to use with this part, refer to www.maximintegrated.com/MAX44244.related.

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Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maximintegrated.com.

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ABSOLUTE MAXIMUM RATINGS

V_{DD} to V_{SS}	-0.3V to +40V	Operating Temperature Range	-40°C to +125°C
Common-Mode Input Voltage	($V_{SS} - 0.3V$) to ($V_{DD} + 0.3V$)	Storage Temperature	-65°C to +150°C
Differential Input Voltage IN_+ , IN_-	6V	Junction Temperature	+150°C
Continuous Input Current Into Any Pin	±20mA	Lead Temperature (soldering, 10s)	+300°C
Output Voltage to V_{SS} (OUT_-)	- 0.3V to ($V_{DD} + 0.3V$)	Soldering Temperature (reflow)	+260°C
Output Short-Circuit Duration (OUT_-)	1s		

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

SO-8	Junction-to-Ambient Thermal Resistance (θ_{JA})	132°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	38°C/W	TSSOP	Junction-to-Ambient Thermal Resistance (θ_{JA})	110°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	30°C/W
SO-14	Junction-to-Ambient Thermal Resistance (θ_{JA})	120°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	37°C/W	µMAX	Junction-to-Ambient Thermal Resistance (θ_{JA})	206.3°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	42°C/W
SOT23	Junction-to-Ambient Thermal Resistance (θ_{JA})	324.3°C/W	Junction-to-Case Thermal Resistance (θ_{JC})	82°C/W					

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to www.maximintegrated.com/thermal-tutorial.

ELECTRICAL CHARACTERISTICS

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $+25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Supply Voltage Range	V_{DD}	Guaranteed by PSRR	2.7		36	V
Power-Supply Rejection Ratio (Note 3)	PSRR	$T_A = +25^\circ C$, $V_{IN+} = V_{IN-} = V_{DD}/2 - 1V$	140	148		dB
		$-40^\circ C < T_A < +125^\circ C$	133			
Quiescent Current per Amplifier	I_{DD}	$T_A = +25^\circ C$		90	130	µA
		$-40^\circ C < T_A < +125^\circ C$			145	
DC SPECIFICATIONS						
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	$V_{SS} - 0.05$		$V_{DD} - 1.5$	V
Common-Mode Rejection Ratio (Note 3)	CMRR	$T_A = +25^\circ C$, $V_{CM} = V_{SS} - 0.05V$ to $V_{DD} - 1.5V$	126	130		dB
		$-40^\circ C < T_A < +125^\circ C$, $V_{CM} = V_{SS} - 0.05V$ to $V_{DD} - 1.5V$	120			
Input Offset Voltage (Note 3)	V_{OS}	$T_A = +25^\circ C$		2	7.5	µV
		$-40^\circ C < T_A < +125^\circ C$			10	
Input Offset Voltage Drift (Note 3)	$TC V_{OS}$			10	30	nV/°C

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $+25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Input Bias Current (Note 3)	I_B	$T_A = +25^\circ C$			150	300	pA
		$-40^\circ C < T_A < +125^\circ C$				700	
Input Offset Current (Note 3)	I_{OS}	$T_A = +25^\circ C$			300	600	pA
		$-40^\circ C < T_A < +125^\circ C$				1400	
Open-Loop Gain (Note 3)	A_{VOL}	$V_{SS} + 0.5V \leq V_{OUT} \leq V_{DD} - 0.5V$	$T_A = +25^\circ C$	140	150		dB
			$-40^\circ C < T_A < +125^\circ C$	135			
Output Short-Circuit Current		To V_{DD} or V_{SS} , noncontinuous			40		mA
Output Voltage Swing	$V_{DD} - V_{OUT}$	$T_A = +25^\circ C$				80	mV
		$-40^\circ C < T_A < +125^\circ C$				110	
	$V_{OUT} - V_{SS}$	$T_A = +25^\circ C$				50	
		$-40^\circ C < T_A < +125^\circ C$				75	
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	$f = 1kHz$			50		nV/\sqrt{Hz}
Input Voltage Noise		$0.1Hz < f < 10Hz$			500		nV_{p-p}
Input Current-Noise Density	i_N	$f = 1kHz$			0.1		pA/\sqrt{Hz}
Gain-Bandwidth Product	GBW				1		MHz
Slew Rate	SR	$A_V = 1V/V$, $V_{OUT} = 2V_{p-p}$			0.7		$V/\mu s$
Capacitive Loading	C_L	No sustained oscillation, $A_V = 1V/V$			400		pF
Total Harmonic Distortion Plus Noise	THD+N	$V_{OUT} = 2V_{p-p}$, $A_V = +1V/V$, $f = 1kHz$			-100		dB
EMI Rejection Ratio	EMIRR	$V_{RF_PEAK} = 100mV$	$f = 400MHz$		75		dB
			$f = 900MHz$		78		
			$f = 1800MHz$		80		
			$f = 2400MHz$		90		

ELECTRICAL CHARACTERISTICS

($V_{DD} = 30V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $+25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER SUPPLY						
Quiescent Current per Amplifier	I_{DD}	$T_A = +25^\circ C$		90	130	μA
		$-40^\circ C < T_A < +125^\circ C$			145	
DC SPECIFICATIONS						
Input Common-Mode Range	V_{CM}	Guaranteed by CMRR test	$V_{SS} - 0.05$		$V_{DD} - 1.5$	V

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ELECTRICAL CHARACTERISTICS (continued)

($V_{DD} = 30V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$, $T_A = -40^\circ C$ to $+125^\circ C$, unless otherwise noted. Typical values are at $+25^\circ C$.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Common-Mode Rejection Ratio (Note 3)	CMRR	$T_A = +25^\circ C$, $V_{CM} = V_{SS} - 0.05V$ to $V_{DD} - 1.5V$		130	140		dB
		$-40^\circ C < T_A < +125^\circ C$, $V_{CM} = V_{SS} - 0.05V$ to $V_{DD} - 1.5V$		126			
Input Offset Voltage (Note 3)	V_{OS}	$T_A = +25^\circ C$			2	7.5	μV
		$-40^\circ C < T_A < +125^\circ C$				10	
Input Offset Voltage Drift (Note 3)	TC V_{OS}				10	30	nV/ $^\circ C$
Input Bias Current (Note 3)	I_B	$T_A = +25^\circ C$			150	300	μA
		$-40^\circ C < T_A < +125^\circ C$				700	
Input Offset Current (Note 3)	I_{OS}	$T_A = +25^\circ C$			300	600	μA
		$-40^\circ C < T_A < +125^\circ C$				1400	
Open-Loop Gain (Note 3)	A_{VOL}	$V_{SS} + 0.5V \leq V_{OUT} \leq V_{DD} - 0.5V$	$T_A = +25^\circ C$	146	150		dB
			$-40^\circ C < T_A < +125^\circ C$	140			
Output Short-Circuit Current		To V_{DD} or V_{SS} , noncontinuous			40		mA
Output Voltage Swing	$V_{DD} - V_{OUT}$	$T_A = +25^\circ C$				200	mV
		$-40^\circ C < T_A < +125^\circ C$				270	
	$V_{OUT} - V_{SS}$	$T_A = +25^\circ C$				140	
		$-40^\circ C < T_A < +125^\circ C$				220	
AC SPECIFICATIONS							
Input Voltage-Noise Density	e_N	$f = 1kHz$			50		nV/ \sqrt{Hz}
Input Voltage Noise		$0.1Hz < f < 10Hz$			500		nV _{P-P}
Input Current-Noise Density	i_N	$f = 1kHz$			0.1		pA/ \sqrt{Hz}
Gain-Bandwidth Product	GBW				1		MHz
Slew Rate	SR	$A_V = 1V/V$, $V_{OUT} = 2V_{P-P}$			0.7		V/ μs
Capacitive Loading	C_L	No sustained oscillation, $A_V = 1V/V$			400		pF
Total Harmonic Distortion Plus Noise	THD+N	$V_{OUT} = 2V_{P-P}$, $A_V = +1V/V$, $f = 1kHz$			-100		dB
EMI Rejection Ratio	EMIRR	$V_{RF_PEAK} = 100mV$	$f = 400MHz$		75		dB
			$f = 900MHz$		78		
			$f = 1800MHz$		80		
			$f = 2400MHz$		90		

Note 2: All devices are 100% production tested at $T_A = +25^\circ C$. Temperature limits are guaranteed by design.

Note 3: Guaranteed by design.

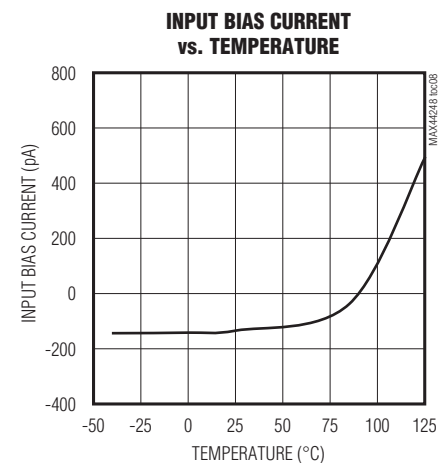
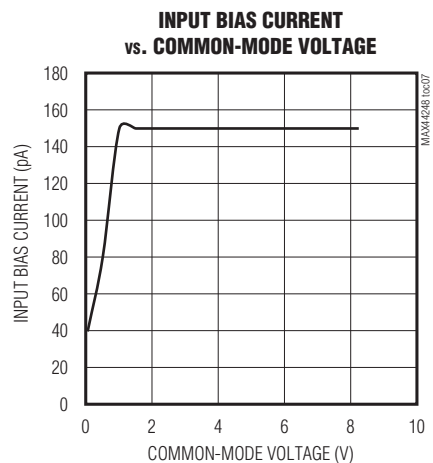
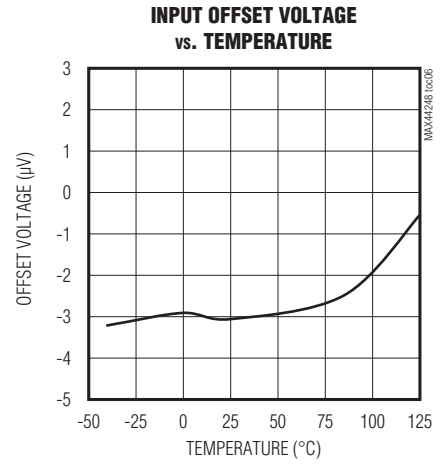
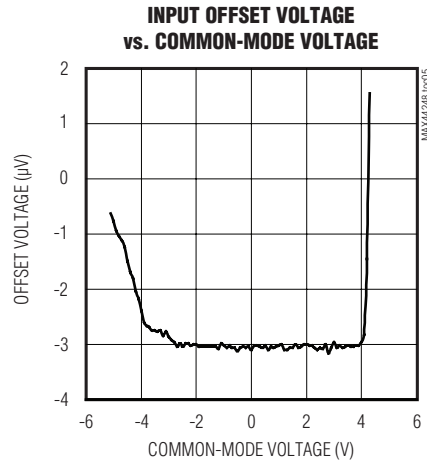
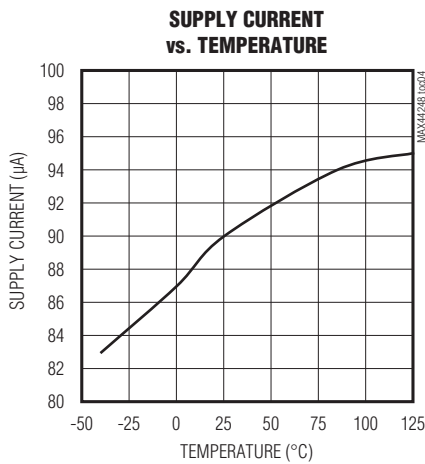
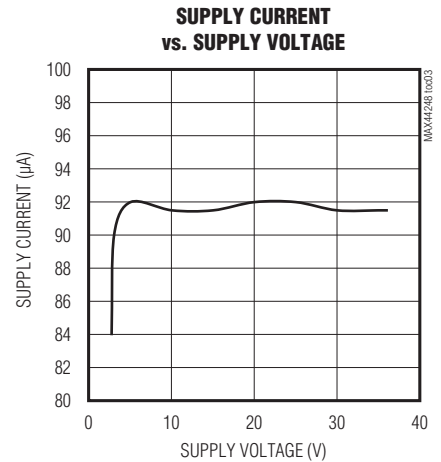
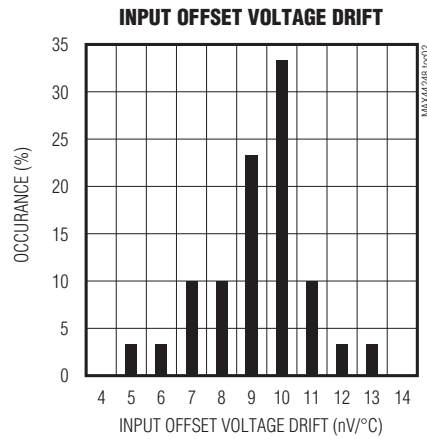
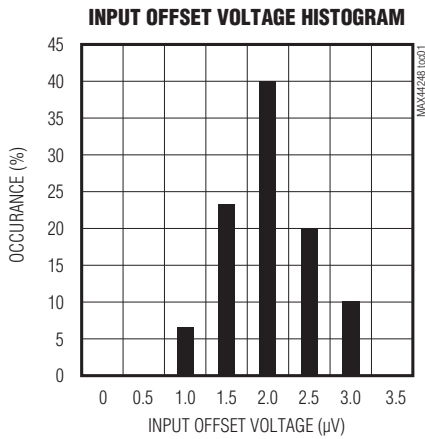
Note 4: At $IN+$ and $IN-$. Defined as $20\log(V_{RF_PEAK}/\Delta V_{OS})$.

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Typical Operating Characteristics

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$. Typical values are at $T_A = +25^\circ C$.)



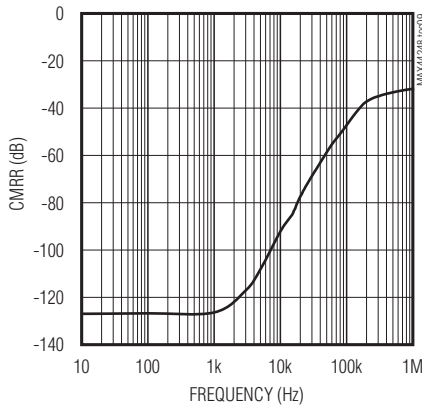
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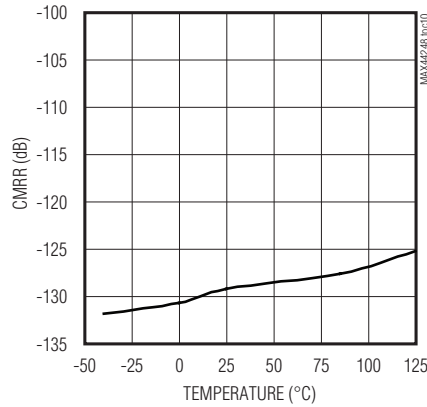
Typical Operating Characteristics (continued)

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$. Typical values are at $T_A = +25^\circ C$.)

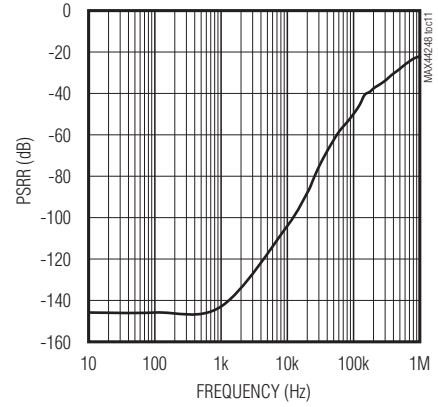
COMMON-MODE REJECTION RATIO vs. FREQUENCY



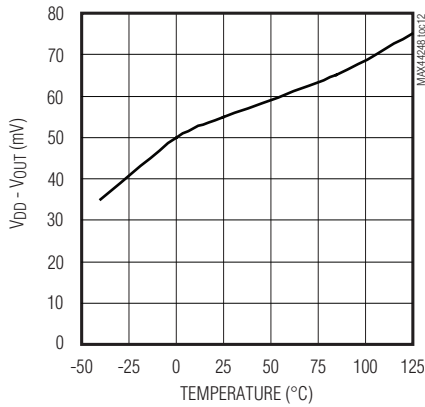
COMMON-MODE REJECTION RATIO vs. TEMPERATURE



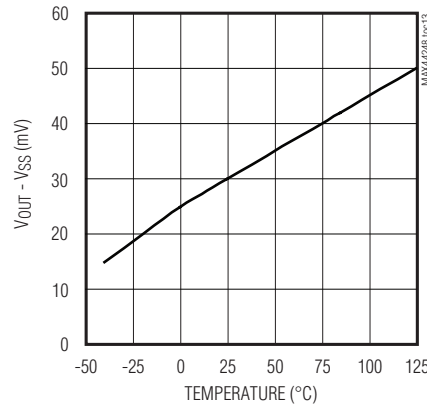
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



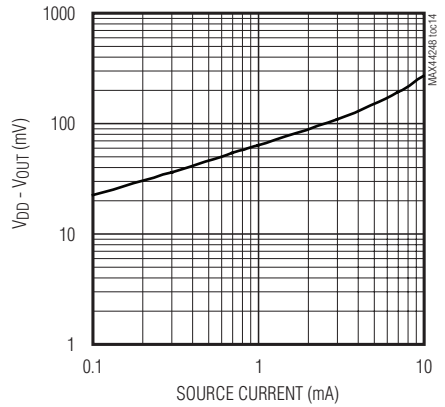
OUTPUT VOLTAGE HIGH vs. TEMPERATURE



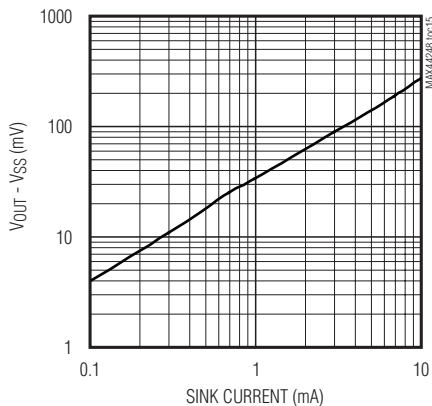
OUTPUT VOLTAGE LOW vs. TEMPERATURE



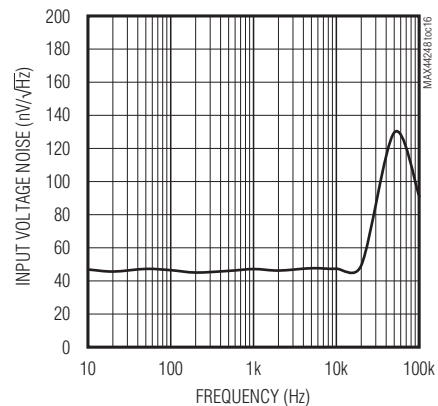
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT



OUTPUT VOLTAGE LOW vs. SINK CURRENT



INPUT VOLTAGE NOISE vs. FREQUENCY



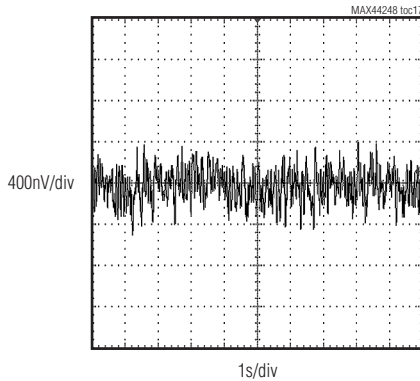
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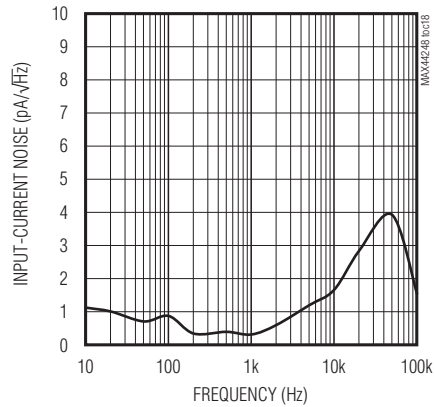
Typical Operating Characteristics (continued)

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$. Typical values are at $T_A = +25^\circ C$.)

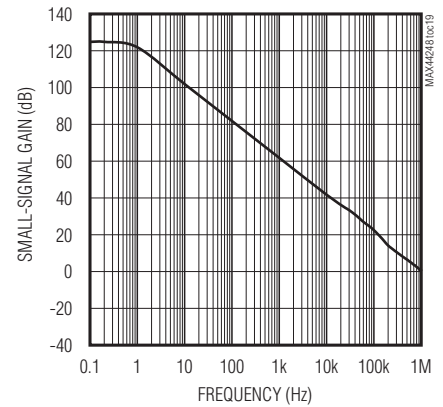
INPUT VOLTAGE 0.1Hz TO 10Hz NOISE



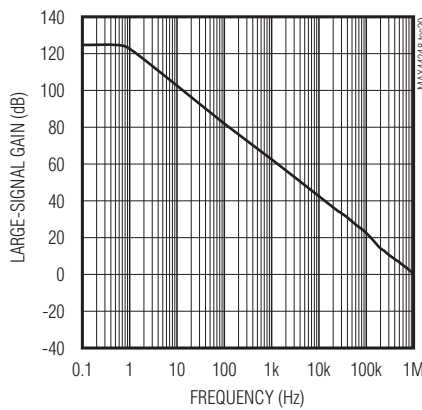
INPUT CURRENT NOISE vs. FREQUENCY



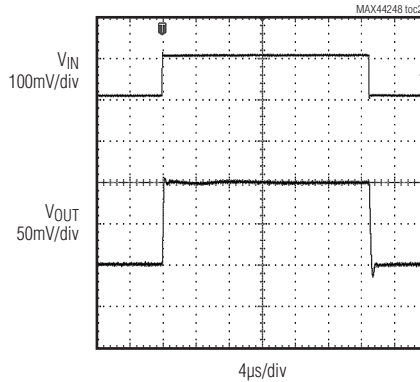
SMALL-SIGNAL GAIN vs. FREQUENCY



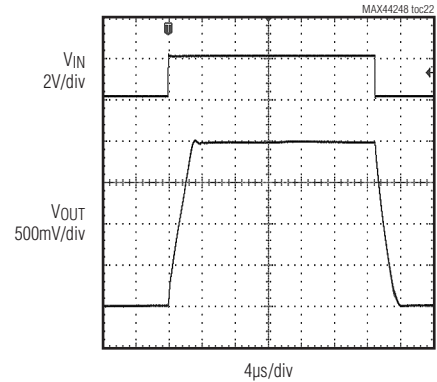
LARGE-SIGNAL GAIN vs. FREQUENCY



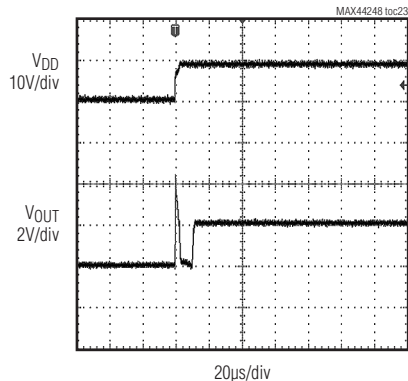
SMALL-SIGNAL STEP RESPONSE



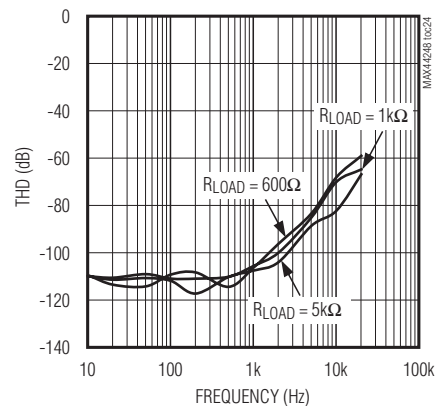
LARGE-SIGNAL STEP RESPONSE



POWER-UP TIME



TOTAL HARMONIC DISTORTION vs. FREQUENCY

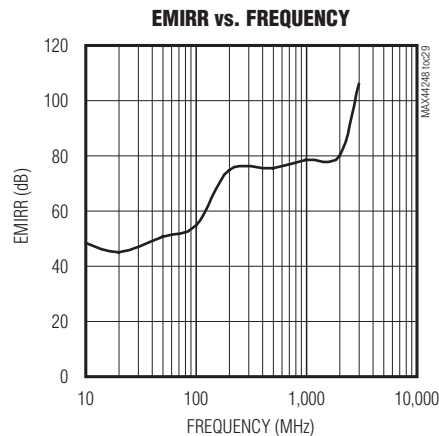
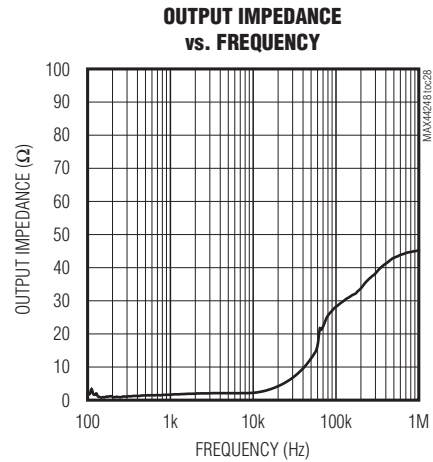
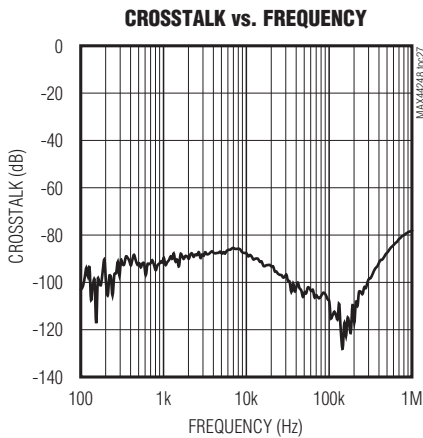
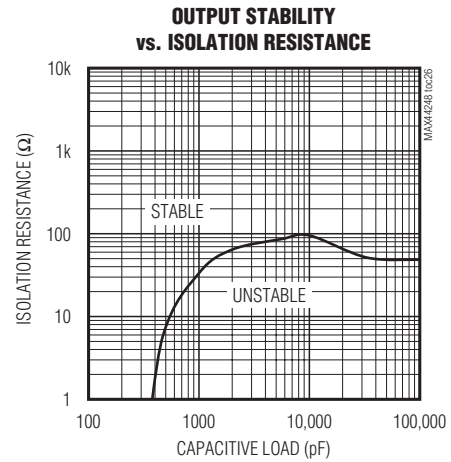
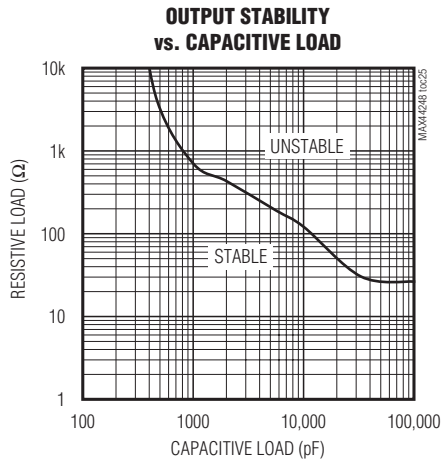


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Typical Operating Characteristics (continued)

($V_{DD} = 10V$, $V_{SS} = 0V$, $V_{IN+} = V_{IN-} = V_{DD}/2$, $R_L = 5k\Omega$ to $V_{DD}/2$. Typical values are at $T_A = +25^\circ C$.)

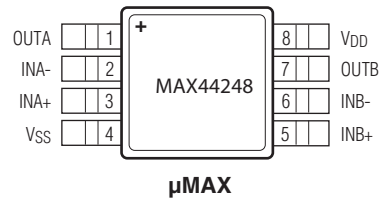
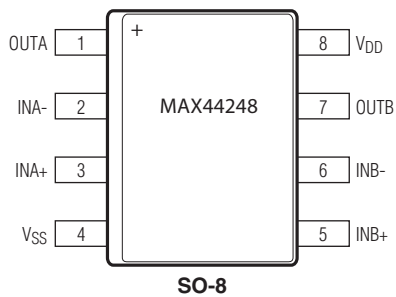
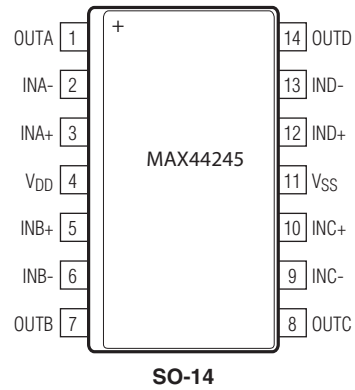
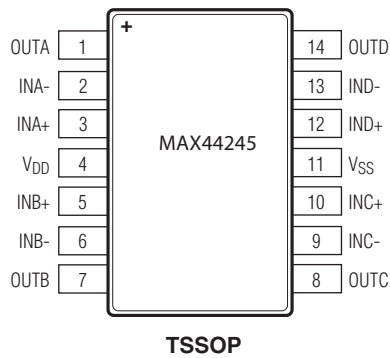
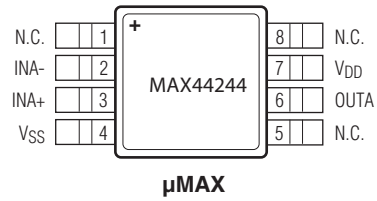
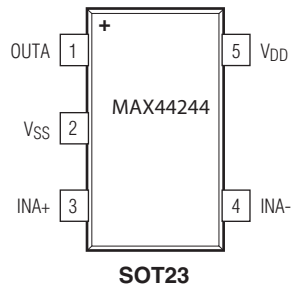


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Pin Configurations

TOP VIEW



MAX44244/MAX44245/MAX44248

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Pin Description

PIN						NAME	FUNCTION
MAX44244		MAX44245		MAX44248			
SOT23	μ MAX	SO-14	TSSOP	SO-8	μ MAX		
1	6	1	1	1	1	OUTA	Channel A Output
2	4	11	11	4	4	V _{SS}	Negative Supply Voltage
3	3	3	3	3	3	INA+	Channel A Positive Input
4	2	2	2	2	2	INA-	Channel A Negative Input
5	7	4	4	8	8	V _{DD}	Positive Supply Voltage
—	—	5	5	5	5	INB+	Channel B Positive Input
—	—	6	6	6	6	INB-	Channel B Negative Input
—	—	7	7	7	7	OUTB	Channel B Output
—	—	8	8	—	—	OUTC	Channel C Output
—	—	9	9	—	—	INC-	Channel C Negative Input
—	—	10	10	—	—	INC+	Channel C Positive Input
—	—	12	12	—	—	IND+	Channel D Positive Input
—	—	13	13	—	—	IND-	Channel D Negative Input
—	—	14	14	—	—	OUTD	Channel D Output
—	1, 5, 8	—	—	—	—	N.C.	No Connection. Not internally connected.

Detailed Description

The MAX44244/MAX44245/MAX44248 are high-precision amplifiers with less than 2 μ V (typ) input-referred offset and low input voltage-noise density at 10Hz. 1/f noise, in fact, is eliminated to improve the performance in low-frequency applications. These characteristics are achieved through an auto-zeroing technique that cancels the input offset voltage and 1/f noise of the amplifier.

External Noise Suppression in EMI Form

These devices have input EMI filters to prevent effects of radio frequency interference on the output. The EMI filters comprise passive devices that present significant higher impedance to higher frequency signals. See the EMIRR vs. Frequency graph in the *Typical Operating Characteristics* section for details.

High Supply Voltage Range

The devices feature 90 μ A current consumption per channel and a voltage supply range from either 2.7V to 36V single supply or \pm 1.35V to \pm 18V split supply.

Applications Information

The devices feature ultra-high precision operational amplifiers with a high supply voltage range designed for load cell, medical instrumentation, and precision instrument applications.

4–20mA Current-Loop Communication

Industrial environments typically have a large amount of broadcast electromagnetic interference (EMI) from high-voltage transients and switching motors. This combined with long cables for sensor communication leads to high-voltage noise on communication lines. Current-Loop communication is resistant to this noise because the EMI induced current is low. This configuration also allows for low-power sensor applications to be powered from the communication lines.

The *Typical Operating Circuit* shows how the device can be used to make a current loop driver.

The circuit uses low-power components such as the MAX44244 op amp, the 16-bit MAX5216 DAC, and the high-precision 60 μ A-only MAX6033 reference. In this

MAX44244/MAX44245/MAX44248

36V, Precision, Low-Power, 90 μ A, Single/Quad/Dual Op Amps

circuit, both the DAC and the reference are referred to the local ground. The MAX44244 op-amp inputs are capable of swinging to the negative supply (which is the local ground in this case). R3 acts as a current mirror with R_{SENSE}. Therefore, if R_{SENSE} = 50 Ω (i.e. 20mA will drop 1V) and if the current through R3 is 10 μ A when I_{OUT} is 20mA (0.05% error) then R3 = 100k Ω . R1 is chosen along with the reference voltage to provide the 4mA offset. R2 = 512k Ω for 20mA full scale or R2 = 614k Ω for 20% over-range. R_{SENSE} is ratiometric with R3, R1 independently sets the offset current and R2 independently sets the DAC scaling.

Driving High-Performance ADCs

The MAX44244/MAX44245/MAX44248's low input offset voltage and low noise make these amplifiers ideal for ADC buffering. Weight scale applications require a low-noise, precision amplifier in front of an ADC. Figure 1 details an example of a load cell and amplifier driven from the same 5V supply, along with a 16-bit delta sigma ADC such as the MAX11205.

The MAX11205 is an ultra-low-power (< 300 μ A, max active current), high-resolution, serial output ADC. It provides the highest resolution per unit power in the industry and is optimized for applications that require very high dynamic range with low power such as sensors on a 4–20mA industrial control loop. The devices provide

a high-accuracy internal oscillator that requires no external components.

Layout Guidelines

The MAX44244/MAX44245/MAX44248 feature ultra-low input offset voltage and noise. Therefore, to get optimum performance follow the layout guidelines.

Avoid temperature gradients at the junction of two dissimilar metals. The most common dissimilar metals used on a PCB are solder-to-component lead and solder-to-board trace. Dissimilar metals create a local thermocouple. A variation in temperature across the board can cause an additional offset due to Seebeck effect at the solder junctions. To minimize the Seebeck effect, place the amplifier away from potential heat sources on the board, if possible. Orient the resistors such that both the ends are heated equally. It is a good practice to match the input signal path to ensure that the type and number of thermoelectric junctions remain the same. For example, consider using dummy 0 Ω resistors oriented in such a way that the thermoelectric source, due to the real resistors in the signal path, are cancelled. It is recommended to flood the PCB with ground plane. The ground plane ensures that heat is distributed uniformly reducing the potential offset voltage degradation due to Seebeck effect.

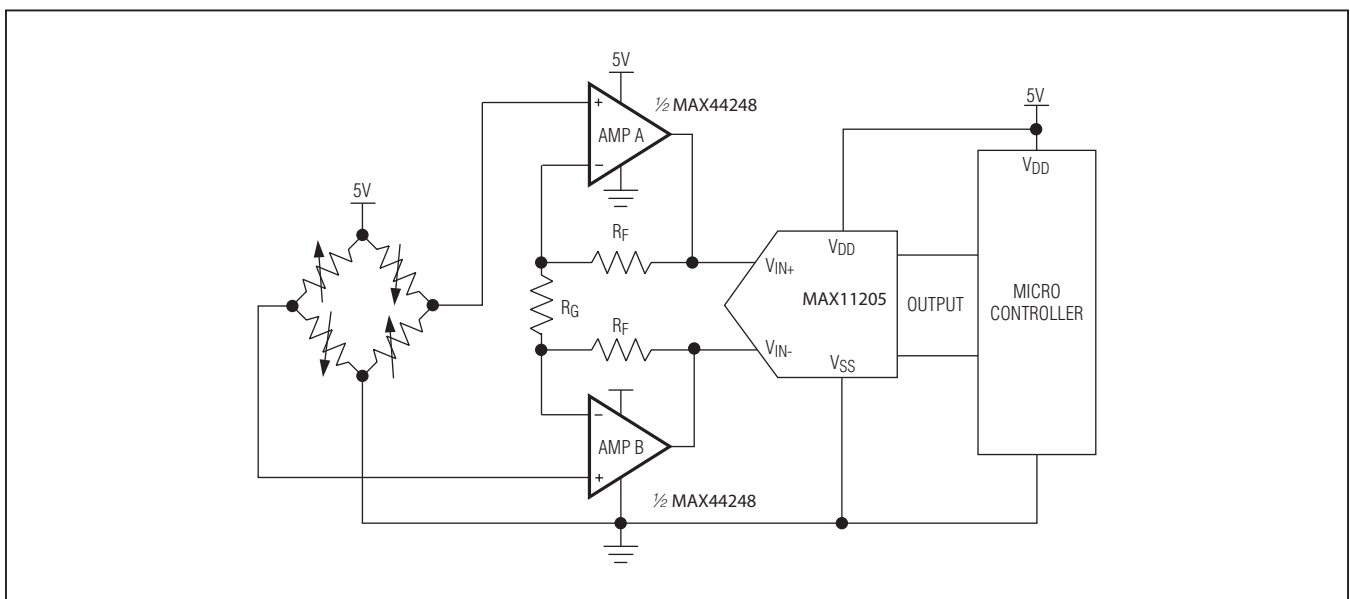


Figure 1. Weight Application

MAX44244/MAX44245/MAX44248

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Chip Information

PROCESS: BiCMOS

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX44244 AUK+*	-40°C to +125°C	5 SOT23	AFMR
MAX44244AUA+*	-40°C to +125°C	8 µMAX	—
MAX44245 ASD+	-40°C to +125°C	14 SO	—
MAX44245AUD+	-40°C to +125°C	14 TSSOP	—
MAX44248 AUA+	-40°C to +125°C	8 µMAX	—
MAX44248ASA+	-40°C to +125°C	8 SO	—

+Denotes a lead(Pb)-free/RoHS-compliant package.

*Future Product—Contact factory for availability.

Package Information

For the latest package outline information and land patterns (footprints), go to www.maximintegrated.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
5 SOT23	U5+1	21-0057	90-0174
8 SO	S8+4	21-0041	90-0096
8 µMAX	U8+1	21-0036	90-0092
14 SO	S14M+4	21-0041	90-0112
14 TSSOP	U14M-1	21-0066	90-0113

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Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	7/12	Initial release	—
1	6/13	Added the MAX44244/MAX44245 to data sheet. Updated the <i>Electrical Characteristics, Absolute Maximum Ratings, Pin Description, and Pin Configurations</i> .	1–13



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