DATA SHEET

74LV165

8-bit parallel-in/serial-out shift register

Philips
Semiconductors

PHILIPS

PHILIPS

8-bit parallel-in/serial-out shift register

74LV165

FEATURES

- Wide operating voltage: 1.0 to 5.5 V
- Optimized for low voltage applications: 1.0 to 3.6 V
- Accepts TTL input levels between V_{CC} = 2.7 V and V_{CC} = 3.6 V
- Typical V_{OLP} (output ground bounce) < 0.8 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Typical V_{OHV} (output V_{OH} undershoot) > 2 V at V_{CC} = 3.3 V, T_{amb} = 25°C
- Asynchronous 8-bit parallel load
- Synchronous serial input
- Output capability: standard
- I_{CC} category: MSI

DESCRIPTION

The 74LV165 is a low-voltage Si-gate CMOS device and is pin and function compatible with 74HC/HCT165.

The 74LV165 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and $\overline{Q}_7$) available from the last stage. When the parallel load ($\overline{PL}$) input is LOW, parallel data from the D_0 to D_7 inputs are loaded into the register asynchronously. When $\overline{PL}$ is HIGH, data enters the register serially at the D_S input and shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the Q_7 output to the D_S input of the succeeding stage.

The clock input is a gated-OR structure which allows one input to be used as an active LOW clock enable ($\overline{CE}$) input. The pin assignment for the CP and $\overline{CE}$ inputs is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of input $\overline{CE}$ should only take place while CP HIGH for predictable operation. Either the CP or the $\overline{CE}$ should be HIGH before the LOW-to-HIGH transition of $\overline{PL}$ to prevent shifting the data when $\overline{PL}$ is activated.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25°C; t_r = $t_f \leq$ 2.5 ns

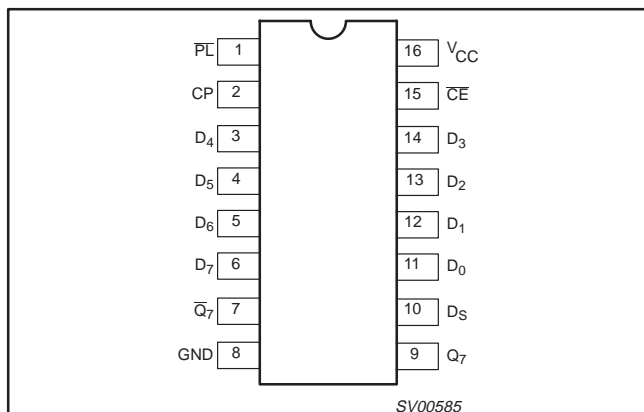| SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
t_{PHL}/t_{PLH}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$ $\overline{PL}$ to Q_7, $\overline{Q}_7$ D_7 to Q_7, $\overline{Q}_7$	C_L = 15 pF; V_{CC} = 3.3 V	18 18 14	ns
f_{max}	Maximum clock frequency		78	MHz
C_I	Input capacitance		3.5	pF
C_{PD}	Power dissipation capacitance per gate	V_{CC} = 3.3 V V_I = GND to V_{CC}[1]	35	pF

NOTES:
1. C_{PD} is used to determine the dynamic power dissipation (P_D in µW)
$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz; C_L = output load capacitance in pF;
f_o = output frequency in MHz; V_{CC} = supply voltage in V;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
16-Pin Plastic DIL	−40°C to +125°C	74LV165 N	74LV165 N	SOT38-4
16-Pin Plastic SO	−40°C to +125°C	74LV165 D	74LV165 D	SOT109-1
16-Pin Plastic SSOP Type II	−40°C to +125°C	74LV165 DB	74LV165 DB	SOT338-1
16-Pin Plastic TSSOP Type I	−40°C to +125°C	74LV165 PW	74LV165PW DH	SOT403-1

PIN CONFIGURATION

Pin	Signal		Pin	Signal
1	$\overline{PL}$		16	V_{CC}
2	CP		15	$\overline{CE}$
3	D_4		14	D_3
4	D_5		13	D_2
5	D_6		12	D_1
6	D_7		11	D_0
7	$\overline{Q}_7$		10	D_S
8	GND		9	Q_7

SV00585

PIN DESCRIPTION

| PIN NUMBER	SYMBOL	FUNCTION
1	$\overline{PL}$	Asynchronous parallel load input (active LOW)
2	CP	Clock input (LOW to HIGH, edge-triggered)
7	$\overline{Q}_7$	Complementary output from the last stage
8	GND	Ground (0 V)
9	Q_7	Serial output from last stage
10	D_S	Serial data input
11, 12, 13, 14, 3, 4, 5, 6	D_0 to D_7	Parallel data inputs
15	$\overline{CE}$	Clock enable input (active LOW)
16	V_{CC}	Positive supply voltage

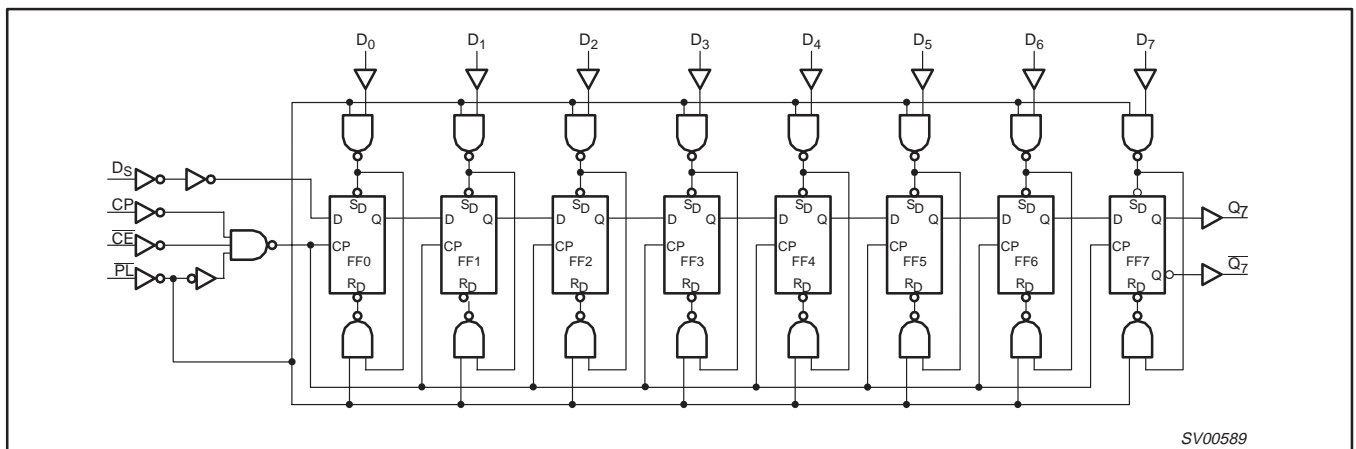## 8-bit parallel-in/serial-out shift register

LOGIC SYMBOL

SV00586

FUNCTIONAL DIAGRAM

SV00588
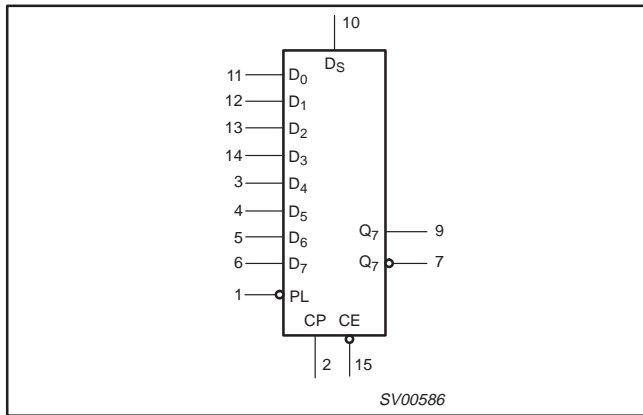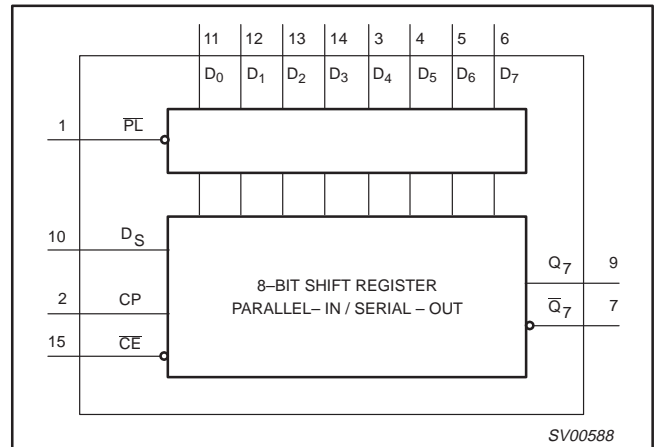
LOGIC SYMBOL (IEEE/IEC)

SV00587

LOGIC DIAGRAM

SV00589
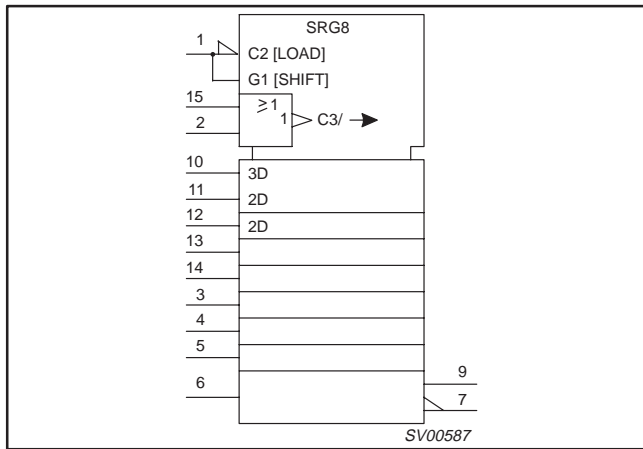
8-bit parallel-in/serial-out shift register

74LV165

FUNCTION TABLE

OPERATING MODES	INPUTS					Qn REGISTERS		OUTPUTS	
	$\overline{PL}$	$\overline{CE}$	CP	D_S	D_0–D_7	Q_0	Q_1–Q_6	Q_7	$\overline{Q}_7$
Parallel load	L	X	X	X	L	L	L–L	L	H
	L	X	X	X	H	H	H–H	H	L
Serial Shift	H	L	↑	l	X	L	q_0–q_5	q_6	$\overline{q}_6$
	H	L	↑	h	X	H	q_0–q_5	q_6	$\overline{q}_6$
Hold "do nothing"	H	H	X	X	X	q_0	q_1–q_6	q_7	q_7

NOTES:
H = HIGH voltage level
h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition
L = LOW voltage level
l = LOW voltage level level one set-up time prior to the LOW-to-HIGH clock transition
q = lower case letters indicate the state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition
X = don't care
↑ = LOW-to-HIGH clock transition

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	DC supply voltage	See Note 1	1.0	3.3	5.5	V
V_I	Input voltage		0	–	V_{CC}	V
V_O	Output voltage		0	–	V_{CC}	V
T_{amb}	Operating ambient temperature range in free air	See DC and AC characteristics	−40 −40		+85 +125	°C
t_r, t_f	Input rise and fall times	V_{CC} = 1.0V to 2.0V V_{CC} = 2.0V to 2.7V V_{CC} = 2.7V to 3.6V V_{CC} = 3.6V to 5.5V	– – – –	– – – –	500 200 100 50	ns/V

NOTE:
1. The LV is guaranteed to function down to V_{CC} = 1.0V (input levels GND or V_{CC}); DC characteristics are guaranteed from V_{CC} = 1.2V to V_{CC} = 5.5V.

ABSOLUTE MAXIMUM RATINGS[1, 2]

In accordance with the Absolute Maximum Rating System (IEC 134).
Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V_{CC}	DC supply voltage		−0.5 to +7.0	V
$\pm I_{IK}$	DC input diode current	V_I < −0.5 or V_I > V_{CC} + 0.5V	20	mA
$\pm I_{OK}$	DC output diode current	V_O < −0.5 or V_O > V_{CC} + 0.5V	50	mA
$\pm I_O$	DC output source or sink current – standard outputs	−0.5V < V_O < V_{CC} + 0.5V	25	mA
$\pm I_{GND}$, $\pm I_{CC}$	DC V_{CC} or GND current for types with – standard outputs		50	mA
T_{stg}	Storage temperature range		−65 to +150	°C
P_{TOT}	Power dissipation per package – plastic DIL – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	for temperature range: −40 to +125°C above +70°C derate linearly with 12 mW/K above +70°C derate linearly with 8 mW/K above +60°C derate linearly with 5.5 mW/K	750 500 400	mW

NOTES:
1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

8-bit parallel-in/serial-out shift register

74LV165

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			-40°C to +85°C			-40°C to +125°C		
			MIN	TYP[1]	MAX	MIN	MAX	
V_{IH}	HIGH level Input voltage	V_{CC} = 1.2 V	0.9			0.9		V
		V_{CC} = 2.0 V	1.4			1.4		
		V_{CC} = 2.7 to 3.6 V	2.0			2.0		
		V_{CC} = 4.5 to 5.5 V	$0.7 * V_{CC}$			$0.7 * V_{CC}$		
V_{IL}	LOW level Input voltage	V_{CC} = 1.2 V			0.3		0.3	V
		V_{CC} = 2.0 V			0.6		0.6	
		V_{CC} = 2.7 to 3.6 V			0.8		0.8	
		V_{CC} = 4.5 to 5.5			$0.3 * V_{CC}$		$0.3 * V_{CC}$	
V_{OH}	HIGH level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA		1.2				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	1.8	2.0		1.8		
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.5	2.7		2.5		
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	2.8	3.0		2.8		
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 100µA	4.3	4.5		4.3		
V_{OH}	HIGH level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 6mA	2.40	2.82		2.20		V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; $-I_O$ = 12mA	3.60	4.20		3.50		
V_{OL}	LOW level output voltage; all outputs	V_{CC} = 1.2 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0				V
		V_{CC} = 2.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 2.7 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 100µA		0	0.2		0.2	
V_{OL}	LOW level output voltage; STANDARD outputs	V_{CC} = 3.0 V; $V_I = V_{IH}$ or V_{IL}; I_O = 6mA		0.25	0.40		0.50	V
		V_{CC} = 4.5 V; $V_I = V_{IH}$ or V_{IL}; I_O = 12mA		0.35	0.55		0.65	
I_I	Input leakage current	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND			1.0		1.0	µA
I_{CC}	Quiescent supply current; MSI	V_{CC} = 5.5 V; $V_I = V_{CC}$ or GND; I_O = 0			20.0		160	µA
ΔI_{CC}	Additional quiescent supply current per input	V_{CC} = 2.7 V to 3.6 V; $V_I = V_{CC} - 0.6$ V			500		850	µA

NOTE:
1. All typical values are measured at T_{amb} = 25°C.

8-bit parallel-in/serial-out shift register

74LV165

AC CHARACTERISTICS

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	LIMITS					UNIT
				−40 to +85 °C			−40 to +125 °C		
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{PLH}/t_{PHL}	Propagation delay $\overline{CE}$, CP to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	115		–		ns
			2.0	–	38	61	–	76	
			2.7	–	27	43	–	54	
			3.0 to 3.6	–	22[2]	36	–	45	
			4.5 to 5.5	–	15	24	–	30	
t_{PLH}/t_{PHL}	Propagation delay $\overline{PL}$ to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	110		–		ns
			2.0	–	35	56	–	70	
			2.7	–	24	39	–	49	
			3.0 to 3.6	–	20[2]	33	–	41	
			4.5 to 5.5	–	14	22	–	27	
t_{PLH}/t_{PHL}	Propagation delay D_7 to Q_7, $\overline{Q}_7$	Figures 1, 2	1.2	–	90		–		ns
			2.0	–	28	45	–	56	
			2.7	–	20	32	–	40	
			3.0 to 3.6	–	17[2]	27	–	33	
			4.5 to 5.5	–	11	18	–	22	
t_w	Clock Pulse width HIGH or LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t_w	Parallel load pulse width LOW	Figures 1, 2	2.0	34	10	–	41	–	ns
			2.7	25	8	–	30	–	
			3.0 to 3.6	20	7[2]	–	24	–	
			4.5 to 5.5	15	5	–	18	–	
t_{rem}	Removal time $\overline{PL}$ to CP, $\overline{CE}$	Figures 1, 2	1.2	–	40	–	–	–	ns
			2.0	24	15	–	30	–	
			2.7	18	11	–	23	–	
			3.0 to 3.6	17	10[2]	–	21	–	
			4.5 to 5.5	12	7	–	15	–	
t_{su}	Set-up time D_S to CP, $\overline{CE}$	Figures 1, 2	1.2	–	−8	–	–	–	ns
			2.0	22	−2	–	26	–	
			2.7	16	−1	–	19	–	
			3.0 to 3.6	13	−1[2]	–	15	–	
			4.5 to 5.5	9	0	–	10	–	
t_{su}	Set-up time $\overline{CE}$ to CP; CP to $\overline{CE}$	Figures 1, 2	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4[2]	–	15	–	
			4.5 to 5.5	9	3	–	10	–	

8-bit parallel-in/serial-out shift register

74LV165

AC CHARACTERISTICS (*Continued*)

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L = 50$pF; $R_L = 1$KΩ

SYMBOL	PARAMETER	WAVEFORM	CONDITION	–40 to +85 °C			–40 to +125 °C		UNIT
			V_{CC}(V)	MIN	TYP[1]	MAX	MIN	MAX	
t_{su}	Set-up time D_n to $\overline{PL}$	Figures 1, 2	1.2	–	25	–	–	–	ns
			2.0	22	8	–	26	–	
			2.7	16	6	–	19	–	
			3.0 to 3.6	13	5[2]	–	15	–	
			4.5 to 5.5	9	4	–	10	–	
t_h	Hold time D_s to CP, $\overline{CE}$ D_n to $\overline{PL}$	Figures 1, 2	1.2	–	20	–	–	–	ns
			2.0	22	7	–	26	–	
			2.7	16	5	–	19	–	
			3.0 to 3.6	13	4	–	15	–	
			4.5 to 5.5	9	3	–	10	–	
t_h	Hold time $\overline{CE}$ to CP, CP to $\overline{CE}$	Figures 1, 2	1.2	–	–30	–	–	–	ns
			2.0	5	–8	–	5	–	
			2.7	5	–6	–	5	–	
			3.0 to 3.6	5	–5[2]	–	5	–	
			4.5 to 5.5	5	–4	–	5	–	
f_{max}	Maximum clock pulse frequency	Figures 1, 2	2.0	14	40	–	12	–	MHz
			2.7	19	60	–	16	–	
			3.0 to 3.6	24	65[2]	–	20	–	
			4.5 to 5.5	36	75	–	30	–	

NOTES:
1. Unless otherwise stated, all typical values are measured at $T_{amb} = 25°C$
2. Typical values are measured at $V_{CC} = 3.3$ V.

AC WAVEFORMS

$V_M = 1.5$ V at $V_{CC} \geq 2.7$ V.
$V_M = 0.5 \times V_{CC}$ at $V_{CC} < 2.7$ V;
V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
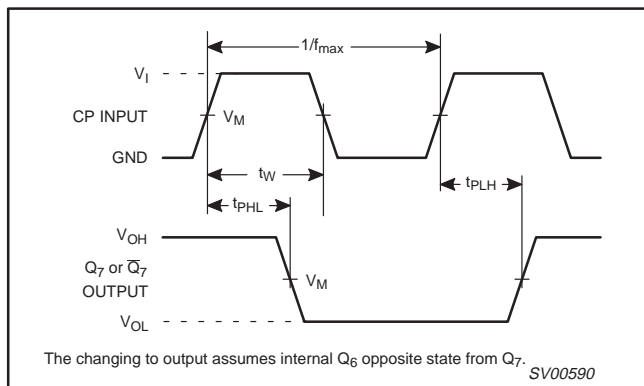

SV00590

Figure 1. Clock (CP) to output (Q_7 or $\overline{Q}_7$) propagation delays, the clock pulse width and the maximum clock frequency.

Note to Figures 1 and 2

The changing to output assumes internal Q_6 opposite state from Q_7.

SV00591

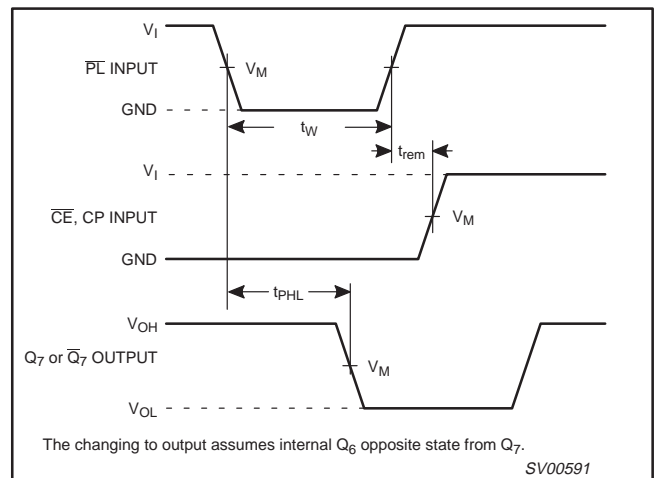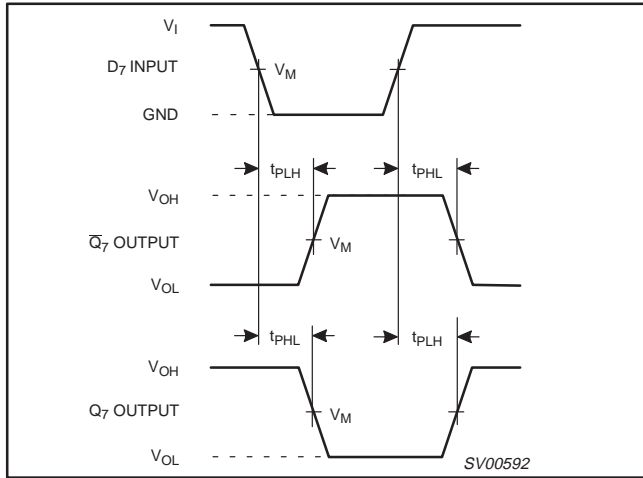**Figure 2. Parallel load ($\overline{PL}$) pulse width, the parallel load to output (Q_7 or $\overline{Q}_7$) propagation delays, the parallel load to clock (CP) and clock enable ($\overline{CE}$) removal time.**

8-bit parallel-in/serial-out shift register

AC WAVEFORMS

V_M = 1.5 V at $V_{CC} \geq$ 2.7 V.

V_M = 0.5 × V_{CC} at V_{CC} < 2.7 V;

V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.

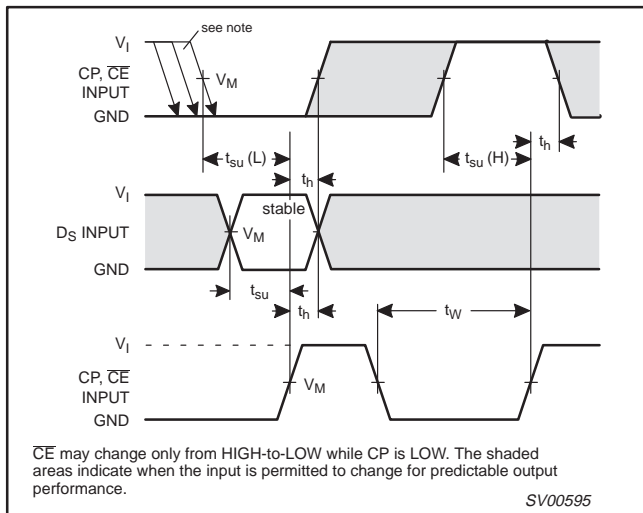**Figure 3. Data input (D_n) to output (Q_7 or $\overline{Q}_7$) propagation delays when $\overline{PL}$ is LOW.**

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.
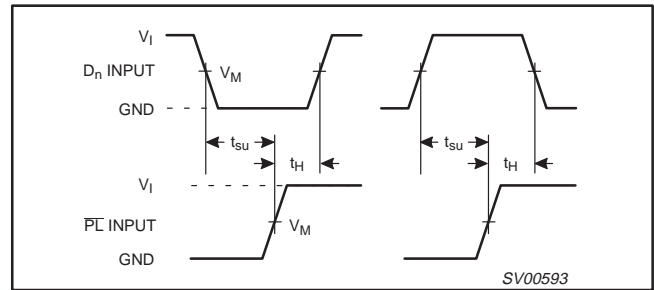
Figure 4. Set-up and hold times from the serial data input (D_S) to the clock (CP) and the clock enable ($\overline{CE}$) inputs, from the clock enable input ($\overline{CE}$) to the clock input (CP) and from the clock input (CP) to the clock enable input ($\overline{CE}$).

Note to Figure 4

$\overline{CE}$ may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Figure 5. Set-up and hold times from the data inputs (D_n) to the parallel load input ($\overline{PL}$).

TEST CIRCUIT

Test Circuit for Outputs

DEFINITIONS

R_L = Load resistor

C_L = Load capacitance includes jig and probe capacitiance

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

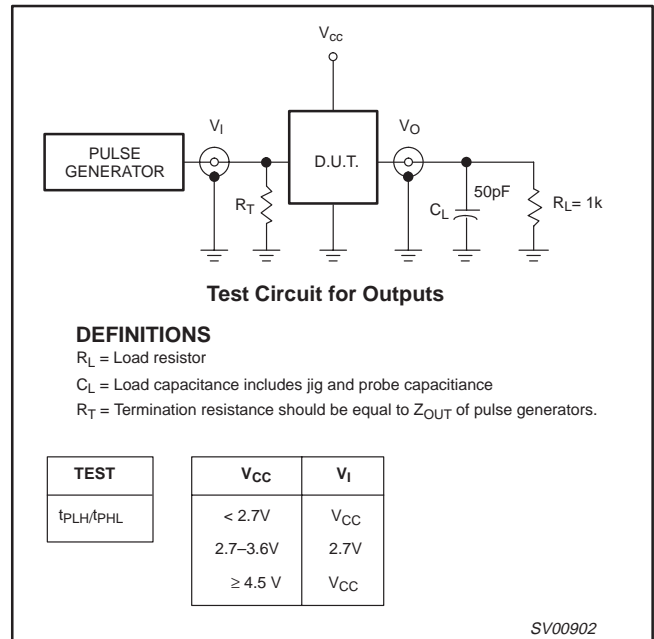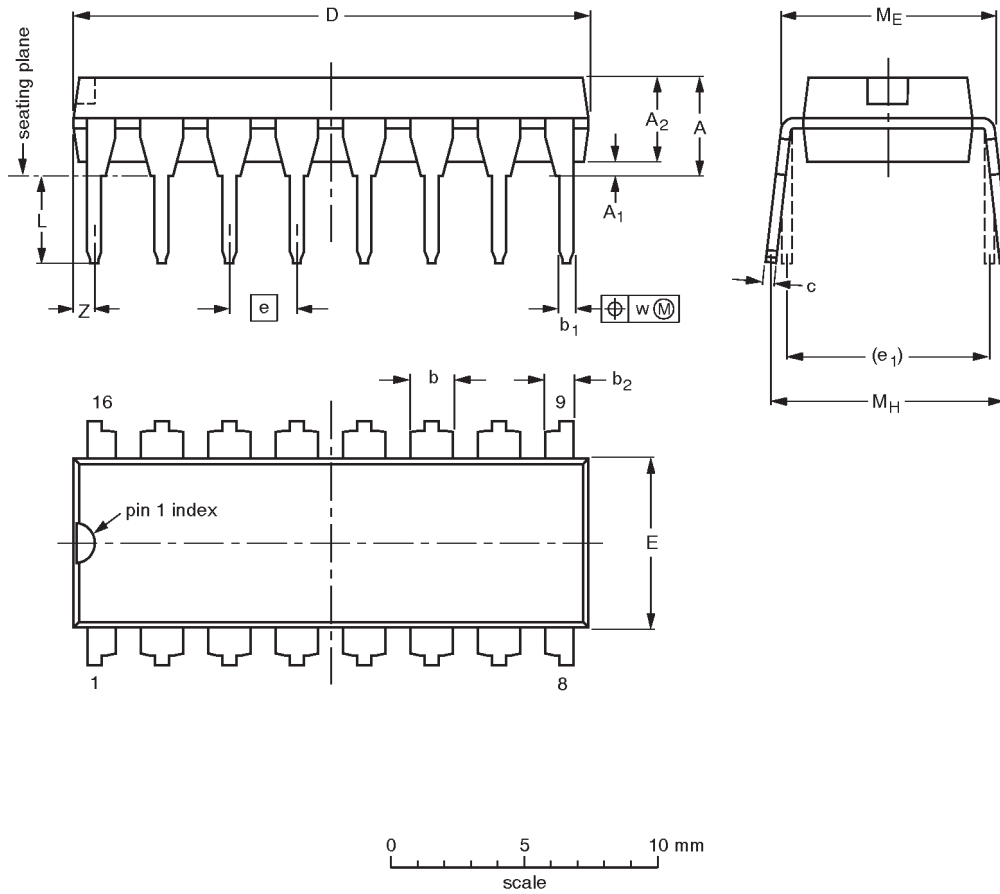| TEST	V_{CC}	V_I
t_{PLH}/t_{PHL}	< 2.7V	V_{CC}
	2.7–3.6V	2.7V
	≥ 4.5 V	V_{CC}

Figure 6. Load circuitry for switching times.

8-bit parallel-in/serial-out shift register

74LV165

DIP16:   plastic dual in-line package; 16 leads (300 mil)   **SOT38-4**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	$D^{(1)}$	$E^{(1)}$	e	e_1	L	M_E	M_H	w	$Z^{(1)}$ max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

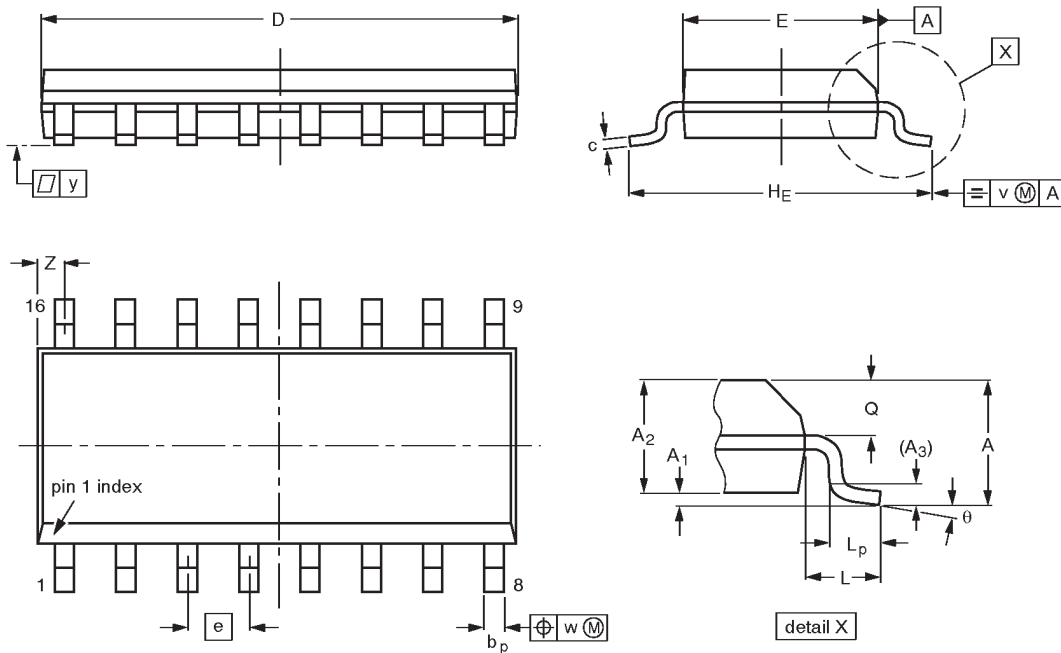1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

8-bit parallel-in/serial-out shift register

74LV165

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D[1]	E[1]	e	H_E	L	L_p	Q	v	w	y	Z[1]	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.0098 0.0039	0.057 0.049	0.01	0.019 0.014	0.0098 0.0075	0.39 0.38	0.16 0.15	0.050	0.24 0.23	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

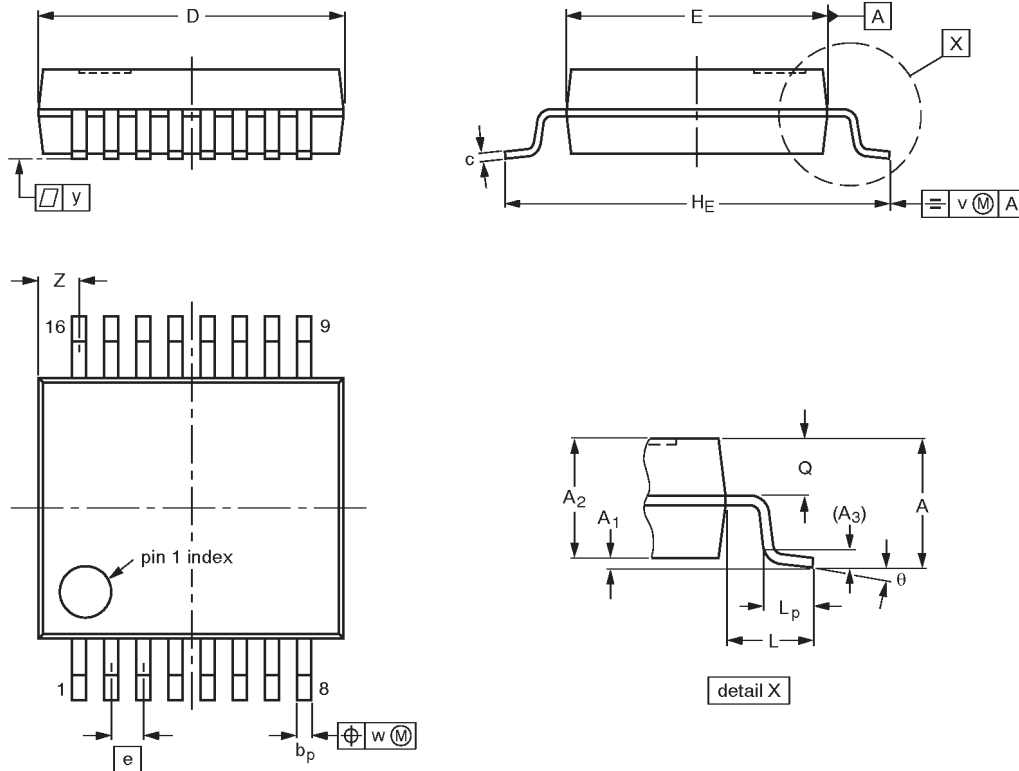1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~91-08-13~~ 95-01-23

8-bit parallel-in/serial-out shift register

74LV165

SSOP16:   plastic shrink small outline package; 16 leads; body width 5.3 mm

SOT338-1

pin 1 index

detail X

```
0        2.5        5 mm
|__|__|__|__|__|__|__|__|__|__|
           scale
```

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

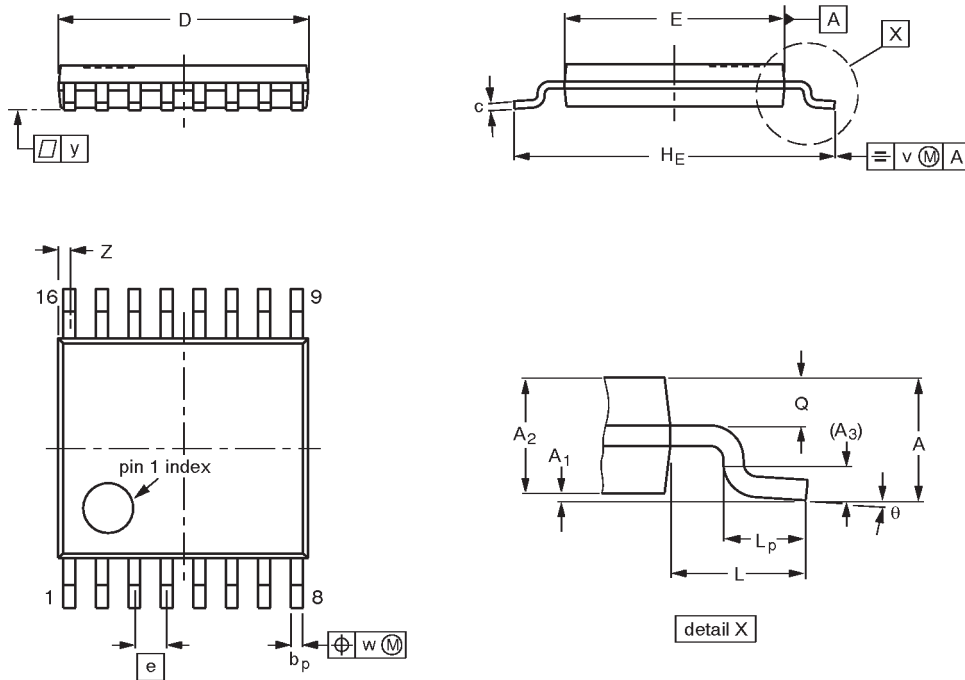1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				94-01-14 95-02-04

8-bit parallel-in/serial-out shift register

74LV165

TSSOP16:   plastic thin shrink small outline package; 16 leads; body width 4.4 mm   SOT403-1
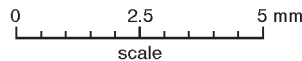
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D (1)	E (2)	e	H_E	L	Lₚ	Q	v	w	y	Z (1)	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT403-1		MO-153				~~94-07-12~~ 95-04-04

NOTES

DEFINITIONS

Data Sheet Identification	Product Status	Definition
Objective Specification	**Formative or in Design**	This data sheet contains the design target or goal specifications for product development. Specifications may change in any manner without notice.
Preliminary Specification	**Preproduction Product**	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product Specification	**Full Production**	This data sheet contains Final Specifications. Philips Semiconductors reserves the right to make changes at any time without notice, in order to improve design and supply the best possible product.

Philips Semiconductors and Philips Electronics North America Corporation reserve the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no license or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified. Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

LIFE SUPPORT APPLICATIONS
Philips Semiconductors and Philips Electronics North America Corporation Products are not designed for use in life support appliances, devices, or systems where malfunction of a Philips Semiconductors and Philips Electronics North America Corporation Product can reasonably be expected to result in a personal injury. Philips Semiconductors and Philips Electronics North America Corporation customers using or selling Philips Semiconductors and Philips Electronics North America Corporation Products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors and Philips Electronics North America Corporation for any damages resulting from such improper use or sale.

Let's make things better.

Philips
Semiconductors

PHILIPS

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for Buffers & Line Drivers *category:*

Click to view products by NXP *manufacturer:*

Other Similar products are found below :

5962-9217601MSA 634810D 875140G HEF4022BP HEF4043BP NL17SG125DFT2G NL17SZ126P5T5G NLU1GT126CMUTCG NLU3G16AMX1TCG NLV27WZ125USG MC74HCT365ADTR2G BCM6306KMLG 54FCT240CTDB Le87401NQC Le87402MQC 028192B 042140C 051117G 070519XB 065312DB 091056E 098456D NL17SG07DFT2G NL17SG17DFT2G NL17SG34DFT2G NL17SZ07P5T5G NL17SZ125P5T5G NLU1GT126AMUTCG NLV27WZ16DFT2G 5962-8982101PA 5962-9052201PA 74LVC07ADR2G MC74VHC1G125DFT1G NL17SH17P5T5G NL17SZ125CMUTCG NLV17SZ07DFT2G NLV37WZ17USG NLVHCT244ADTR2G NC7WZ17FHX 74HCT126T14-13 NL17SH125P5T5G NLV14049UBDTR2G NLV37WZ07USG 74VHC541FT(BE) RHFAC244K1 74LVC1G17FW4-7 74LVC1G126FZ4-7 BCM6302KMLG 74LVC1G07FZ4-7 74LVC1G125FW4-7