HG277/HG2277/HG4277
High Precision Operational Amplifiers

1 Features

- Ultralow Offset Voltage: 10 μV
- Ultralow Drift: ±0.1 μV/°C
- High Open-Loop Gain: 134 dB
- High Common-Mode Rejection: 140 dB
- High Power Supply Rejection: 130 dB
- Low Bias Current: 1-nA maximum
- Wide Supply Range: ±2 V to ±18 V
- Low Quiescent Current: 800 μA/amplifier
- Single, Dual, and Quad Versions

2 Applications

- Transducer Amplifiers
- Bridge Amplifiers
- Temperature Measurements
- Strain Gage Amplifiers
- Precision Integrators
- Battery-Powered Instruments
- Test Equipment

3 Description

The HGx277 series precision operational amplifiers replace the industry standard HG-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications, for maximum design flexibility.

HGx277 series operational amplifiers operate from ±2-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers which are specified at only one supply voltage, the HGx277 series is specified for real-world applications; a single limit applies over the ±5-V to ±15-V supply range. High performance is maintained as the amplifiers swing to their specified limits. Because the initial offset voltage (±20 μV maximum) is so low, user adjustment is usually not required. However, the single version (HG277) provides external trim pins for special applications.

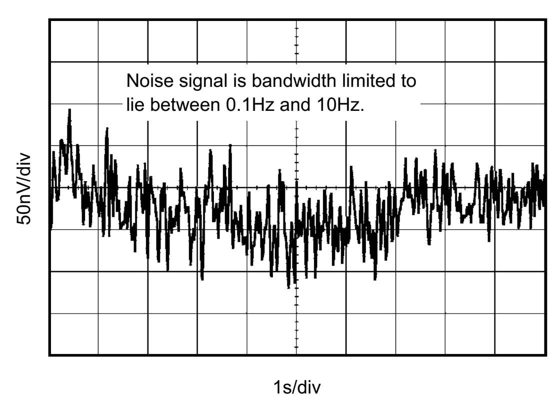
HG277 operational amplifiers are easy to use and free from phase inversion and the overload problems found in some other operational amplifiers. They are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
HG277 HG2277	VSON (8)	4.00 mm × 4.00 mm
	SOIC (8)	3.91 mm × 4.90 mm
	PDIP (8)	6.35 mm × 9.81 mm
HG4277	SOIC (14)	3.91 mm × 8.65 mm
	PDIP (14)	6.35 mm × 19.30 mm

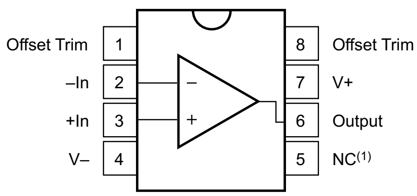
(1) For all available packages, see the orderable addendum at the end of the data sheet.

0.1 Hz to 10 Hz Noise

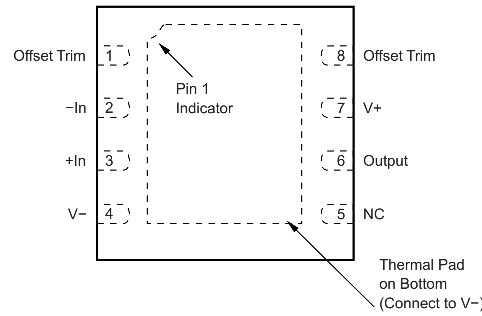


4 Pin Configuration and Functions

HG277 P and D Packages
8-Pin PDIP and SOIC
Top View



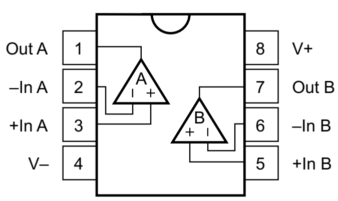
HG277 DRM Package
8-Pin VSON
Top View



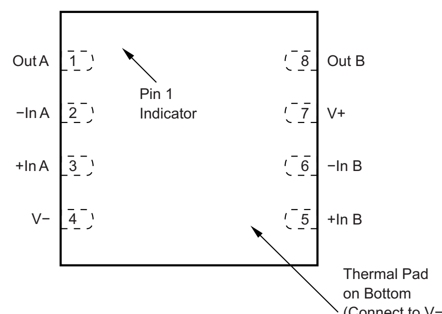
Pin Functions: HG277

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Offset Trim	I	Input offset voltage trim (leave floating if not used)
2	–In	I	Inverting input
3	+In	I	Noninverting input
4	V–	—	Negative (lowest) power supply
5	NC	—	No internal connection (can be left floating)
6	Output	O	Output
7	V+	—	Positive (highest) power supply
8	Offset Trim	—	Input offset voltage trim (leave floating if not used)

HG2277 P and D Packages
8-Pin PDIP and SOIC
Top View



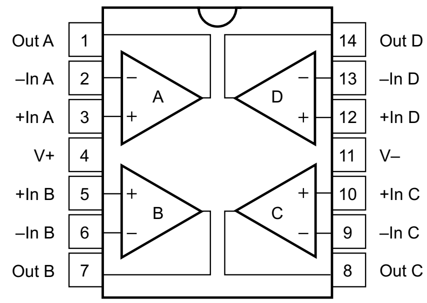
HG2277 DRM Package
8-Pin VSON
Top View



Pin Functions: HG2277

PIN			I/O	DESCRIPTION
NAME	PDIP, SOIC NO.	DFN NO.		
Out A	1	1	O	Output channel A
–In A	2	2	I	Inverting input channel A
+In A	3	3	I	Noninverting input channel A
V–	4	4	—	Negative (lowest) power supply
+In B	5	5	I	Noninverting input channel B
–In B	6	6	I	Inverting input channel B
Out B	7	8	O	Output channel B
V+	8	7	—	Positive (highest) power supply

HG4277 P and D Packages
14 Pins PDIP and SOIC
Top View



Pin Functions: HG4277

PIN		I/O	DESCRIPTION
NO.	NAME		
1	Out A	O	Output channel A
2	–In A	I	Inverting input channel A
3	+In A	I	Noninverting input channel A
4	V+	—	Positive (highest) power supply
5	+In B	I	Noninverting input channel B
6	–In B	I	Inverting input channel B
7	Out B	O	Output channel B
8	Out C	O	Output channel C
9	–In C	I	Inverting input channel C
10	+In C	I	Noninverting input channel C
11	V–	—	Negative (lowest) power supply
12	+In D	I	Noninverting input channel D
13	–In D	I	Inverting input channel D
14	Out D	O	Output channel D

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)		36	V
Input voltage	(V–) –0.7	(V+) +0.7	V
Output short-circuit (2)	Continuous		
Operating temperature	–55	125	°C
Junction temperature		150	°C
Lead temperature		300	°C
Storage temperature, T_{stg}	–55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Short-circuit to ground, one amplifier per package.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage, Vs = (V+) – (V–)	4 (±2)	30 (±15)	36 (±18)	V
Specified temperature	–40		+85	°C

5.4 Thermal Information for HG277

THERMAL METRIC (1)		HG277			UNIT
		P (PDIP)	D (SOIC)	DRM (VSON)	
		8 PINS			
$R_{θJA}$	Junction-to-ambient thermal resistance	49.2	110.1	40.7	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	39.4	52.2	41.3	°C/W
$R_{θJB}$	Junction-to-board thermal resistance	26.4	52.3	16.7	°C/W
$ψ_{JT}$	Junction-to-top characterization parameter	15.4	10.4	0.6	°C/W
$ψ_{JB}$	Junction-to-board characterization parameter	26.3	51.5	16.9	°C/W
$R_{θJC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	3.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Thermal Information for HG2277

THERMAL METRIC (1)		HG2277			UNIT
		P (PDIP)	D (SOIC)	DRM (VSON)	
		8 PINS			
$R_{θJA}$	Junction-to-ambient thermal resistance	47.2	107.4	39.3	°C/W
$R_{θJC(top)}$	Junction-to-case (top) thermal resistance	36.0	45.8	36.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Thermal Information for HG2277 (continued)

THERMAL METRIC(1)		HG2277 P (PDIP) 8 PINS	HG2277 D (SOIC) 8 PINS	HG2277 DRM (VSON) 8 PINS	UNIT
$R_{\theta JB}$	Junction-to-board thermal resistance	24.4	47.9	15.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	13.4	5.7	0.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	24.3	47.3	15.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	2.2	°C/W

5.6 Thermal Information for HG4277

THERMAL METRIC(1)		HG4277 D (SOIC) 14 PINS	HG4277 P (PDIP) 14 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	67.0	66.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	24.1	20.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.5	26.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	2.2	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	22.1	26.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Electrical Characteristics for HGx277P, HGx277U, and HGx277xA

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	HG277P, U HG2277P, U MIN	HG277P, U HG2277P, U TYP(1)	HG277P, U HG2277P, U MAX	HG277xA HG2277xA HG4277xA MIN	HG277xA HG2277xA HG4277xA TYP(1)	HG277xA HG2277xA HG4277xA MAX	UNIT
OFFSET VOLTAGE										
V_{OS}	Input Offset Voltage				±10	±20		±20	±50	μV
	Input Offset Voltage Over Temperature	HG277P, U (high-grade, single)	T_A = –40°C to 85°C			±30				μV
		HG2277P, U (high-grade, dual)				±50				
		All PA, UA, Versions							±100	
		AIDRM Versions								
dV_{OS}/dT	Input Offset Voltage Drift	HG277P, U (high-grade, single)	T_A = –40°C to 85°C		±0.1	±0.15				μV/°C
		HG2277P, U (high-grade, dual)			±0.1	±0.25				
		All PA, UA, AIDRM Versions						±0.15	±1	
	Input Offset Voltage: (all models)	vs Time			0.2			See (2)		μV/mo
		vs Power Supply (PSRR)	V_S = ±2 V to ±18 V		±0.3	±0.5		See (2)	±1	μV/V
			T_A = –40°C to 85°C			±0.5			±1	
	Channel Separation (dual, quad)		DC		0.1			See (2)		μV/V

(1) V_S = ±15 V
(2) Specifications are the same as HG277P, U.

Electrical Characteristics for HGx277P, HGx277U, and HGx277xA (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	HG277P, U HG2277P, U			HG277xA HG2277xA HG4277xA			UNIT
				MIN	TYP [1]	MAX	MIN	TYP [1]	MAX	
INPUT BIAS CURRENT										
I_B	Input Bias Current		T_A = –40°C to 85°C		±0.5	±1		See [2]	±2.8	nA
						±2			±4	
I_{OS}	Input Offset Current		T_A = –40°C to 85°C		±0.5	±1		See [2]	±2.8	nA
						±2			±4	
NOISE										
	Input Voltage Noise, f = 0.1 to 10 Hz				0.22			See [2]		μV_{PP}
e_n	Input Voltage Noise Density	f = 10 Hz			12			See [2]		nV/√Hz
		f = 100 Hz			8			See [2]		
		f = 1 kHz			8			See [2]		
		f = 10 kHz			8			See [2]		
i_n	Current Noise Density, f = 1 kHz				0.2			See [2]		pA/√Hz
INPUT VOLTAGE RANGE										
V_{CM}	Common-Mode Voltage Range			(V–)+2		(V+)–2	See [2]		See [2]	V
CMRR	Common-Mode Rejection		V_{CM} = (V–) +2 V to (V+) –2 V	130	140		115	See [2]		dB
			T_A = –40°C to 85°C	128			115			
INPUT IMPEDANCE										
	Differential				100 || 3			See [2]		MΩ || pF
	Common-Mode		V_{CM} = (V–) +2 V to (V+) –2 V		250 || 3			See [2]		GΩ || pF
OPEN-LOOP GAIN										
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+0.5 V to (V+)–1.2 V, R_L = 10 kΩ		140			See [2]		dB
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	126	134		See [2]	See [2]		
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ; T_A = –40°C to 85°C	126			See [2]			dB
FREQUENCY RESPONSE										
GBW	Gain-Bandwidth Product				1			See [2]		MHz
SR	Slew Rate				0.8			See [2]		V/µs
	Settling Time	0.1%	V_S = ±15 V, G = 1, 10-V Step		14			See [2]		µs
		0.01%			16			See [2]		
	Overload Recovery Time		V_{IN} × G = V_S		3			See [2]		µs
THD+N	Total Harmonic Distortion + Noise		1 kHz, G = 1, V_O = 3.5 Vrms		0.002%			See [2]		

Electrical Characteristics for HGx277P, HGx277U, and HGx277xA (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	HG277P, U HG2277P, U			HG277xA HG2277xA HG4277xA			UNIT
			MIN	TYP [1]	MAX	MIN	TYP [1]	MAX	
OUTPUT									
V_O	Voltage Output	R_L = 10 kΩ	(V–)+0.5		(V+)–1.2	See [2]		See [2]	V
		T_A = –40°C to +85°C	(V–)+0.5		(V+)–1.2	See [2]		See [2]	
		R_L = 2 kΩ	(V–)+1.5		(V+)–1.5	See [2]		See [2]	
		T_A = –40°C to +85°C	(V–)+1.5		(V+)–1.5	See [2]		See [2]	
I_{SC}	Short-Circuit Current			±35			See [2]		mA
C_{LOAD}	Capacitive Load Drive			See [3]					
Z_O	Open-loop output impedance	f = 1 MHz		40			See [2]		Ω
POWER SUPPLY									
V_S	Specified Voltage Range		±5		±15	See [2]		See [2]	V
	Operating Voltage Range		±2		±18	See [2]		See [2]	V
I_Q	Quiescent Current (per amplifier)	I_O = 0		±790	±825		See [2]	See [2]	µA
		T_A = –40°C to 85°C			±900			See [2]	
TEMPERATURE RANGE									
	Specified Range		–40		85	See [2]		See [2]	°C
	Operating Range		–55		125	See [2]		See [2]	°C

(3) See *Typical Characteristics*

6.8 Electrical Characteristics for HGx277AIDRM

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	HG277AIDRM HG2277AIDRM			UNIT
				MIN	TYP [1]	MAX	
OFFSET VOLTAGE							
V_{0S}	Input Offset Voltage				±35	±100	µV
	Input Offset Voltage Over Temperature	HG277P, U (high-grade, single)	T_A = –40°C to 85°C				µV
		HG2277P, U (high-grade, dual)					
		All PA, UA, Versions					
		AIDRM Versions				±165	
dV_{0S}/dT	Input Offset Voltage Drift	HG277P, U (high-grade, single)	T_A = –40°C to 85°C				µV/°C
		HG2277P, U (high-grade, dual)					
		All PA, UA, AIDRM Versions			±0.15	±1	
	Input Offset Voltage: (all models)	vs Time			See [2]		µV/mo
		vs Power Supply (PSRR)	V_S = ±2 V to ±18 V		See [2]	±1	µV/V
			T_A = –40°C to 85°C			±1	
	Channel Separation (dual, quad)		DC		See [2]		µV/V

(1) V_S = ±15 V
(2) Specifications are the same as HG277P, U.

Electrical Characteristics for HGx277AIDRM (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER			TEST CONDITIONS	HG277AIDRM HG2277AIDRM			UNIT
				MIN	TYP [1]	MAX	
INPUT BIAS CURRENT							
I_B	Input Bias Current		T_A = –40°C to 85°C			±2.8	nA
						±4	
I_{OS}	Input Offset Current		T_A = –40°C to 85°C			±2.8	nA
						±4	
NOISE							
	Input Voltage Noise, f = 0.1 to 10 Hz				See [2]		μV_{PP}
e_n	Input Voltage Noise Density	f = 10 Hz			See [2]		nV/√Hz
		f = 100 Hz			See [2]		
		f = 1 kHz			See [2]		
		f = 10 kHz			See [2]		
i_n	Current Noise Density, f = 1 kHz				See [2]		pA/√Hz
INPUT VOLTAGE RANGE							
V_{CM}	Common-Mode Voltage Range			See [2]		See [2]	V
CMRR	Common-Mode Rejection		V_{CM} = (V–) +2 V to (V+) –2 V	115	See [2]		dB
			T_A = –40°C to 85°C	115			
INPUT IMPEDANCE							
	Differential				See [2]		MΩ || pF
	Common-Mode		V_{CM} = (V–) +2 V to (V+) –2 V		See [2]		GΩ || pF
OPEN-LOOP GAIN							
A_{OL}	Open-Loop Voltage Gain		V_O = (V–)+0.5 V to (V+)–1.2 V, R_L = 10 kΩ		See [2]		dB
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	See [2]	See [2]		
			V_O = (V–)+1.5 V to (V+)–1.5 V, R_L = 2 kΩ	See [2]			dB
			T_A = –40°C to 85°C				
FREQUENCY RESPONSE							
GBW	Gain-Bandwidth Product				See [2]		MHz
SR	Slew Rate				See [2]		V/μs
	Settling Time	0.1%	V_S = ±15 V, G = 1, 10-V Step		See [2]		μs
		0.01%			See [2]		
	Overload Recovery Time		V_{IN} × G = V_S		See [2]		μs
THD+N	Total Harmonic Distortion + Noise		1 kHz, G = 1, V_O = 3.5 Vrms		See [2]		
OUTPUT							
V_O	Voltage Output		R_L = 10 kΩ	See [2]		See [2]	V
			T_A = –40°C to +85°C	See [2]		See [2]	
			R_L = 2 kΩ	See [2]		See [2]	
			T_A = –40°C to +85°C	See [2]		See [2]	
I_{SC}	Short-Circuit Current				See [2]		mA
C_{LOAD}	Capacitive Load Drive						
Z_O	Open-loop output impedance		f = 1 MHz		See [2]		Ω

Electrical Characteristics for HGx277AIDRM (continued)

At T_A = 25°C, and R_L = 2 kΩ, unless otherwise noted

PARAMETER		TEST CONDITIONS	HG277AIDRM HG2277AIDRM			UNIT
			MIN	TYP(1)	MAX	
POWER SUPPLY						
V_S	Specified Voltage Range		See (2)		See (2)	V
	Operating Voltage Range		See (2)		See (2)	V
I_Q	Quiescent Current (per amplifier)	I_O = 0		See (2)	See (2)	µA
		T_A = –40°C to 85°C			See (2)	
TEMPERATURE RANGE						
	Specified Range		See (2)		See (2)	°C
	Operating Range		See (2)		See (2)	°C

6.9 Typical Characteristics

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

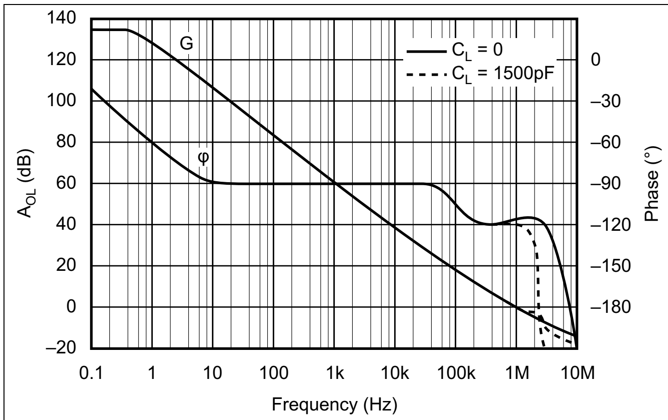


Figure 1. Open-Loop Gain and Phase vs Frequency

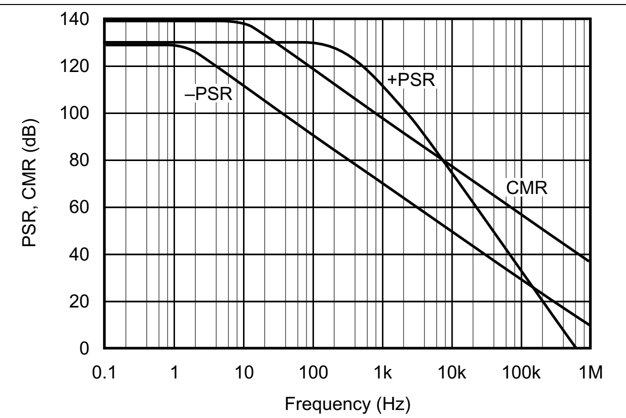


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

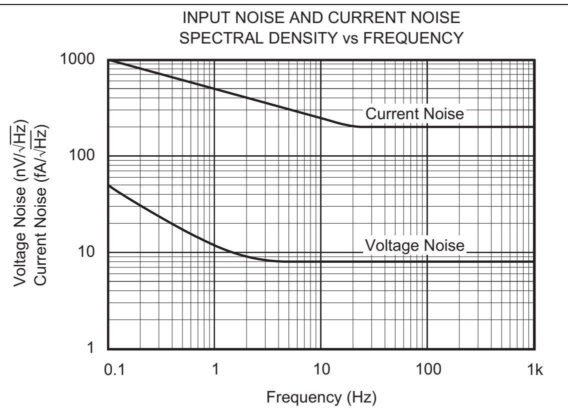


Figure 3. Input Noise and Current Noise Spectral Density vs Frequency

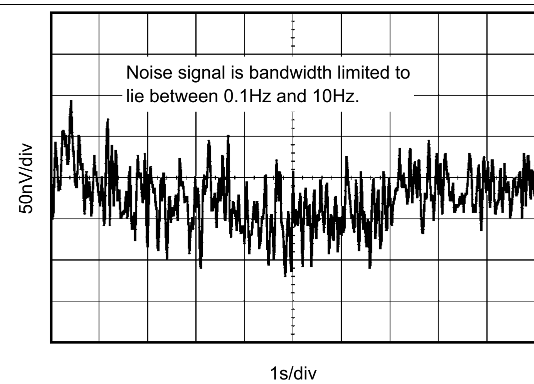


Figure 4. Input Noise Voltage vs Time

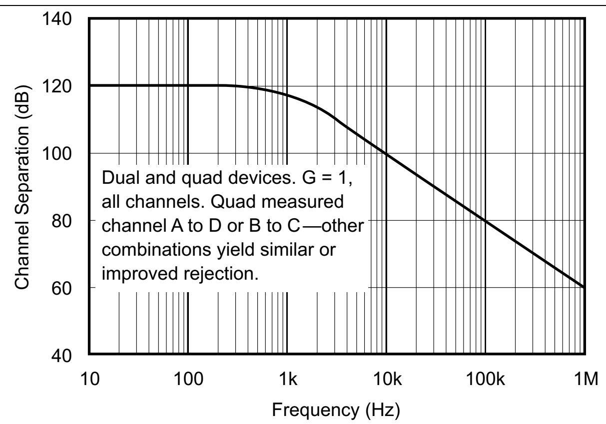


Figure 5. Channel Separation vs Frequency

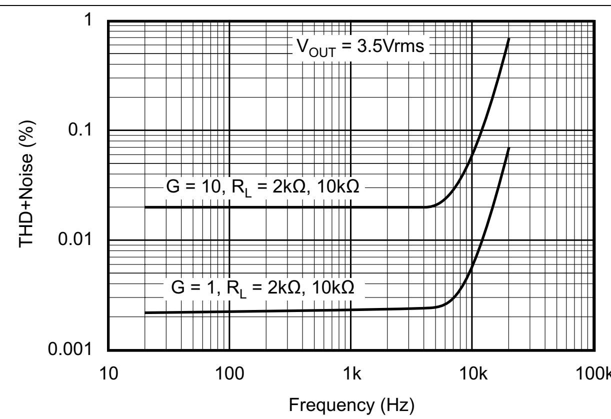


Figure 6. Total Harmonic Distortion + Noise vs Frequency

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

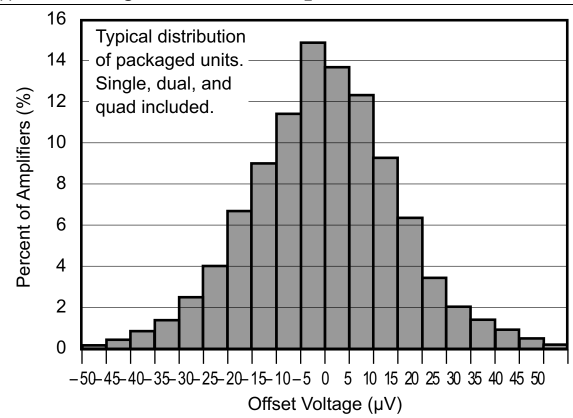


Figure 7. Offset Voltage Production Distribution

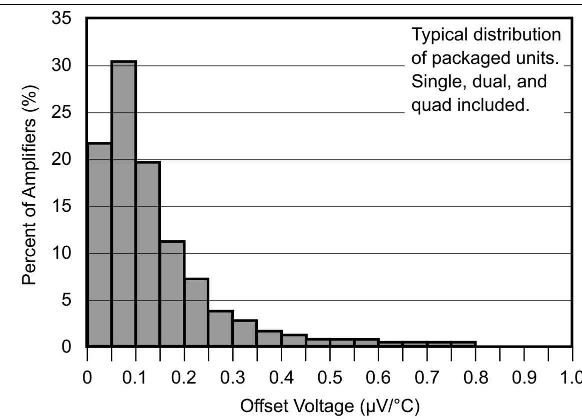


Figure 8. Offset Voltage Drift Production Distribution

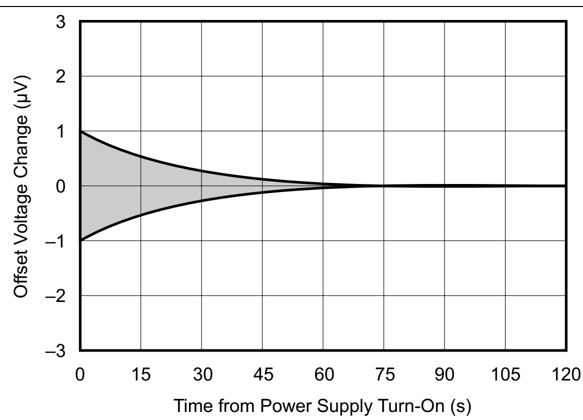


Figure 9. Warm-Up Offset Voltage Drift

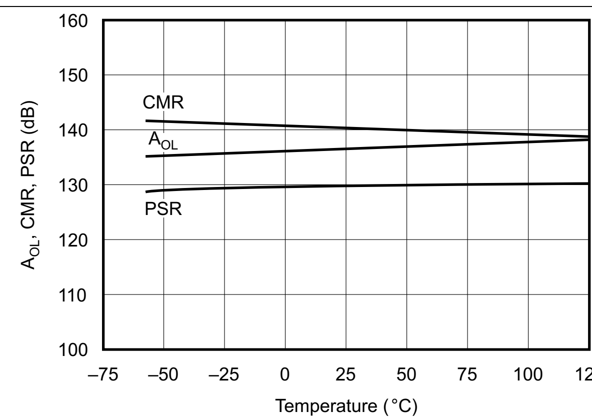


Figure 10. A_{OL}, CMR, PSR vs Temperature

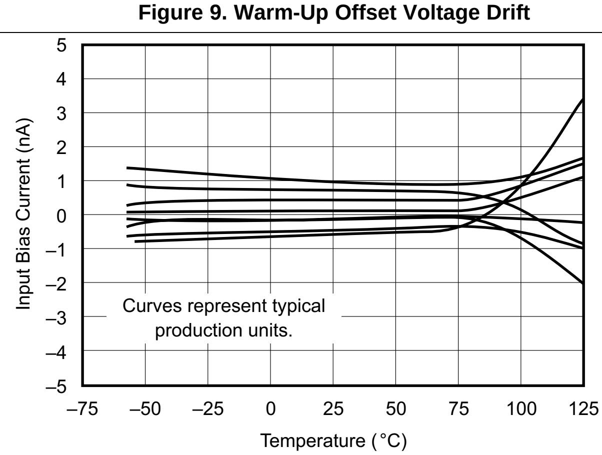


Figure 11. Input Bias Current vs Temperature

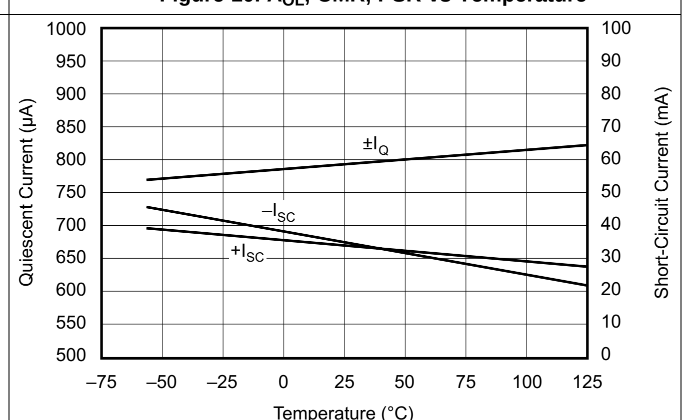


Figure 12. Quiescent Current and Short-Circuit Current vs Temperature

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

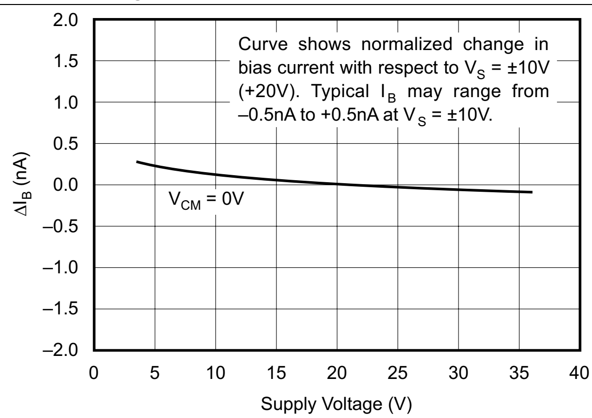


Figure 13. Change in Input Bias Current vs Power Supply Voltage

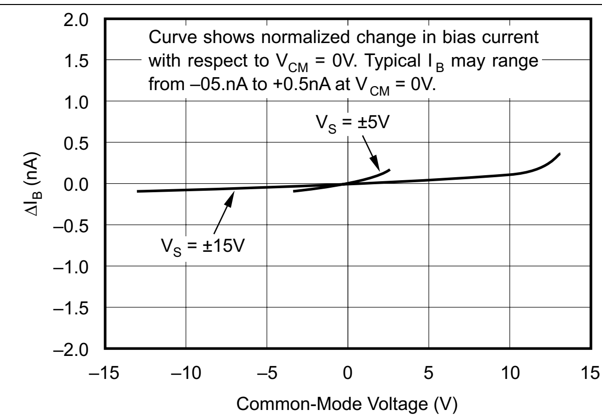


Figure 14. Change in Input Bias Current vs Common-Mode Voltage

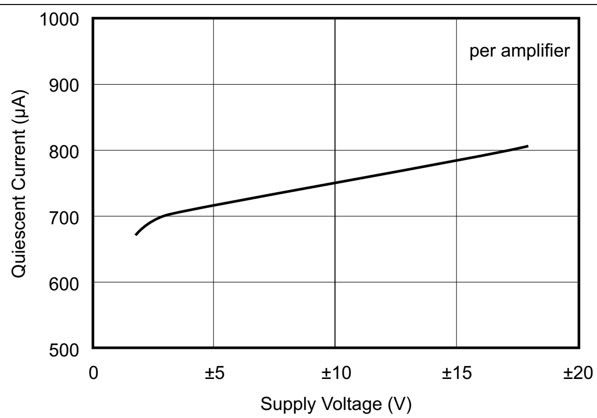


Figure 15. Quiescent Current vs Supply Voltage

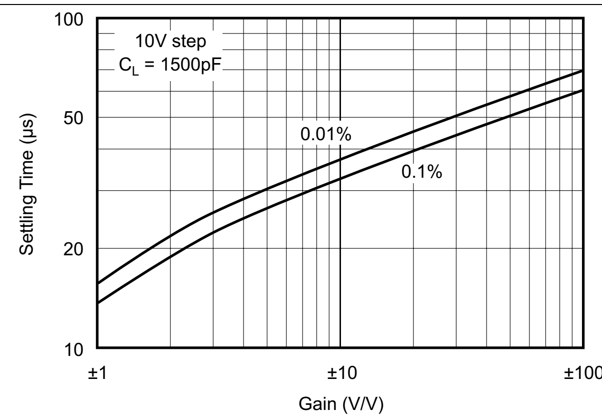


Figure 16. Settling Time vs Closed-Loop Gain

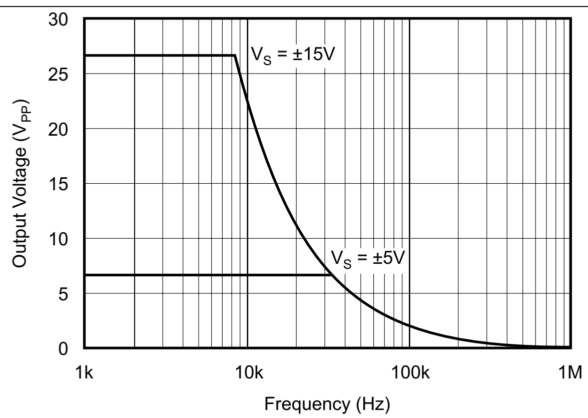


Figure 17. Maximum Output Voltage vs Frequency

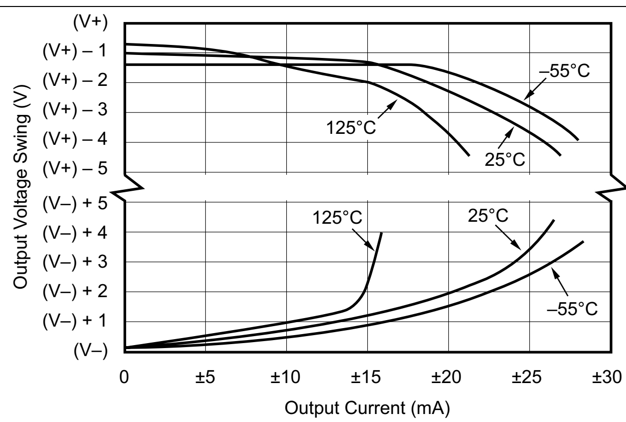


Figure 18. Output Voltage Swing vs Output Current

Typical Characteristics (continued)

At T_A = 25°C, V_S = ±15 V, and R_L = 2 kΩ, unless otherwise noted.

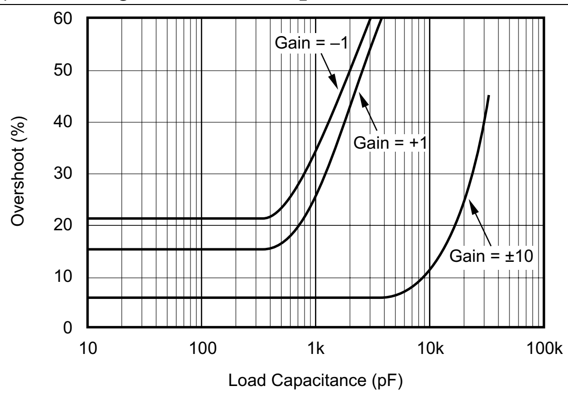


Figure 19. Small-Signal Overshoot vs Load Capacitance

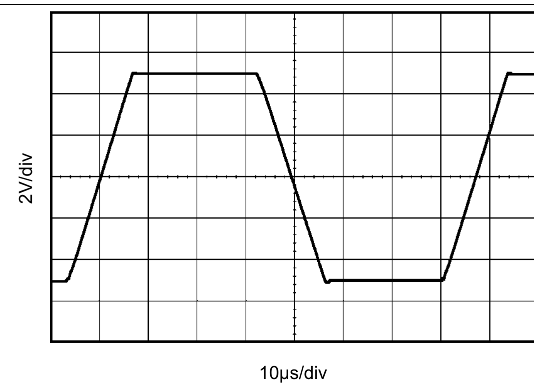


Figure 20. Large-Signal Step Response
G = 1, C_L = 1500 pF, V_S = ±15 V

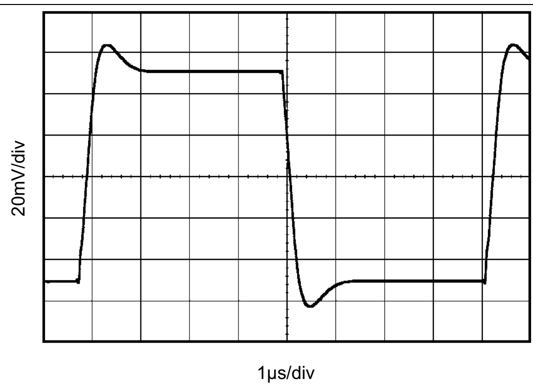


Figure 21. Small-Signal Step Response
G= +1, C_L = 0, V_S = ±15 V

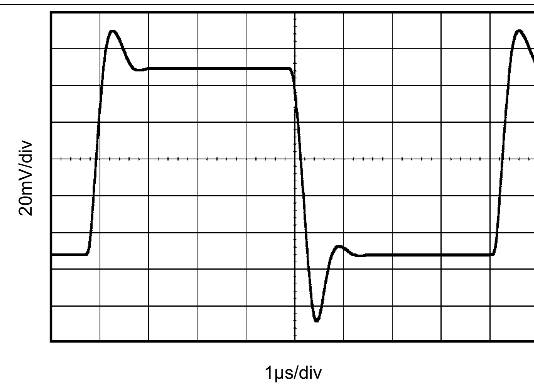


Figure 22. Small-Signal Step Response
G= 1, C_L = 1500 pF, V_S = ±15 V

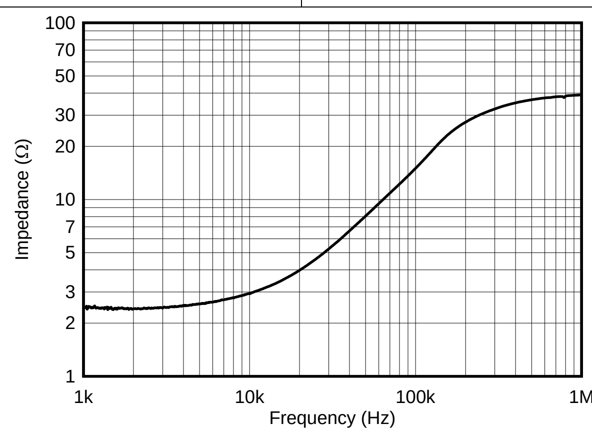


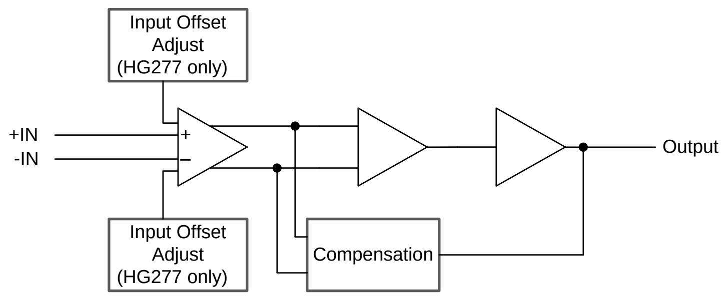
Figure 23. Open-Loop Output Impedance
V_S = ±15 V

7 Detailed Description

7.1 Overview

The HGx277 series precision operational amplifiers replace the industry standard HG-177. They offer improved noise, wider output voltage swing, and are twice as fast with half the quiescent current. Features include ultralow offset voltage and drift, low bias current, high common-mode rejection, and high power supply rejection. Single, dual, and quad versions have identical specifications, for maximum design flexibility.

7.2 Functional Block Diagram



7.3 Feature Description

The HGx277 series is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high-impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1-μF capacitors are adequate.

The HGx277 series has low offset voltage and drift. To achieve highest performance, the circuit layout and mechanical conditions should be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the operational amplifier inputs. Connections of dissimilar metals generate thermal potential, which can degrade the ultimate performance of the HGx277 series. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep the thermal mass of the connections to the two input terminals similar
- Locate heat sources as far as possible from the critical input circuitry
- Shield operational amplifier and input circuitry from air currents, such as cooling fans

7.3.1 Operating Voltage

HGx277 series operational amplifiers operate from ±2-V to ±18-V supplies with excellent performance. Unlike most operational amplifiers, which are specified at only one supply voltage, the HG277 series is specified for real-world applications; a single limit applies over the ±5-V to ±15-V supply range. This allows a customer operating at V_S = ±10 V to have the same assured performance as a customer using ±15-V supplies. In addition, key parameters are assured over the specified temperature range, –40°C to 85°C. Most behavior remains unchanged through the full operating voltage range (±2 V to ±18 V). Parameters which vary significantly with operating voltage or temperature are shown in *Typical Characteristics*.

7.3.2 Offset Voltage Adjustment

The HGx277 series is laser-trimmed for low offset voltage and drift, so most circuits do not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer, as shown in Figure 24. Only use this adjustment to null the offset of the operational amplifier. This adjustment should not be used to compensate for offsets created elsewhere in a system, because this can introduce additional temperature drift.

Feature Description (continued)

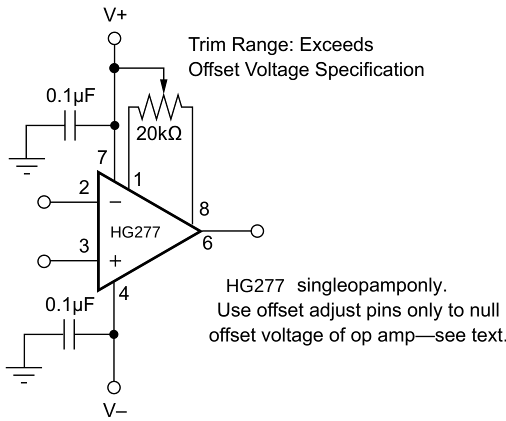


Figure 24. HG277 Offset Voltage Trim Circuit

7.3.3 Input Protection

The inputs of the HGx277 series are protected with 1-kΩ series input resistors and diode clamps. The inputs can withstand ±30-V differential inputs without damage. The protection diodes conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the operational amplifier.

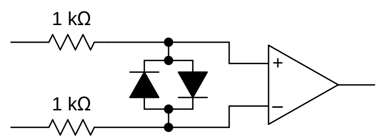


Figure 25. HGx277 Input Protection

7.3.4 Input Bias Current Cancellation

The input stage base current of the HGx277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor, as is often done with other operational amplifiers (see Figure 26). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

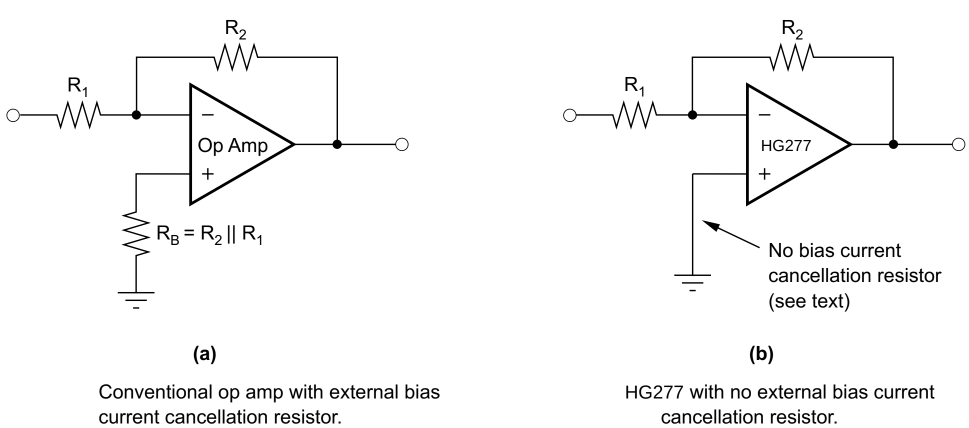


Figure 26. Input Bias Current Cancellation

Feature Description (continued)

7.3.5 EMI Rejection Ratio (EMIRR)

The electromagnetic interference (EMI) rejection ratio, or EMIRR, describes the EMI immunity of operational amplifiers. An adverse effect that is common to many operational amplifiers is a change in the offset voltage as a result of RF signal rectification. An operational amplifier that is more efficient at rejecting this change in offset as a result of EMI has a higher EMIRR and is quantified by a decibel value. Measuring EMIRR can be performed in many ways, but this report provides the EMIRR IN+, which specifically describes the EMIRR performance when the RF signal is applied to the noninverting input pin of the operational amplifier. In general, only the noninverting input is tested for EMIRR for the following three reasons:

1. Operational amplifier input pins are known to be the most sensitive to EMI, and typically rectify RF signals better than the supply or output pins.
2. The noninverting and inverting operational amplifier inputs have symmetrical physical layouts and exhibit nearly matching EMIRR performance.
3. EMIRR is easier to measure on noninverting pins than on other pins because the noninverting input terminal can be isolated on a printed circuit board (PCB). This isolation allows the RF signal to be applied directly to the noninverting input terminal with no complex interactions from other components or connecting PCB traces.

A more formal discussion of the EMIRR IN+ definition and test method is provided in application report SBOA128, *EMI Rejection Ratio of Operational Amplifiers*, available for download at www.ti.com. The EMIRR IN+ of the OPA277 is plotted versus frequency as shown in Figure 27.

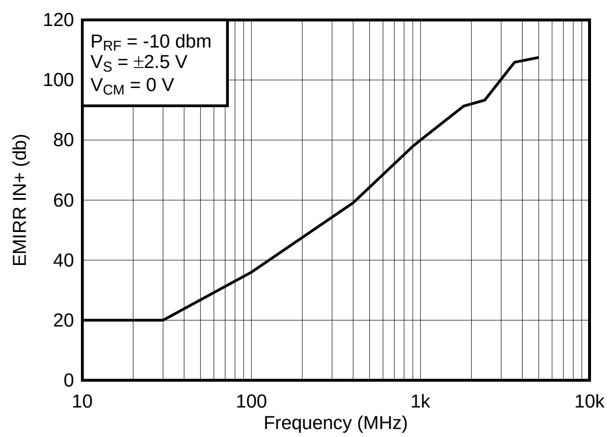


Figure 27. HG277 EMIRR IN+ vs Frequency

If available, any dual and quad operational amplifier device versions have nearly similar EMIRR IN+ performance. The HG277 unity-gain bandwidth is 1 MHz. EMIRR performance below this frequency denotes interfering signals that fall within the operational amplifier bandwidth.

Feature Description (continued)

Table 1 shows the EMIRR IN+ values for the HG277 at particular frequencies commonly encountered in real-world applications. Applications listed in Table 1 may be centered on or operated near the particular frequency shown. This information may be of special interest to designers working with these types of applications, or working in other fields likely to encounter RF interference from broad sources, such as the industrial, scientific, and medical (ISM) radio band.

Table 1. HG277 EMIRR IN+ for Frequencies of Interest

FREQUENCY	APPLICATION/ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite/space operation, weather, radar, UHF	59.1 dB
900 MHz	GSM, radio com/nav./GPS (to 1.6 GHz), ISM, aeronautical mobile, UHF	77.9 dB
1.8 GHz	GSM, mobile personal comm. broadband, satellite, L-band	91.3 dB
2.4 GHz	802.11b/g/n, Bluetooth™, mobile personal comm., ISM, amateur radio/satellite, S-band	93.3 dB
3.6 GHz	Radiolocation, aero comm./nav., satellite, mobile, S-band	105.9 dB
5.0 GHz	802.11a/n, aero comm./nav., mobile comm., space/satellite operation, C-band	107.5 dB

7.3.5.1 EMIRR IN+ Test Configuration

Figure 28 shows the circuit configuration for testing the EMIRR IN+. An RF source is connected to the operational amplifier noninverting input terminal using a transmission line. The operational amplifier is configured in a unity gain buffer topology with the output connected to a low-pass filter (LPF) and a digital multimeter (DMM). Note that a large impedance mismatch at the operational amplifier input causes a voltage reflection; however, this effect is characterized and accounted for when determining the EMIRR IN+. The resulting dc offset voltage is sampled and measured by the multimeter. The LPF isolates the multimeter from residual RF signals that may interfere with multimeter accuracy. Refer to SBOA128 for more details.

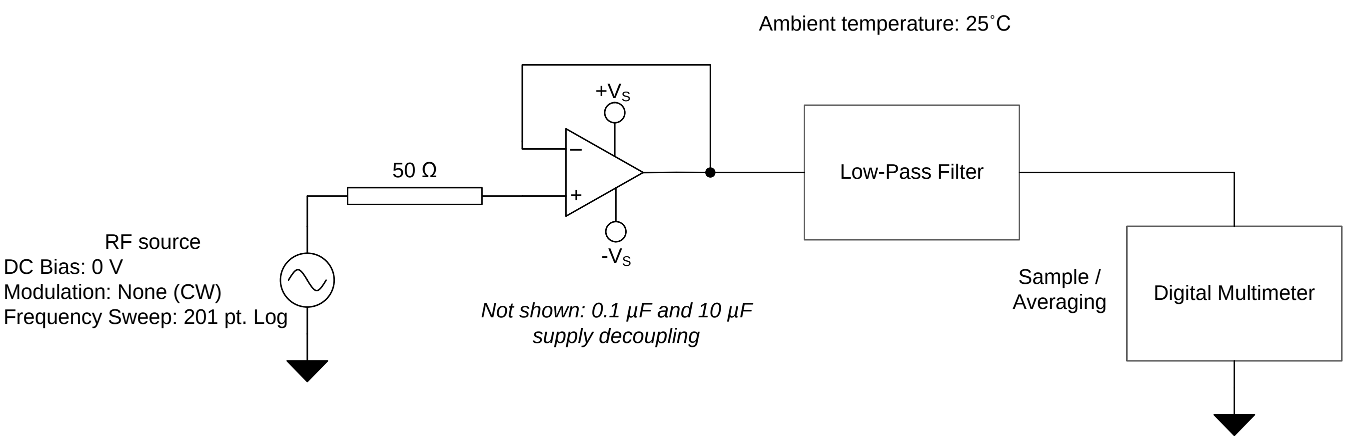


Figure 28. EMIRR IN+ Test Configuration Schematic

7.4 Device Functional Modes

The HGx277 has a single functional mode and is operational when the power-supply voltage is greater than 4 V (±2 V). The maximum power supply voltage for the HGx277 is 36 V (±18 V).

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The HGx277 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer ultralow offset voltage and offset voltage drift, as well as 1-MHz bandwidth and high capacitive load drive. These features make the HGx277 a robust, high-performance operational amplifier for high-voltage industrial applications.

8.2 Typical Applications

8.2.1 Second-Order Lowpass Filter

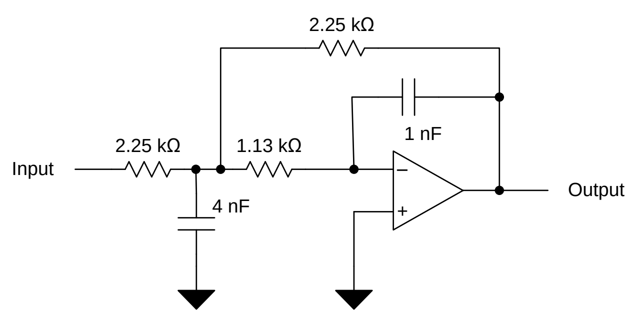


Figure 29. Second-Order Lowpass Filter

8.2.1.1 Design Requirements

- Gain = 1 V/V
- Lowpass cutoff frequency = 50 kHz
- –40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

8.2.1.2 Detailed Design Procedure

WEBENCH® Filter Designer is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, WEBENCH® Filter Designer allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

Typical Applications (continued)

8.2.1.3 Application Curve

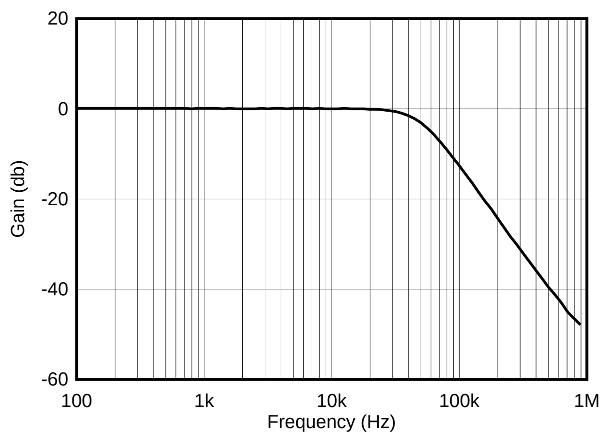
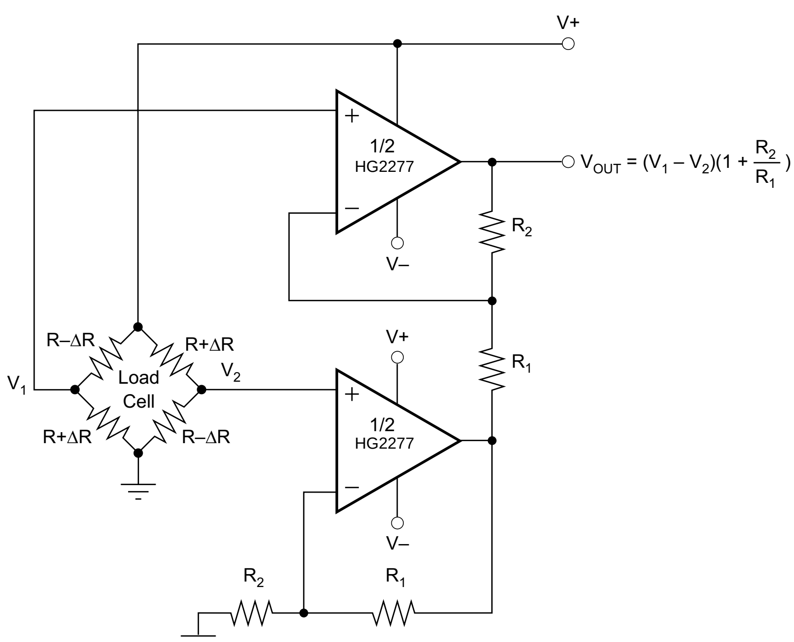


Figure 30. HG277 Second-Order 50-kHz, Lowpass Filter

8.2.2 Load Cell Amplifier



For integrated solution see: INA126, INA2126 (dual)
INA125 (on-board reference)
INA122 (single-supply)

Figure 31. Load Cell Amplifier

Typical Applications (continued)

8.2.3 Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

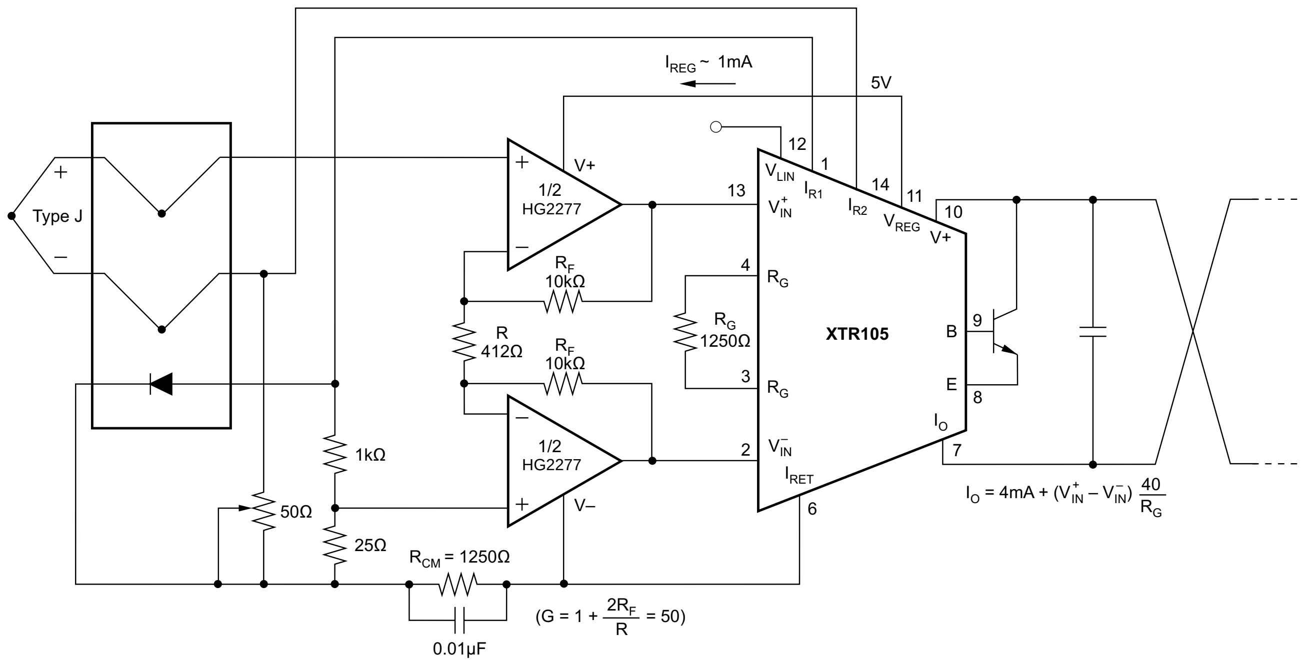


Figure 32. Thermocouple Low-Offset, Low-Drift Loop Measurement With Diode Cold Junction Compensation

10.3 DFN Package

The HGx277 series uses the 8-lead DFN (also known as SON), a QFN package with contacts on only two sides of the package bottom. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed-circuit-board (PCB) assembly techniques. See *QFN/SON PCB Attachment* (SLUA271) and *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at www.ti.com.

The exposed leadframe die pad on the bottom of the package should be connected to V–.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.