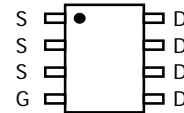# SPS source chips

SM4411

P-Channel Enhancement Mode Field Effect Transistor

Description

The SM4411 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge. This device is suitable for use as a load switch or in PWM applications.

Top View

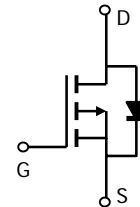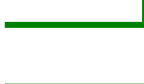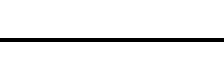**SOIC-8**

General Features

V_{DS} (V) = -30V

I_D = -8 A (V_{GS} = -10V)

$R_{DS(ON)}$ < 35mΩ (V_{GS} = -10V)

$R_{DS(ON)}$ < 58mΩ (V_{GS} = -4.5V)

◆ **Ordering Information**

Ordering Number		Package	Pin Assignment								Packing
Lead Free	Halogen Free		1	2	3	4	5	6	7	8	
SM4411PRL	SM4411PRG	SOP-8	S2	G2	S1	G1	D1	D1	D2	D2	Tape Reel

SM4411 X X X

(1)Package Type

(2)Packing Type

(3)Lead Free

(1) P：SOP-8

(2) R：Tape Reel

(3) G：Halogen Free；L：Lead Free

◆ Absolute Maximum Ratings $(T_A=25^oC$, unless otherwise noted)

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [A]	$T_A=25°C$	I_D	-8	A
	$T_A=70°C$		-6.6	
Pulsed Drain Current [B]		I_{DM}	-40	
Power Dissipation [A]	$T_A=25°C$	P_D	3	W
	$T_A=70°C$		2.1	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

a:Fused current that based on wire numbers and diameter

b:Repetitive Rating: Pulse width limited by the maximum junction temperature

c:1-in^2 2oz Cu PCB board

◆ Electrical Characteristics $(T_A=25°C$, unless otherwise noted)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
STATIC PARAMETERS							
BV_{DSS}	Drain-Source Breakdown Voltage	$I_D=-250\mu A$, $V_{GS}=0V$		-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-24V$, $V_{GS}=0V$				-1	μA
			$T_J=55°C$			-5	
I_{GSS}	Gate-Body leakage current	$V_{DS}=0V$, $V_{GS}=±20V$				±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}$ $I_D=-250\mu A$		-1.2	-2	-2.4	V
$I_{D(ON)}$	On state drain current	$V_{GS}=-10V$, $V_{DS}=-5V$		-40			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	$V_{GS}=-10V$, $I_D=-8A$			24.5	32	mΩ
			$T_J=125°C$		33		
		$V_{GS}=-4.5V$, $I_D=-5A$			41	55	mΩ
g_{FS}	Forward Transconductance	$V_{DS}=-5V$, $I_D=-8A$			14.5		S
V_{SD}	Diode Forward Voltage	$I_S=-1A$, $V_{GS}=0V$			-0.76	-1	V
I_S	Maximum Body-Diode Continuous Current					-4.2	A
DYNAMIC PARAMETERS							
C_{iss}	Input Capacitance	$V_{GS}=0V$, $V_{DS}=-15V$, f=1MHz			920	1120	pF
C_{oss}	Output Capacitance				190		pF
C_{rss}	Reverse Transfer Capacitance				122		pF
R_g	Gate resistance	$V_{GS}=0V$, $V_{DS}=0V$, f=1MHz			3.6	5	Ω
SWITCHING PARAMETERS							
$Q_g(10V)$	Total Gate Charge (10V)	$V_{GS}=-10V$, $V_{DS}=-15V$, $I_D=-8A$			18.4	23	nC
$Q_g(4.5V)$	Total Gate Charge (4.5V)				9.3	11.5	nC
Q_{gs}	Gate Source Charge				2.7		nC
Q_{gd}	Gate Drain Charge				4.9		nC
$t_{D(on)}$	Turn-On DelayTime	$V_{GS}=-10V$, $V_{DS}=-15V$, $R_L=1.8\Omega$, $R_{GEN}=3\Omega$			7.1		ns
t_r	Turn-On Rise Time				3.4		ns
$t_{D(off)}$	Turn-Off DelayTime				18.9		ns
t_f	Turn-Off Fall Time				8.4		ns
t_{rr}	Body Diode Reverse Recovery Time	$I_F=-8A$, dI/dt=100A/μs			21.5	27	ns
Q_{rr}	Body Diode Reverse Recovery Charge	$I_F=-8A$, dI/dt=100A/μs			12.5		nC

Note: Pulse Test: Pulse Width ≤300us, Duty Cycle≤2%

d: Guaranteed by design: not subject to production testing

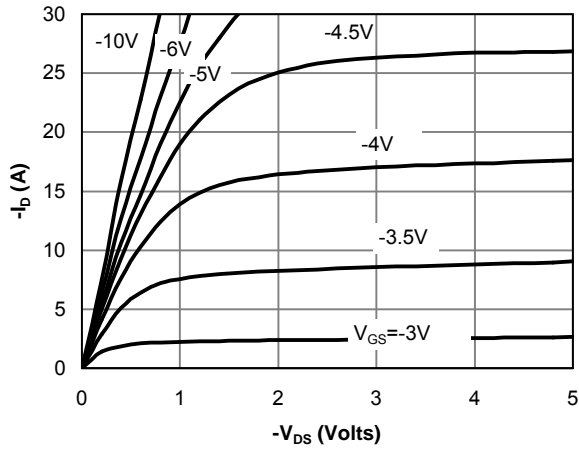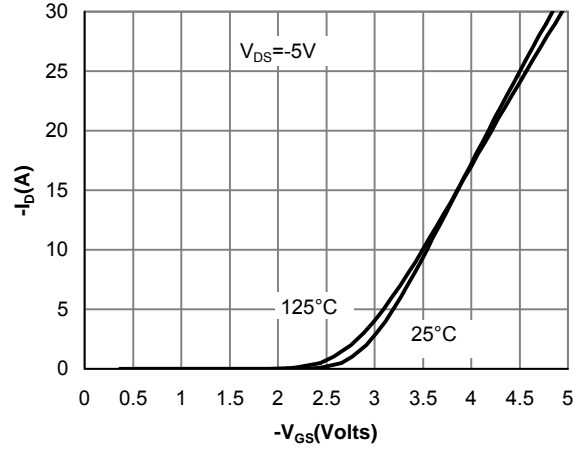TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

Fig 1: On-Region Characteristics
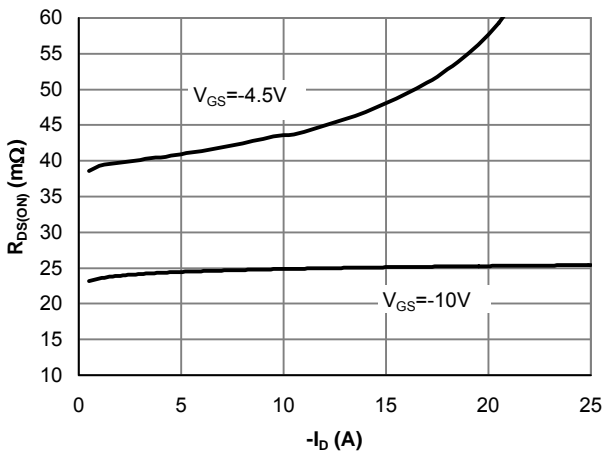
Figure 2: Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current and Gate Voltage
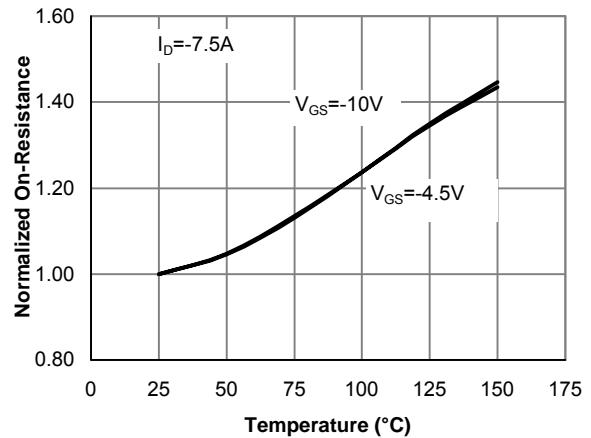
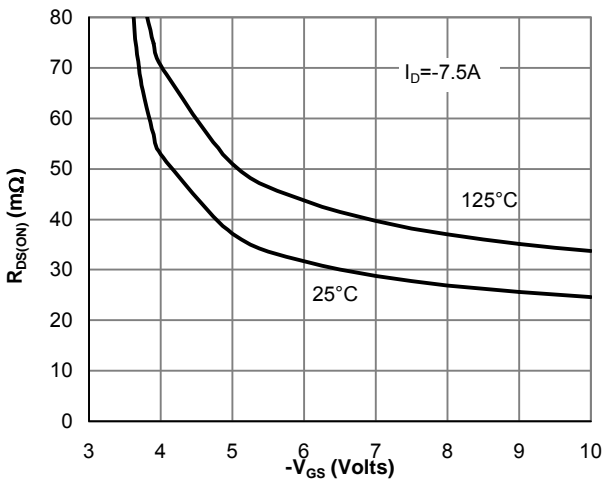**Figure 4: On-Resistance vs. Junction Temperature**
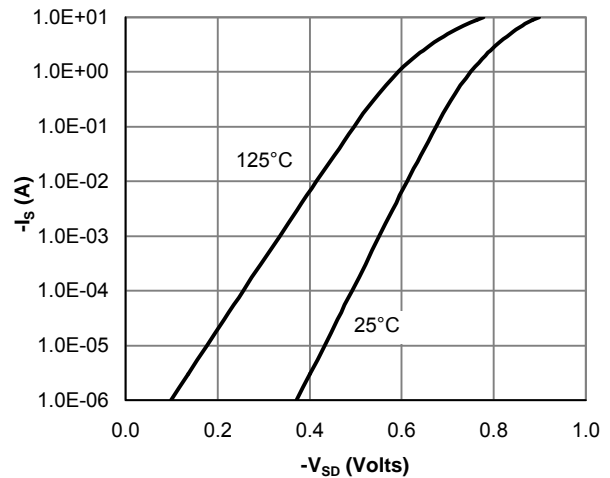
Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics
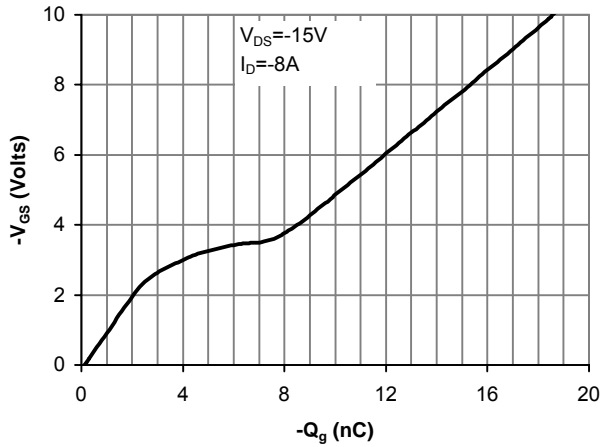
TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

V_{DS}=-15V
I_D=-8A

Figure 7: Gate-Charge Characteristics

C_{iss}

C_{oss} C_{rss}
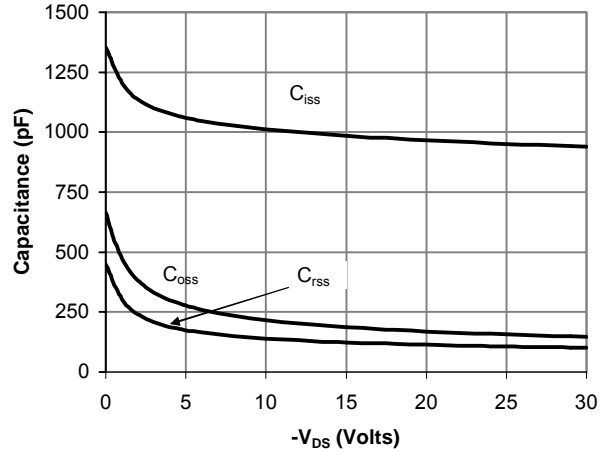
Figure 8: Capacitance Characteristics

$T_{J(Max)}$=150°C, T_A=25°C

10μs

$R_{DS(ON)}$ limited

100μs

0.1s   1ms

10ms

1s

10s

DC
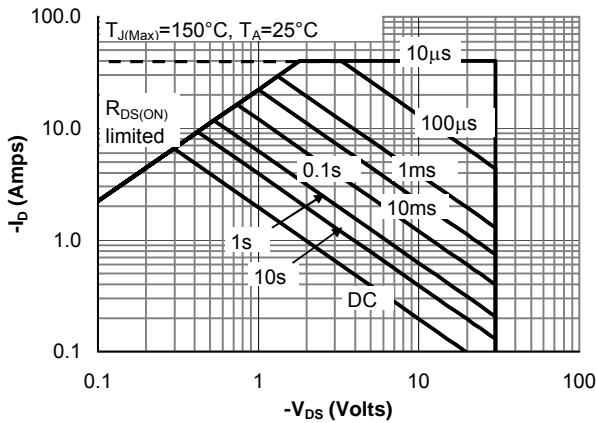
Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

$T_{J(Max)}$=150°C
T_A=25°C
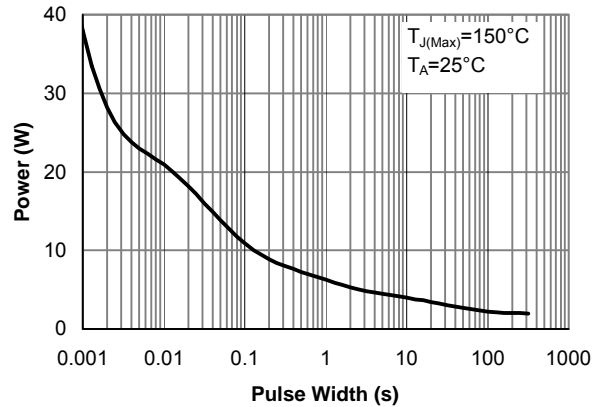
Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

$D=T_{on}/T$
$T_{J,PK}=T_A+P_{DM} \cdot Z_{\theta JA} \cdot R_{\theta JA}$
$R_{\theta JA}$=40°C/W

In descending order
D=0.5, 0.3, 0.1, 0.05, 0.02, 0.01, single pulse
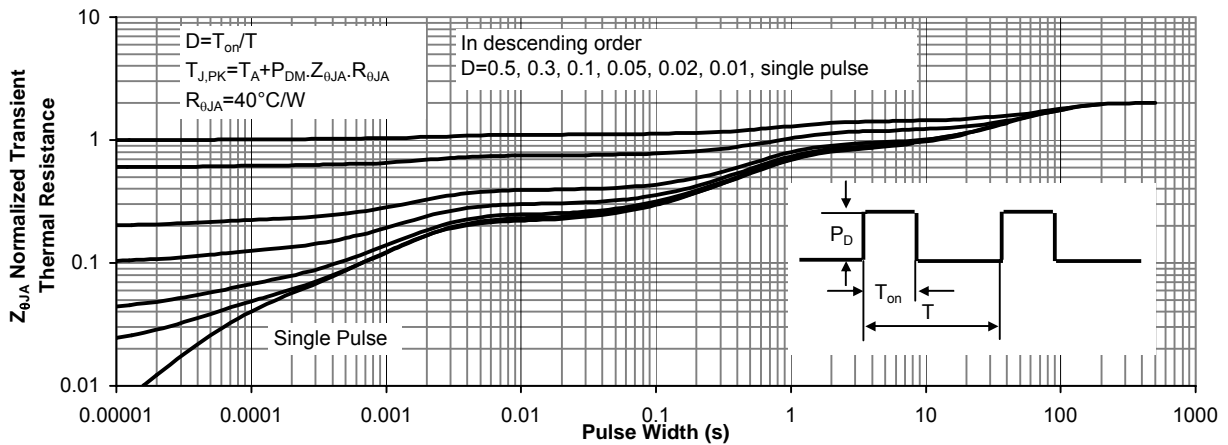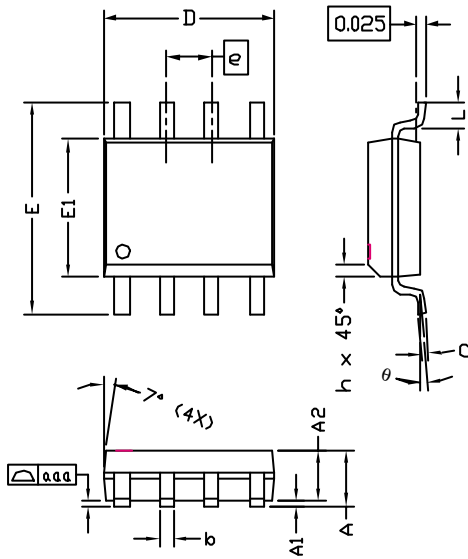
P_D

T_{on}

T

Single Pulse

Figure 11: Normalized Maximum Transient Thermal Impedance

SO-8 Package Data

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.45	1.50	1.55	0.057	0.059	0.061
A1	0.00	——	0.10	0.000	——	0.004
A2	——	1.45	——	——	0.057	——
b	0.33	——	0.51	0.013	——	0.020
c	0.19	——	0.25	0.007	——	0.010
D	4.80	——	5.00	0.189	——	0.197
E1	3.80	——	4.00	0.150	——	0.157
e	1.27 BSC			0.050 BSC		
E	5.80	——	6.20	0.228	——	0.244
h	0.25	——	0.50	0.010	——	0.020
L	0.40	——	1.27	0.016	——	0.050
aaa	——	——	0.10	——	——	0.004
θ	0°	——	8°	0°	——	8°

NOTE:
1. LEAD FINISH: 150 MICROINCHES (3.8 um) MIN.
   THICKNESS OF Tin/Lead (SOLDER) PLATED ON LEAD
2. TOLERANCE   ±0.100 mm (4 mil) UNLESS OTHERWISE
   SPECIFIED
3. COPLANARITY : 0.1000 mm
4. DIMENSION L IS MEASURED IN GAGE PLANE

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