

STRUCTURE Silicon Monolithic Integrated Circuit  
 PRODUCT SERIES Motor Driver for electronic camera module

TYPE **BU64240GWZ**

- FEATURES
- Linear current sink driver
  - 10bit resolution current control
  - I<sup>2</sup>C serial Interface
  - Integrated current sense resistor
  - Intelligent Slew Rate Control(ISRC) for mechanical ringing compensation

●Absolute maximum ratings

Parameter	Symbol	Limit	Unit
Power supply voltage	VCC	-0.5 to +5.5	V
Power save input voltage	VPS	-0.5 to 5.5	V
Control input voltage <sup>※1</sup>	VIN	-0.5 to 5.5	V
Power dissipation	Pd	220 <sup>※2</sup>	mW
Operating temperature range	Topr	-25 to +85	°C
Junction temperature	Tjmax	125	°C
Storage temperature range	Tstg	-55 to +125	°C
Output current	Iout	+200 <sup>※3</sup>	mA

※1 VIN is I2C BUS input pin (SCL, SDA).

※2 Reduced by 2.2 mW/°C over 25°C, when mounted on a glass epoxy board (50mm × 58mm × 1.75mm; 8 layers)

※3 Must not exceed Pd, ASO, or Tjmax of 125°C.

●Operating Conditions (Ta= -25°C to +85°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VCC	2.3	3.0	4.8	V
Power save input voltage	VPS	0	-	4.8	V
Control input voltage	VIN	0	-	4.8	V
I <sup>2</sup> C Bus Frequency	fCLK	-	-	400	kHz
Output current	Iout	-	-	130 <sup>※4</sup>	mA

※4 Must not exceed Pd, ASO.

● Electrical Characteristics (Unless otherwise specified Ta=25°C, VCC=3.0V )

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
<b>Overall</b>						
Circuit current during standby operation	ICCST	-	0	5	μA	PS=0V
Circuit current	ICC	-	0.6	1.0	mA	PS=3V, SCL=400kHz
<b>Power save input</b>						
High level input voltage	VPSH	1.26	-	VCC	V	
Low level input voltage	VPSL	0	-	0.5	V	
Low level input current	IPSL	-10	-	10	μA	VPS=0V
High level input current	IPSH	-10	-	10	μA	VPS=3V
<b>Control input (VIN=SCL, SDA)</b>						
High level input voltage	VINH	1.26	-	VCC	V	
Low level input voltage	VINL	0	-	0.5	V	
Low level output voltage	VINOL	-	-	0.4	V	IIN=+3.0mA (SDA)
High level input current	IINH	-10	-	10	μA	Input voltage=0.9 × VIN
Low level input current	IINL	-10	-	10	μA	Input voltage=0.1 × VIN
<b>UVLO</b>						
UVLO voltage	VUVLO	1.6	-	2.2	V	
<b>10bit D/A converter(for setting limit voltage)</b>						
Resolution	DRES	-	10	-	Bits	
Differential Nonlinearity	DDNL	-1	-	1	LSB	
Integral Nonlinearity	DINL	-4	-	4	LSB	
<b>Constant-Current Driver block</b>						
Output current resolution	IORES	-	126	-	μA	
Output maximum current	IOMAX	117	130	143	mA	DACcode = 3'h3FF
Zero code offset current	IOOFS	0	1	5	mA	DACcode = 3'h000
Output Voltage	VOOUT	-	150	200	mV	Io = 100mA
Maximum applied voltage	VOMAX	-	-	VCC	V	

This specification is supposed to be revised for improvement etc.

●Package Outline

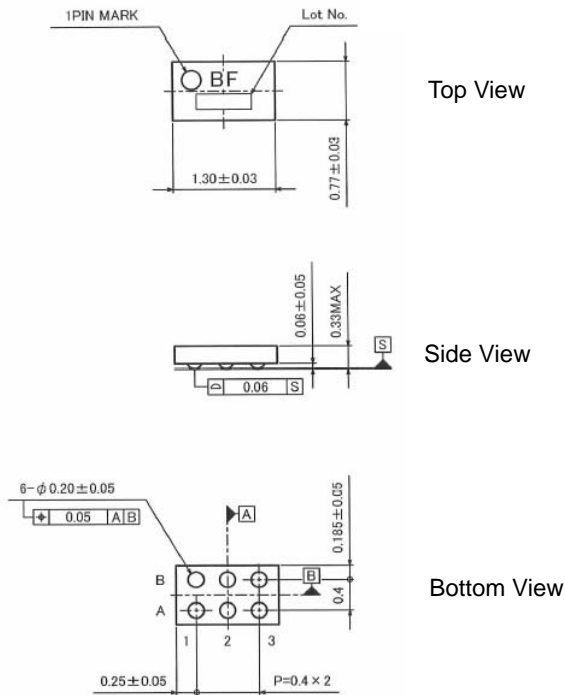


Fig.1 UCSP30L1 Package (Unit: mm)

●Pin Arrangement (Top View)

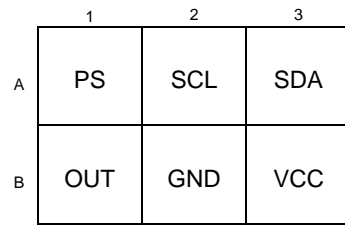


Fig.2 BU64240GWZ Pin Arrangement (Top View)

●Block Diagram

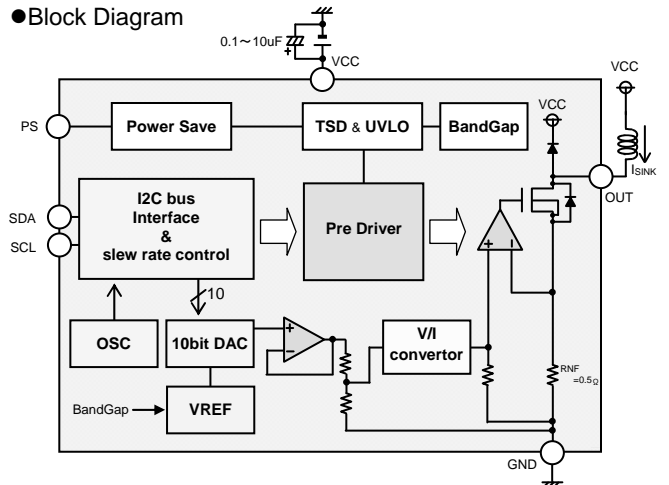
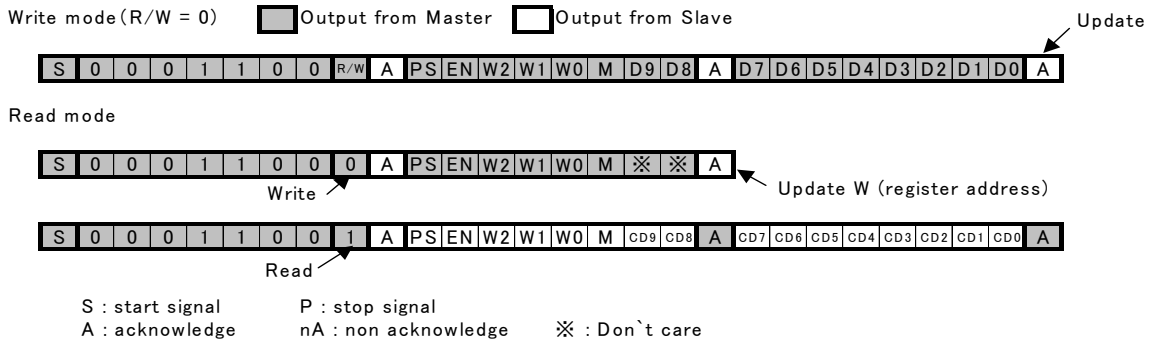


Fig.3 BU64240GWZ Block Diagram

●I2C BUS Format (Fast mode: SCL=400kHz)



Register name	Setting item	Description
PS	Serial power save	'0' = Standby mode, '1' = Operating mode
EN	OUT pin status	'0' = Hi-impedance, '1' = Constant current sink.
M	Mode select signal	'0' = ISRC Mode Disabled, '1' = ISRC Mode Enabled
W2W1W0	Register address	'000' = Limit Voltage setting, '001' = Operating parameter setting1 '010' = Operating parameter setting2, '011' = Operating parameter setting 3 '100' = Operating parameter setting4
D9~D0	Limit Voltage	Target position DAC code[D9:D0]
	Operating parameter1	Resonance frequency setting[D7:D3], Slew rate speed setting[D1:D0]
	Operating parameter2	VCM un-control current setting1[D9:D0]
	Operating parameter3	VCM un-control current setting2[D9:D0]
	Operating parameter4	Step resolution[D7:D5] ( Minimum step resolution = 1LSB@10bit_DAC) Step time setting[D4:D0] ( Minimum step time resolution = 50us )

- Characteristics of the SDA and SCL bus lines for 2-wire serial interface.  
(Unless otherwise specified,  $T_a = -25 \sim +85^\circ\text{C}$ ,  $V_{CC} = 2.3 \sim 4.8\text{V}$ )

Parameter	Symbol	STANDARD-MODE <sup>※6</sup>		FAST-MODE <sup>※6</sup>		Unit
		Min.	Max.	Min.	Max.	
LOW level input voltage	VIL	-0.5	0.5	-0.5	0.5	V
High level input voltage	VIH	1.26	4.8	1.26	4.8	V
Hysteresis of Schmitt trigger inputs	Vhys	-	-	0.15	-	V
LOW level output voltage at 3mA sink current	VOL	0	0.4	0	0.4	V
Pulse width of spikes which must be suppressed by the input filter	tSP	0	50	0	50	ns
Input current each I/O pin with an input voltage between 0.1V and 0.9V <sub>INmax</sub>	Ii	-10	10	-10	10	uA
SCL clock frequency	fSCL	-	100	-	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	tHD;STA	4.0	-	0.6	-	us
LOW period of the SCL clock	tLOW	4.7	-	1.3	-	us
High period of the SCL clock	tHIGH	4.0	-	0.6	-	us
Set-up time for repeated START condition	tSU;STA	4.7	-	0.6	-	us
Data hold time	tHD;DAT	0	3.45	0	0.9	us
Data set-up time	tSU;DAT	250	-	100	-	ns
Set-up time for STOP condition	tSU;STO	4.0	-	0.6	-	us
Bus free time between a STOP and START condition	tBUF	4.7	-	1.3	-	us

※6 STANDARD-MODE and FAST-MODE 2-wire serial interface devices must be able to transmit or receive at that speed.  
The maximum bit transfer rates of 100 kbit/s for STANDARD-MODE devices and 400 kbit/s for FAST-MODE devices  
This transfer rates is provided the maximum transfer rates, for example it is able to drive 100 kbit/s of clocks with FAST-MODE.

- Definition of timing on the 2-wire serial interface

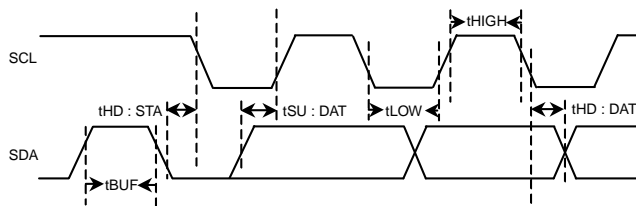


Fig.4 Definition of timing for serial data

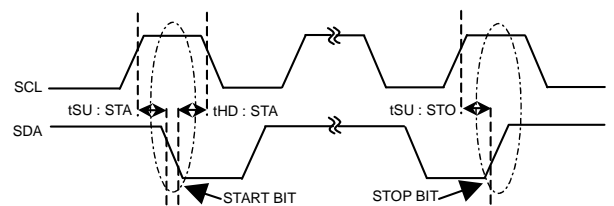


Fig.5 Definition of timing for START and STOP bit

●Operation Notes

(1) Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. The implementation of a physical safety measure such as a fuse should be considered when use of the IC in a special mode where the absolute maximum ratings may be exceeded is anticipated.

(2) Power supply lines

Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance in full consideration of all the characteristics of the electrolytic capacitor, because the electrolytic capacitor may lose some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

(3) Ground potential

Ensure a minimum GND pin potential in all operating conditions.

(4) Setting of heat

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

(5) Actions in strong magnetic field

Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

(6) ASO

When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

(7) Thermal shutdown circuit

This IC incorporates a TSD (thermal shutdown) circuit (TSD circuit). If the temperature of the chip reaches the following temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent runaway thermal operation. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

TSD ON temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
150	20

(8) Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the application's reference point so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

(9) Power Save (PS) terminal

PS holds the reset function on logic concurrently. Please release PS after the start-up of VCC. Reset is not normally done when VCC is short-circuited to PS and it uses it, and there is a possibility of malfunctions.

This specification is supposed to be revised for improvement etc

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