

Parameters Subject to Change Without Notice

DESCRIPTION

The JW[®]5052S is a current mode monolithic buck voltage converter. Operating with an input range of 3.7~18V, the JW5052S delivers 2A of continuous output current with two integrated N-Channel MOSFETs. At light loads, regulators operate in low frequency to maintain high efficiency and low output ripple.

The JW5052S guarantees robustness with short circuit protection, thermal protection, current run-away protection, and input under voltage lockout.

The JW5052S is available in a 6-pin TSOT23-6 package, which provides a compact solution with minimal external components.

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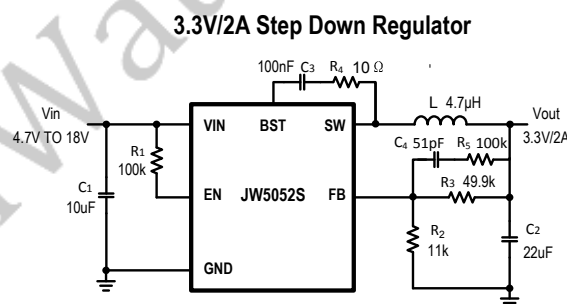
FEATURES

- 3.7V to 18V operating input range
- 2A output current
- Up to 95% efficiency
- High efficiency (>80%) at light load
- Fixed 800kHz Switching frequency
- Input under voltage lockout
- Start-up current run-away protection
- Over current protection and Hiccup
- Thermal protection
- Available in TSOT23-6 package

APPLICATIONS

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

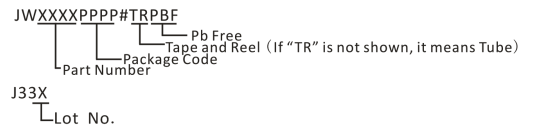
TYPICAL APPLICATION



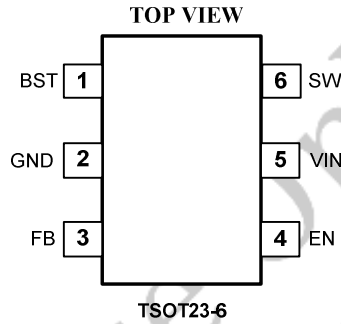
ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PACKAGE	TOP MARKING
JW5052STSOTB#PBF	JW5052STSOTB#TRPBF	TSOT23-6	JE2X

Note:



PIN CONFIGURATION



ABSOLUTE MAXIMUM RATING¹⁾

VIN, EN, SW Pin	-0.3V to 22V
BST Pin	SW-0.3V to SW+5V
All other Pins	-0.3V to 6V
Junction Temp. ^{2) 3)}	150°C
Lead Temperature	260°C

RECOMMENDED OPERATING CONDITIONS

Input Voltage VIN	3.7V to 18V
Output Voltage Vout	0.6V to VIN-3V

THERMAL PERFORMANCE⁴⁾

Absolute Max Storage Temp.	Recommended Operating Junction Temp. Range	Recommended Max Case Temp. T _c (°C)	Abs. Max Junction Temp. T _j (°C)	Recommended Max Power Loss P _{D@25°C} (W)
-65°C to 150°C	-40°C to 125°C	119	150	0.9
R _{θJC} (°C/W)	R _{θJA} (°C/W)	R _{θJB} (°C/W)	ψ _{JT} (°C/W)	ψ _{JB} (°C/W)
55	110	14.7	1.2	14.7

Note:

- 1) Exceeding these ratings may damage the device.
- 2) The JW5052S guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
- 3) The JW5052S includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
- 4) Measured on JESD51-7, 4-layer PCB

ELECTRICAL CHARACTERISTICS

<i>V_{IN}=12V, T_A=25 °C, Unless otherwise stated.</i>						
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
V _{IN} Under Voltage Lock-out Threshold	V _{IN_MIN}	V _{IN} rising	3.3	3.5	3.7	V
V _{IN} Under voltage Lockout Hysteresis	V _{IN_MIN_HYST}			300		mV
Shutdown Supply Current	I _{SD}	V _{EN} =0V		0.1	1	μA
Supply Current	I _Q	V _{EN} =5V, V _{FB} =1.2V		120	150	μA
Feedback Voltage	V _{FB}	3.7V<V _{IN} <20V	585	600	615	mV
Top Switch Resistance ⁵⁾	R _{DS(ON)T}			120		mΩ
Bottom Switch Resistance ⁵⁾	R _{DS(ON)B}			60		mΩ
Top Switch Leakage Current	I _{LEAK_TOP}	V _{IN} =20V, V _{EN} =0V, V _{SW} =0V		0.1	1	μA
Bottom Switch Leakage Current	I _{LEAK_BOT}	V _{IN} =20V, V _{EN} =0V, V _{SW} =20V		0.1	1	μA
Top Switch Current Limit ⁵⁾	I _{LIM_TOP}	Minimum Duty Cycle		3.8		A
Switch Frequency	F _{SW}		600	800	1000	kHz
Minimum On Time ⁵⁾	T _{ON_MIN}			100		ns
Minimum Off Time ⁵⁾	T _{OFF_MIN}	V _{FB} =0.4V		150		ns
EN Rising threshold voltage	V _{EN_TH}	V _{EN} rising	1.9	2	2.1	V
EN shut down hysteresis ⁵⁾	V _{EN_HYST}		150	170	200	mV
Thermal Shutdown ⁵⁾	T _{TSD}			145		°C
Thermal Shutdown hysteresis ⁵⁾	T _{TSD_HYST}			20		°C

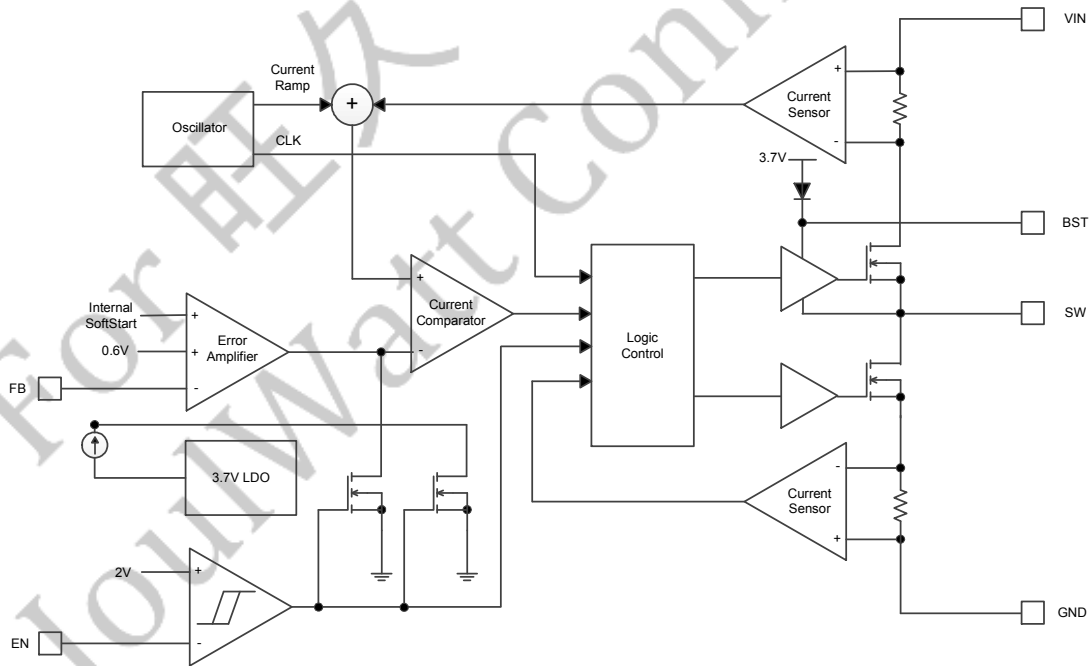
Note:

5) Guaranteed by design.

PIN DESCRIPTION

TSOT23-6 Pin	Name	Description
1	GND	Ground.
2	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 3.7V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
5	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
6	BST	Bootstrap pin for top switch. A 0.1uF or larger capacitor should be connected between this pin and the SW pin to supply current to the top switch and top switch driver.

BLOCK DIAGRAM

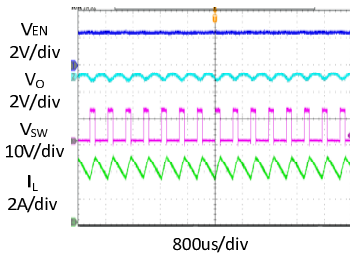


TYPICAL PERFORMANCE CHARACTERISTICS

Vin =12V, Vout = 3.3V, L = 4.7μH, Cout = 22μF, TA = +25°C, unless otherwise noted

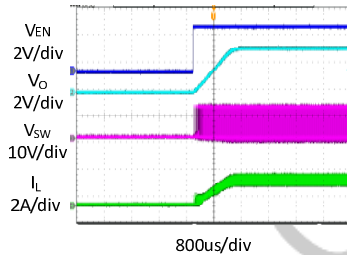
Steady State Test

VIN=12V, Vout=3.3V
Iout=2A



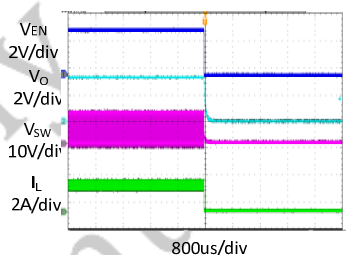
Startup through Enable

VIN=12V, Vout=3.3V
Iout=2A(Resistive load)



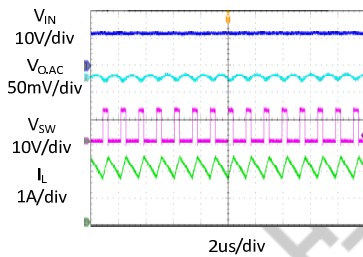
Shutdown through Enable

VIN=12V, Vout=3.3V
Iout=2A (Resistive load)



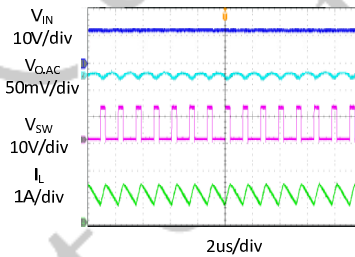
Heavy Load Operation

2A LOAD



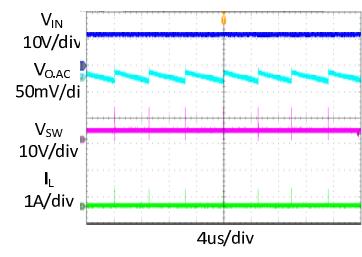
Medium Load Operation

1A LOAD



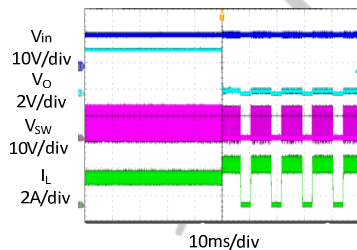
Light Load Operation

0 A LOAD



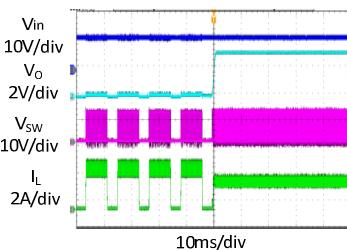
Short Circuit Protection

VIN=12V, Vout=3.3V
Iout=2A- Short



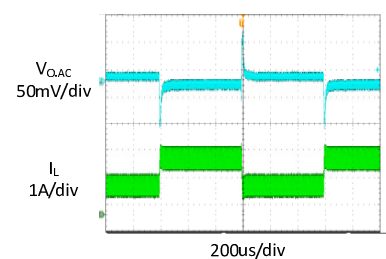
Short Circuit Recovery

VIN=12V, Vout=3.3V
Iout= Short-2A



Load Transient

1A LOAD → 2A LOAD → 1A LOAD



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Vin=12V, TA = +25°C, unless otherwise noted

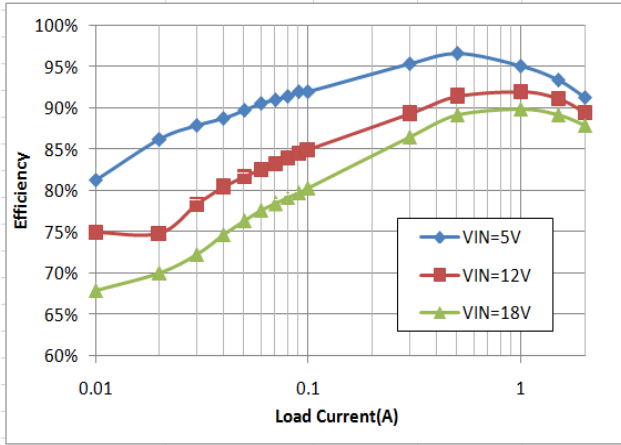


Figure 5. Efficiency vs Load Current (Vout=3.3V)

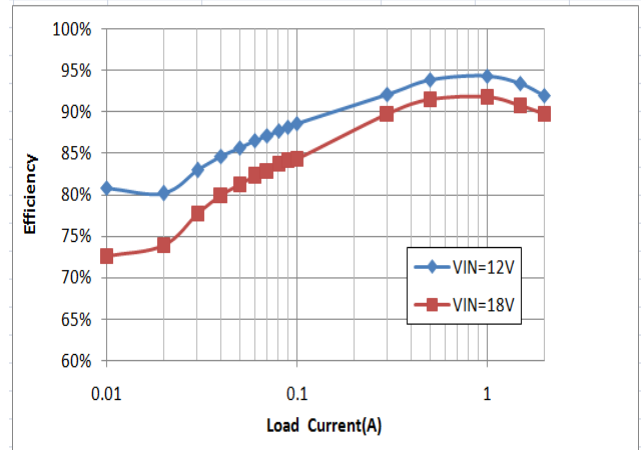


Figure 7. Efficiency vs Load Current (Vout=5V, L=4.7uH)

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FUNCTIONAL DESCRIPTION

The JW5052S is a synchronous, current-mode, step-down regulator. It regulates input voltages from 3.7V to 18V down to an output voltage as low as 0.6V, and is capable of supplying up to 2A of load current.

Current-Mode Control

The JW5052S utilizes current-mode control to regulate the FB voltage. Voltage at the FB pin is regulated at 0.6V so that by connecting an appropriate resistive divider between VOUT and GND, designed output voltage can be achieved.

PFM Mode

The JW5052S operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Internal Soft-Start.

Soft-Start makes output voltage rising smoothly follow an internal SS voltage until SS voltage is higher than the internal reference voltage. It can prevent overshoot of output voltage when startup.

Power Switch

N-Channel MOSFET switches are integrated on the JW5052S to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and GND, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 2V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the JW5052S so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Over Current Protection and Hiccup

JW5052S has a cycle-by-cycle current limit. When the inductor current triggers current limit, JW5052S enters hiccup mode and periodically restart the chip.

JW5052S will exit hiccup mode while not triggering current limit.

Thermal Protection

When the temperature of the JW5052S rises above 145°C, it is forced into thermal shut-down.

Only when core temperature drops below 125°C can the regulator becomes active again.

APPLICATION INFORMATION

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_2 + R_3}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_2 around 10kΩ, and then R_3 can be calculated by:

$$R_3 = R_2 \left(\frac{V_{OUT}}{0.6V} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

Vout(V)	R2(kΩ)	R3(kΩ)
2.5	10	31.6
3.3	11	49.9
5	15	110

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where I_{LOAD} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C_1 is the input capacitance value, f_s is the switching frequency, ΔV_{IN} is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2} \right)$$

where C_2 is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22uF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum

switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

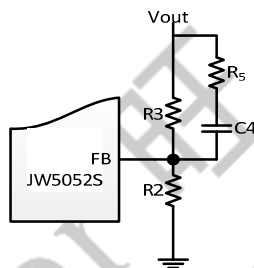
where V_{IN} is the input voltage, V_{OUT} is the output voltage, f_s is the switching frequency, and ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to be connected to the BST pin and SW pin.

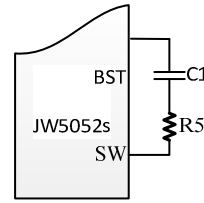
Feed Forward Note

In order to improve the dynamic performance, a feed forward capacitor in series with a resistor should be in parallel to the upper divider resistor. Choose R_5 around 100kΩ and C_4 around 51pF.



Start up through EN

If JW5052S slow start up through V_{in} when $V_{in}=5V$, $V_{out}=3.3V$, a 10Ω resistor should be connected in series with 100nF capacitor between BST pin and SW to make the output waveform become monotonic .



PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5052S (V_{IN} pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

Figure 1. Top Layer

Figure 2. Bottom Layer

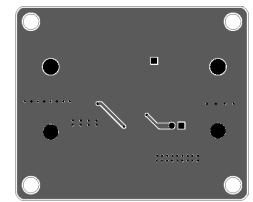
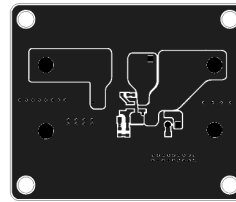
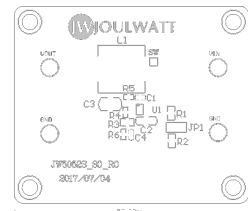


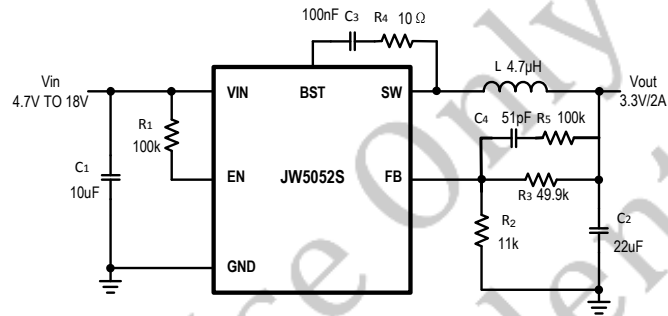
Figure 3. Top-Silk Layer



REFERENCE DESIGN

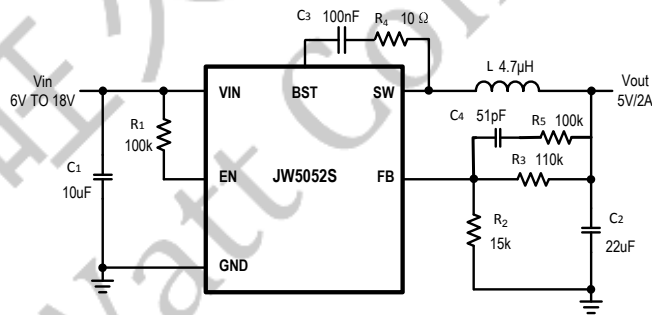
Reference 1:

V_{IN} : 4.7V ~ 18V
 V_{OUT} : 3.3V
 I_{OUT} : 0~2A

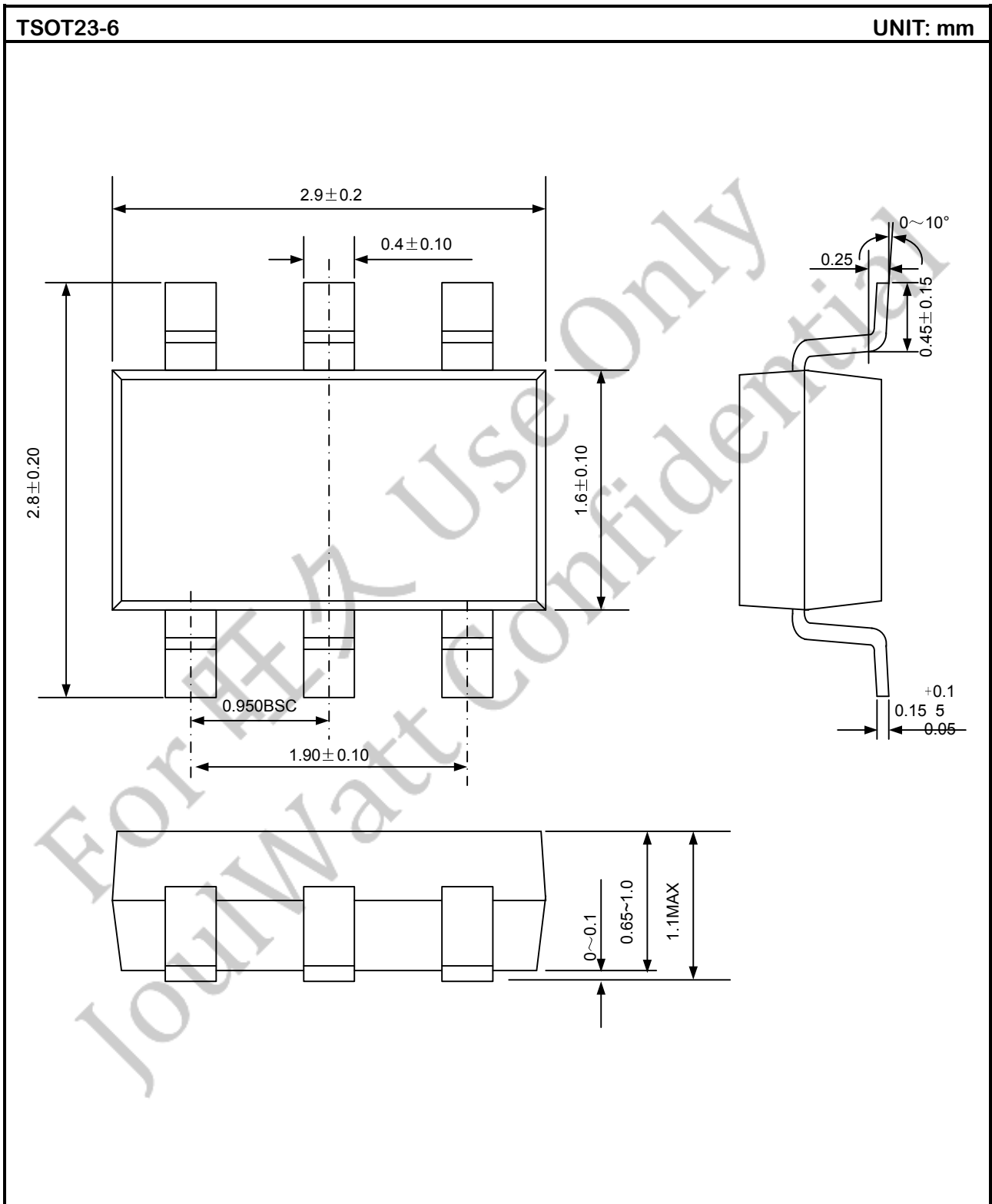


Reference 2:

V_{IN} : 6V ~ 18V
 V_{OUT} : 5V
 I_{OUT} : 0~2A



PACKAGE OUTLINE



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